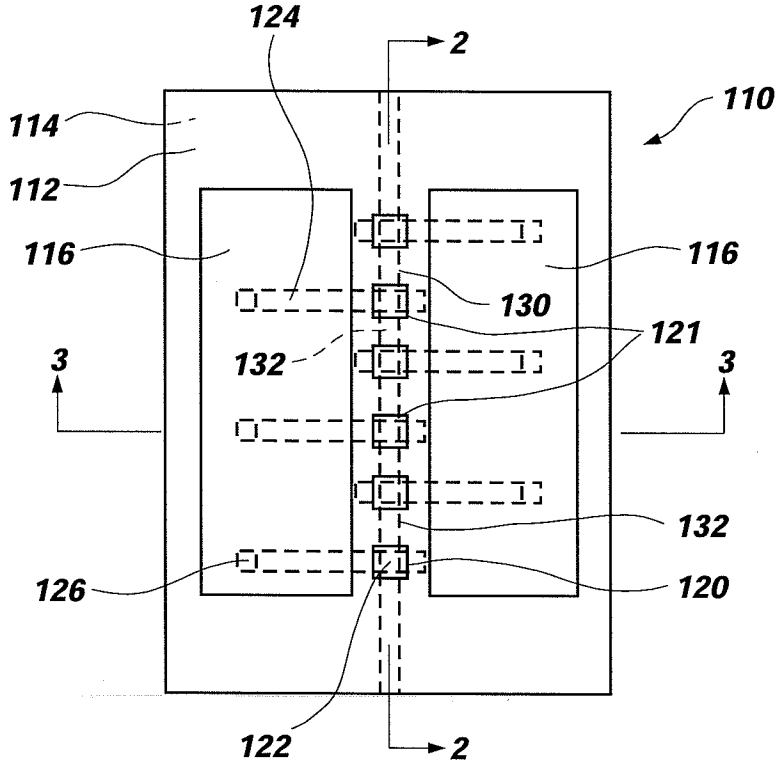


Fig. 1

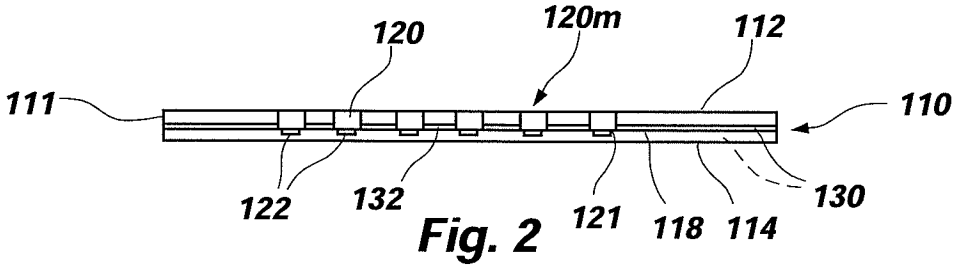


Fig. 2

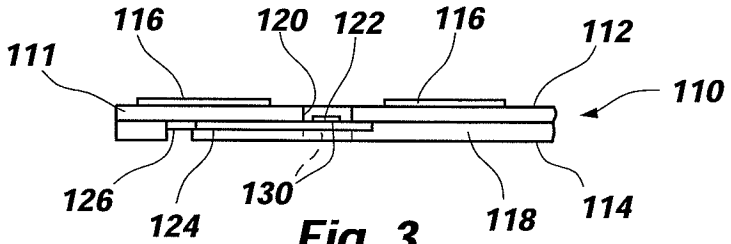


Fig. 3

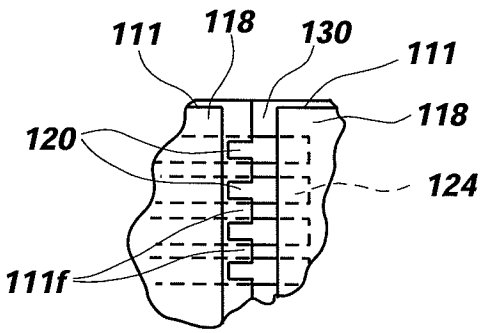


Fig. 1A

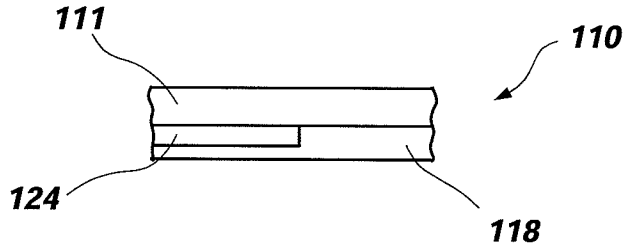


Fig. 4A

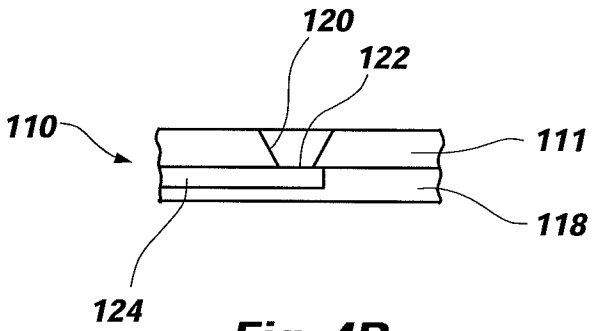


Fig. 4B

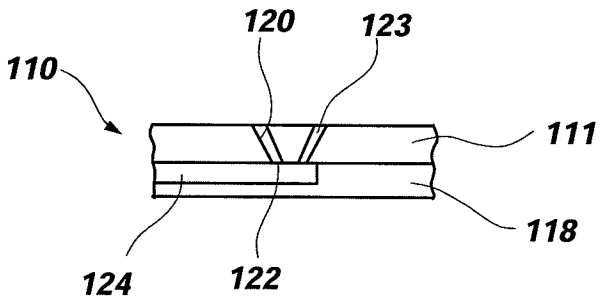


Fig. 4C

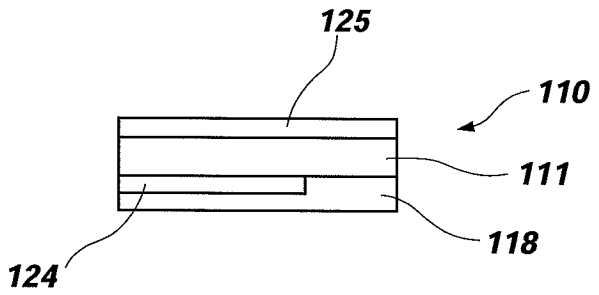


Fig. 5A

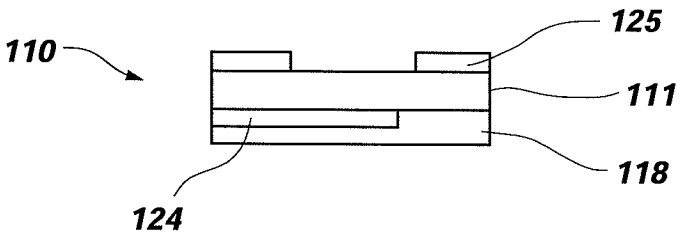


Fig. 5B

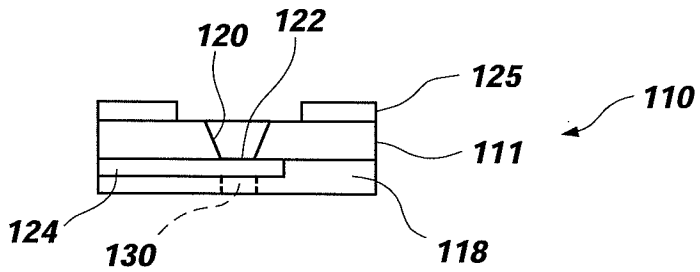


Fig. 5C

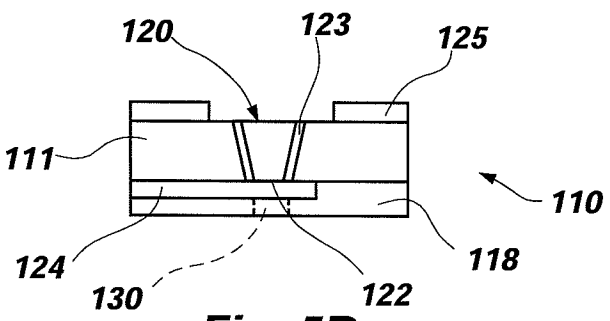


Fig. 5D

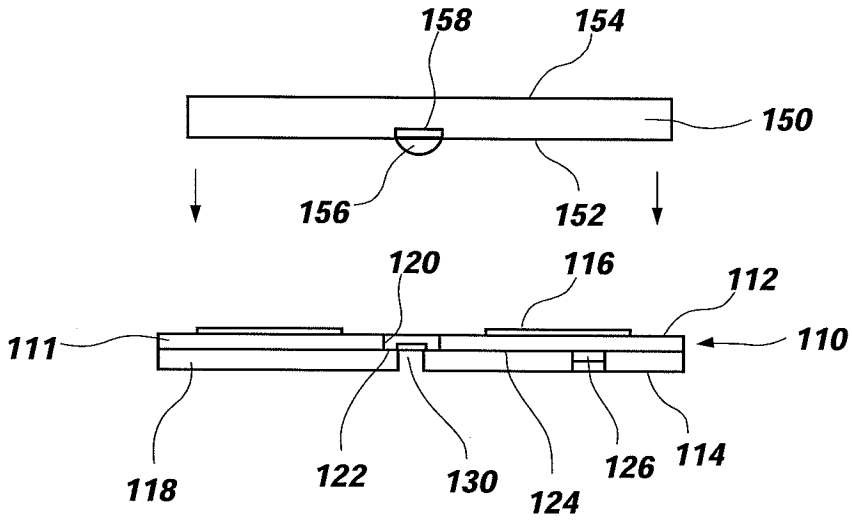

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Fig. 6A

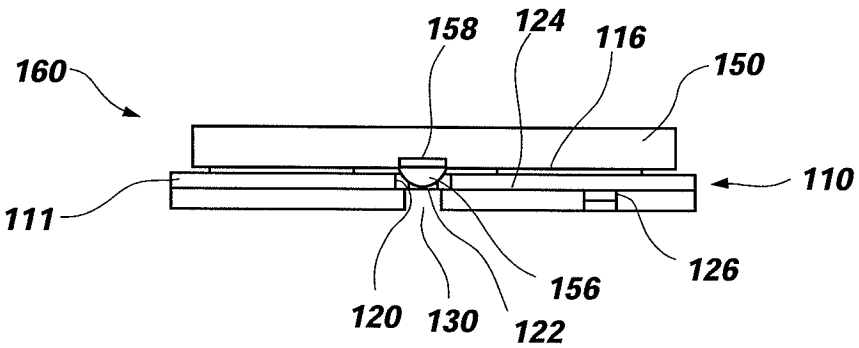

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Fig. 6B

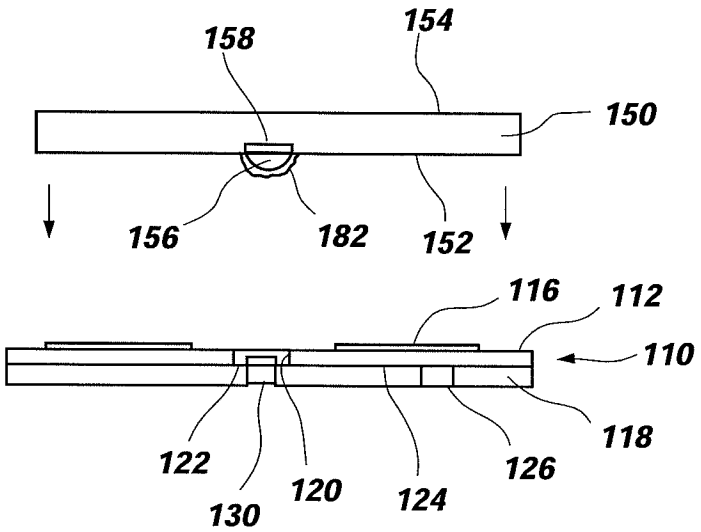

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Fig. 7A

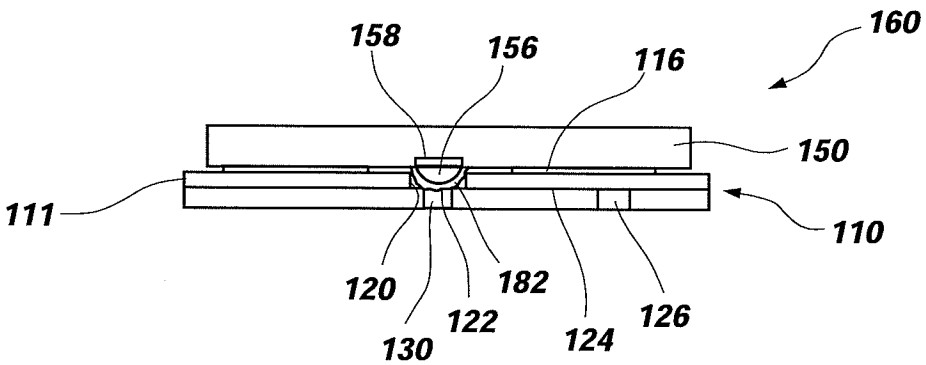

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Fig. 7B

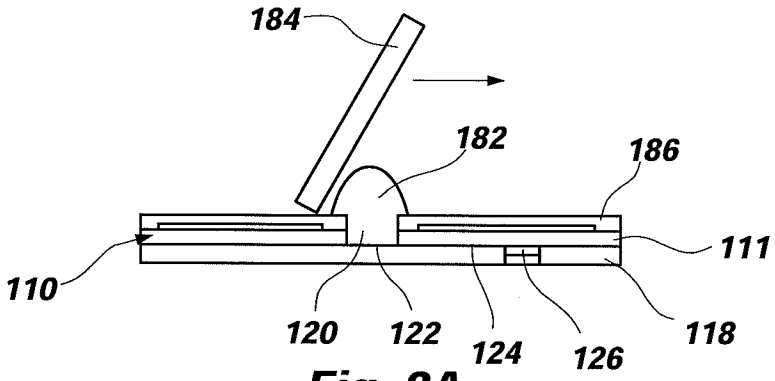


Fig. 8A

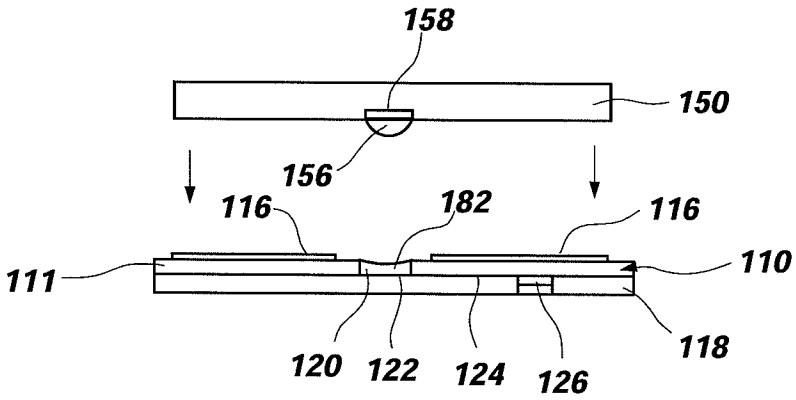


Fig. 8B

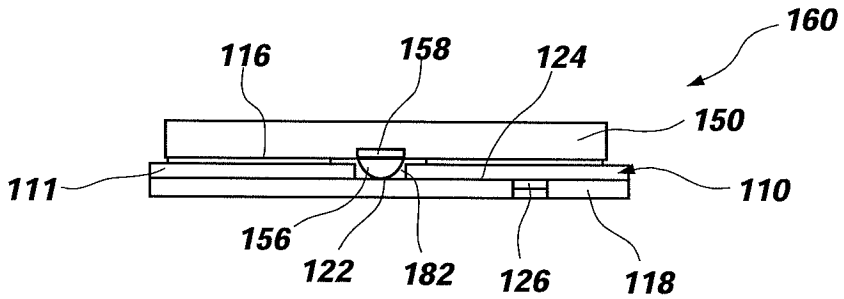


Fig. 8C

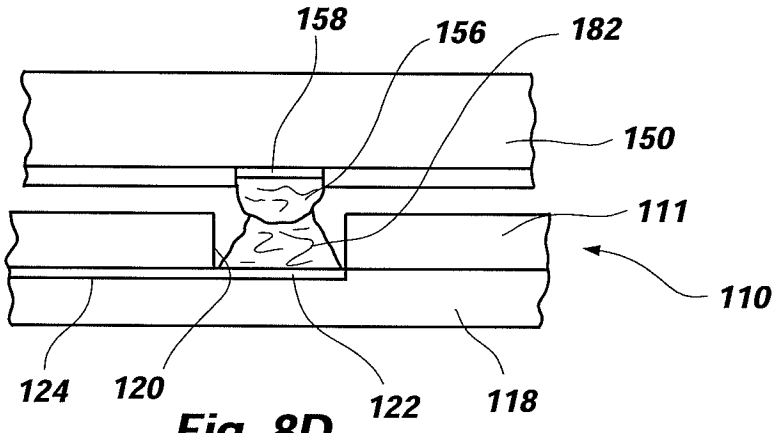


Fig. 8D

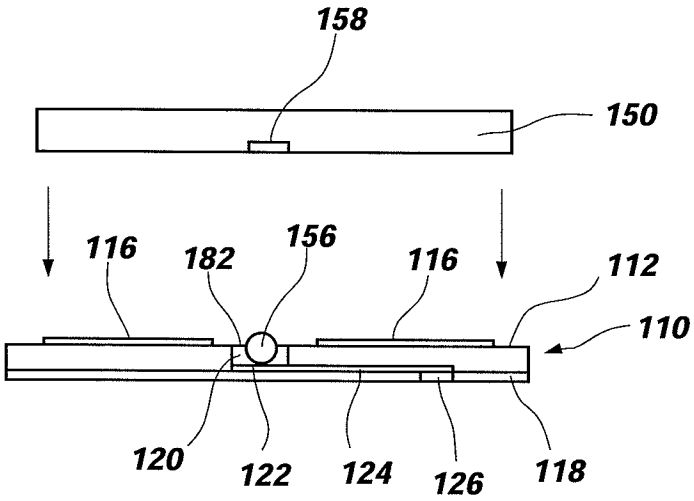

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Fig. 9A

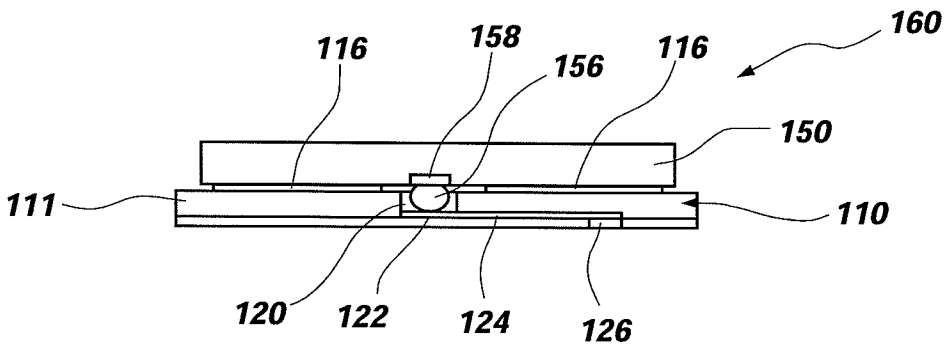

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Fig. 9B

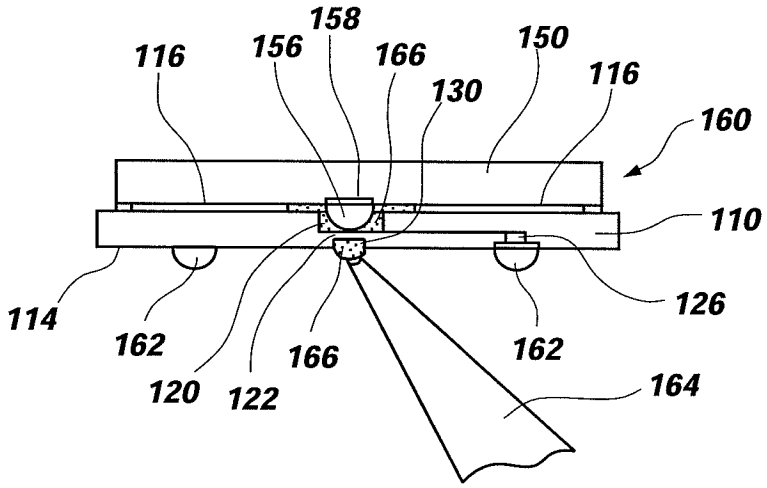

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Fig. 10

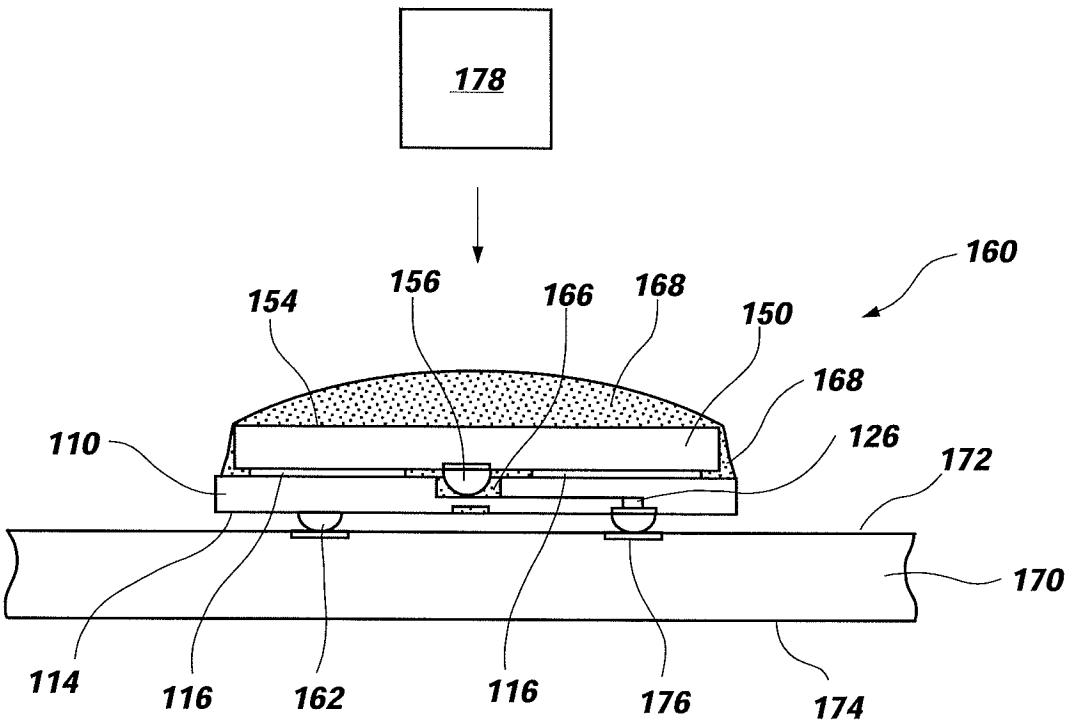

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Fig. 11

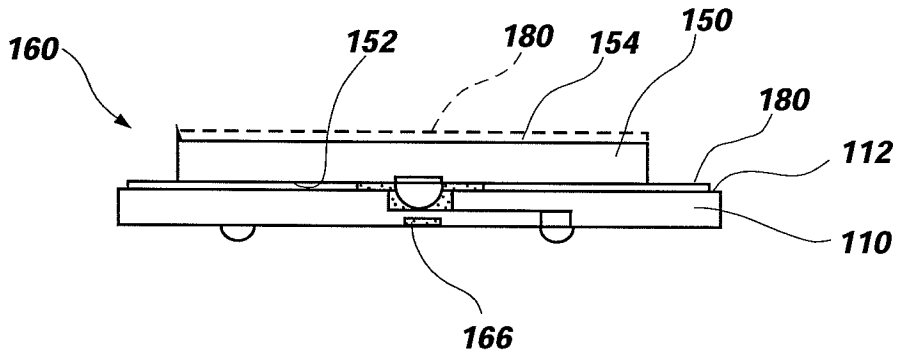


Fig. 12

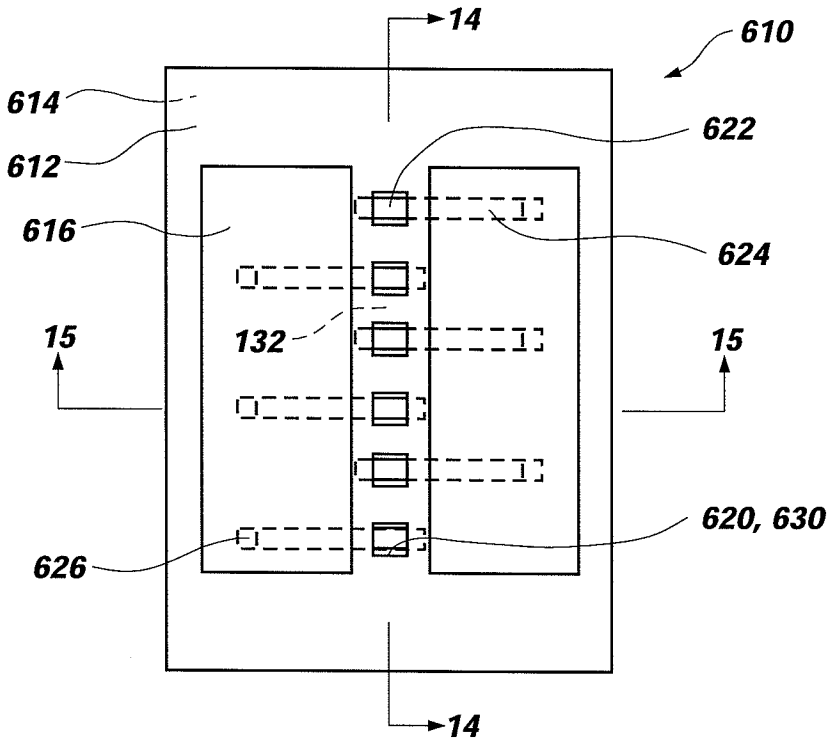


Fig. 13

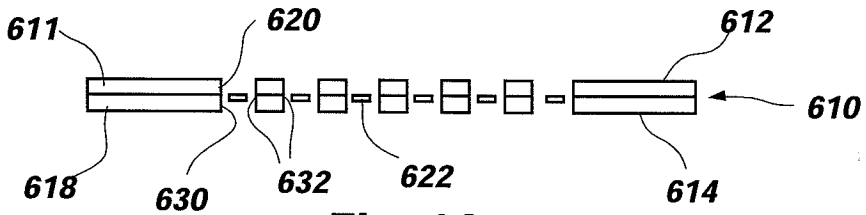


Fig. 14

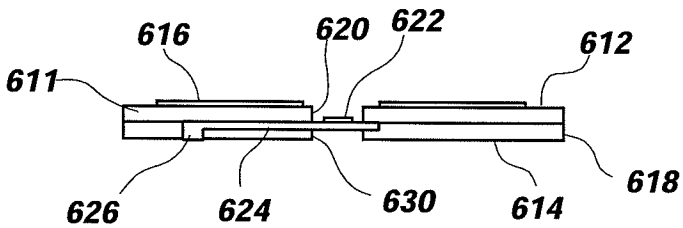


Fig. 15

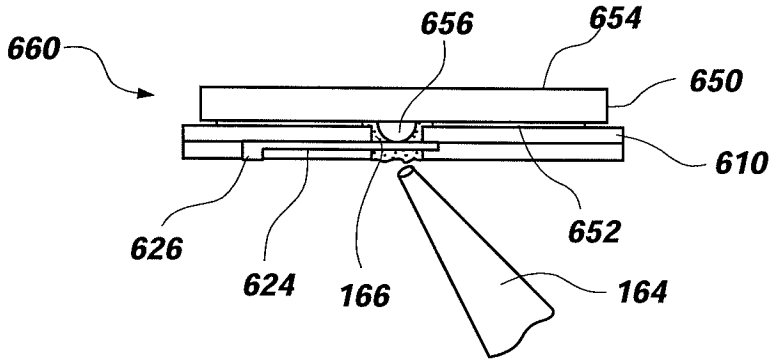


Fig. 16

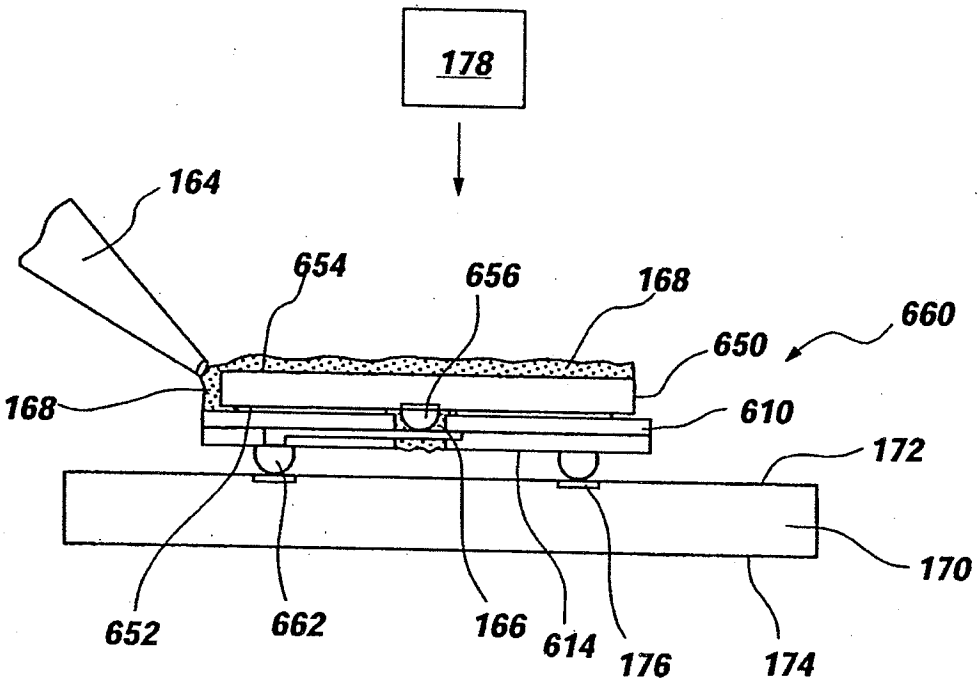

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Fig. 17

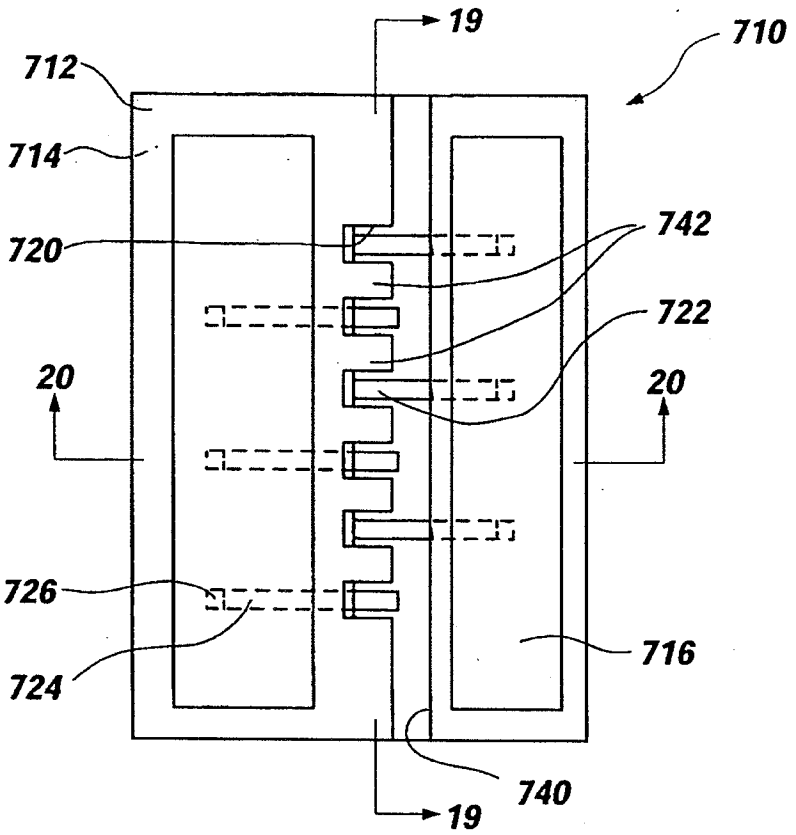


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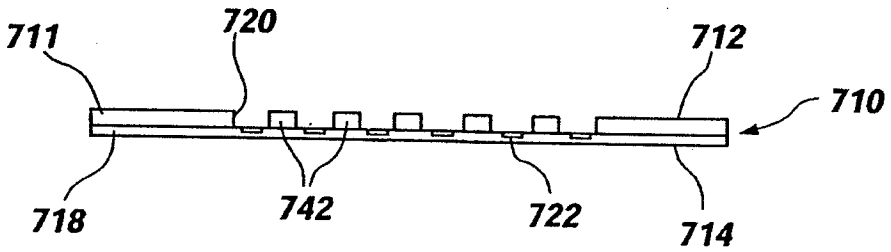


Fig. 19

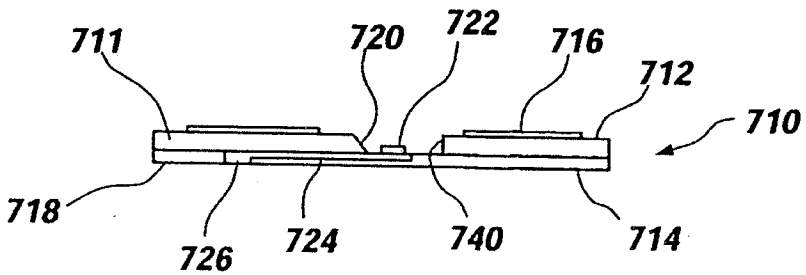


Fig. 20

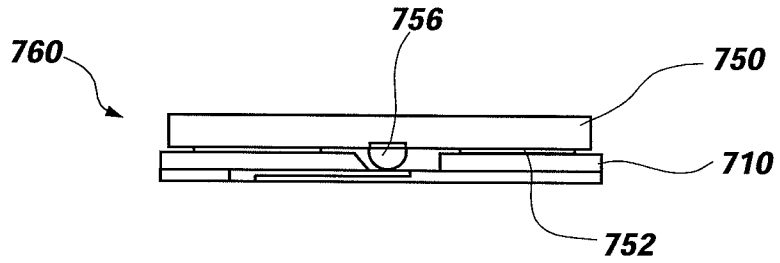


Fig. 21

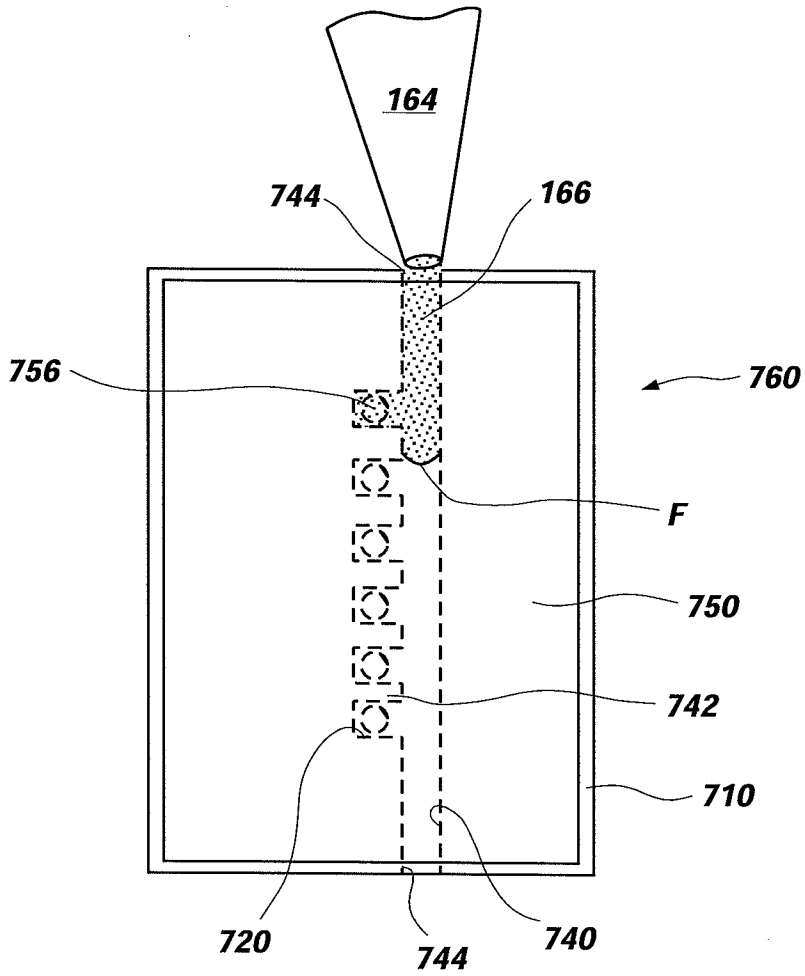


Fig. 22

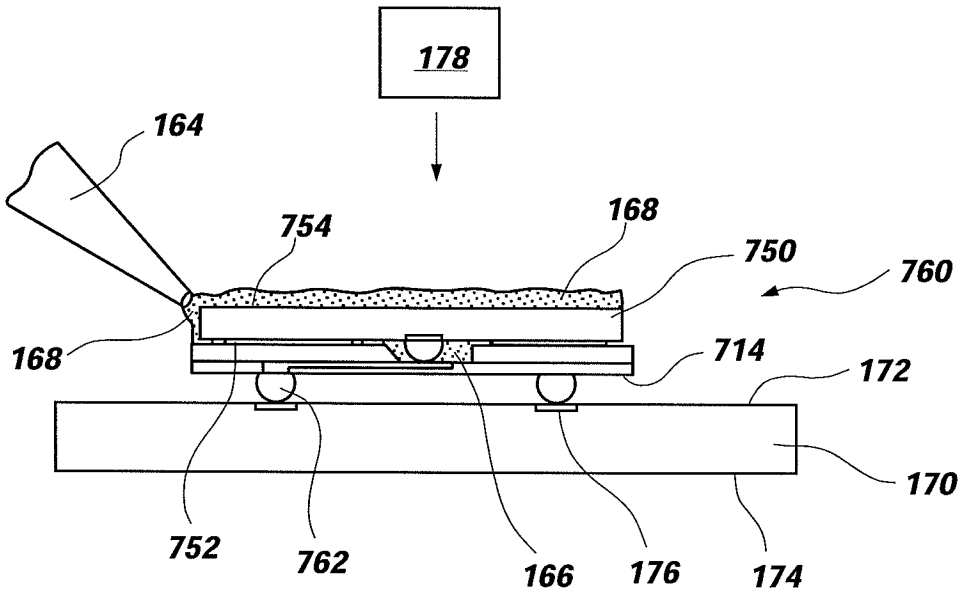


Fig. 23

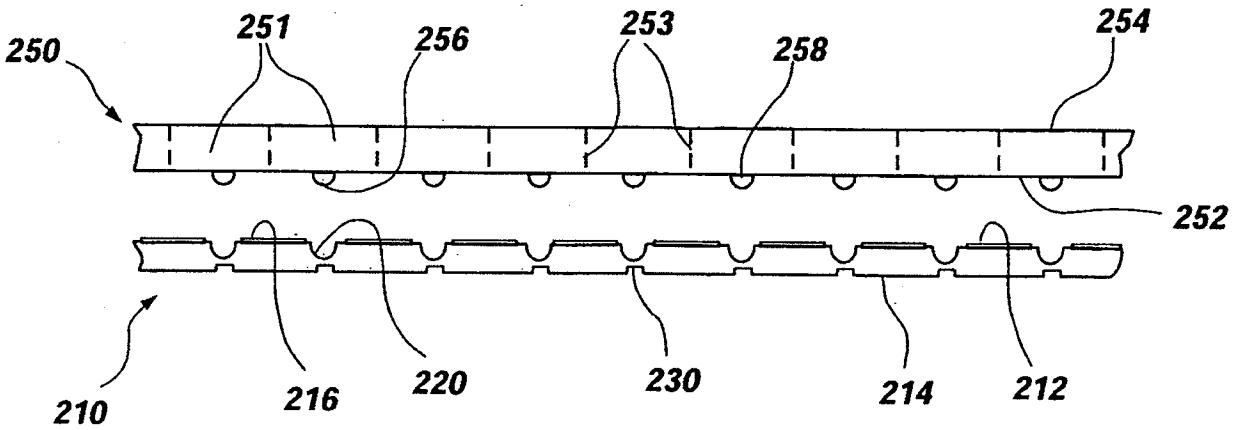


Fig. 24A

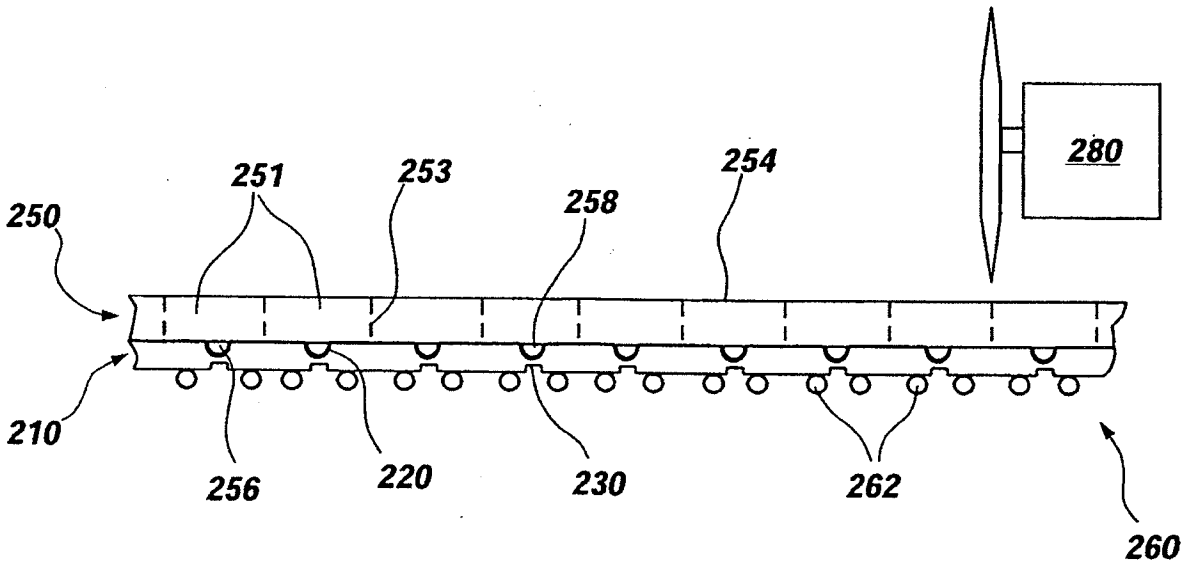


Fig. 24B

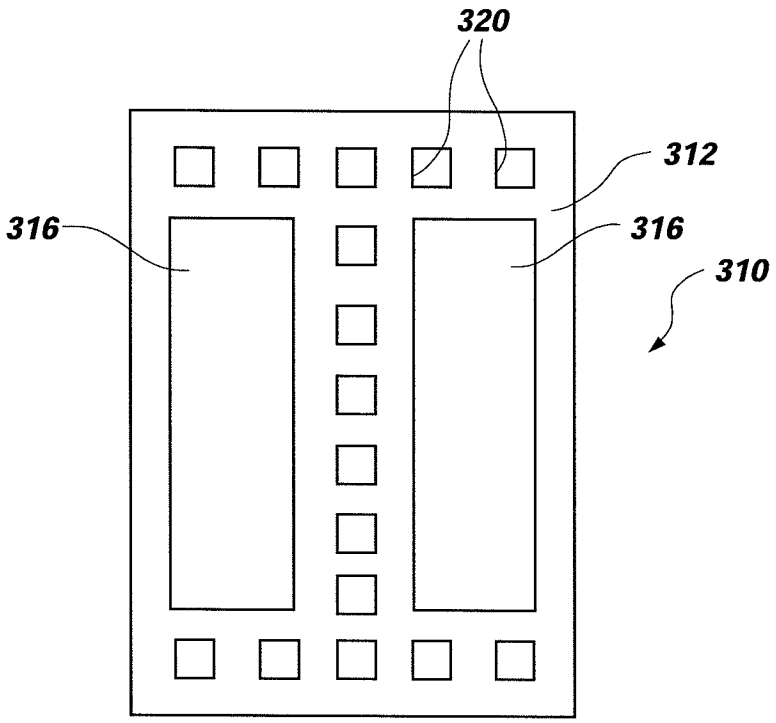


Fig. 25

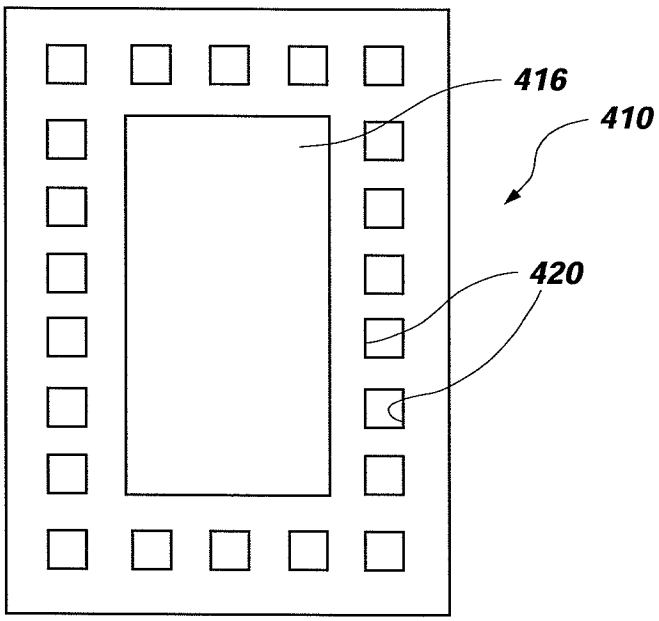


Fig. 26

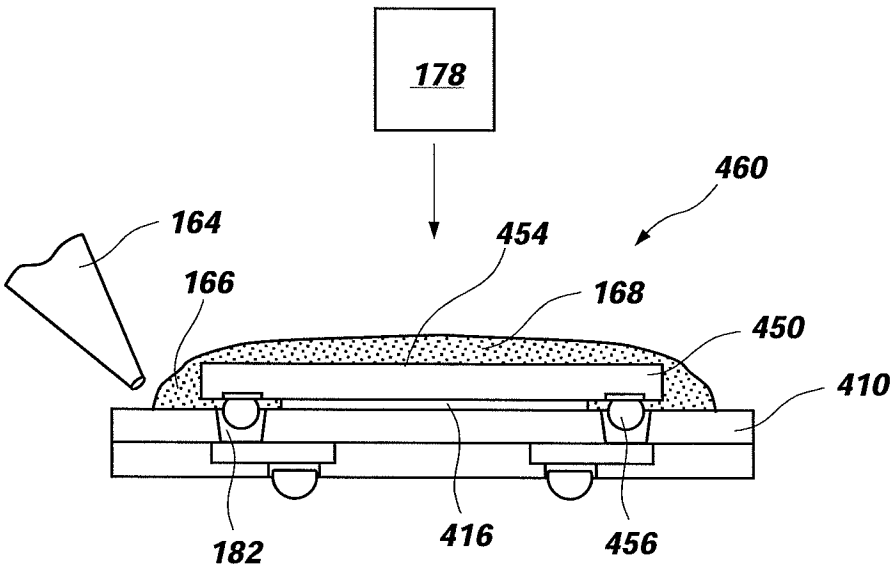

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Fig. 27

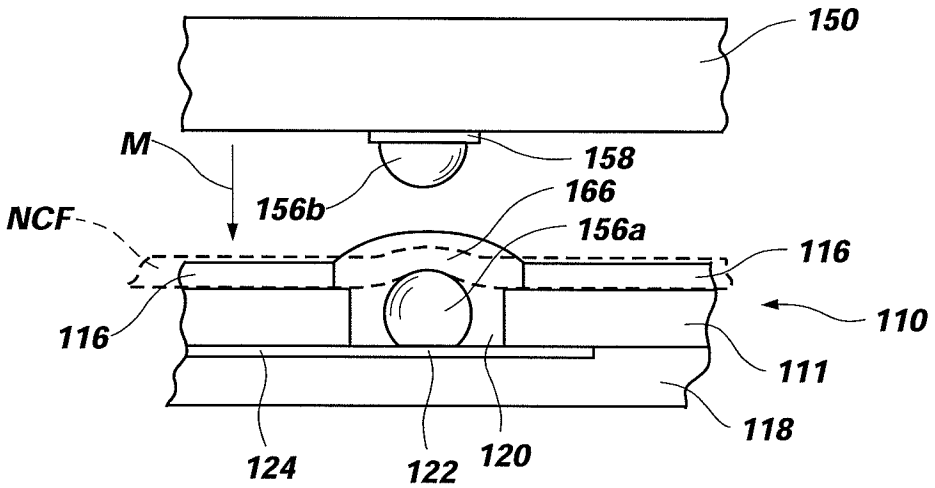

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Fig. 29

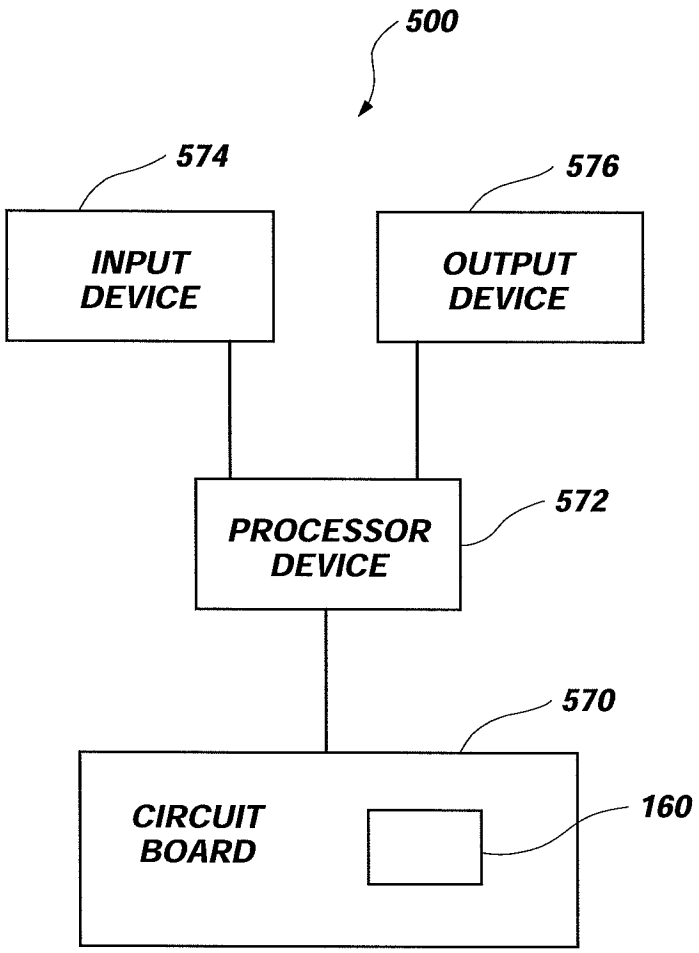

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INPUT DEVICE
OUTPUT DEVICE
PROCESSOR DEVICE
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CIRCUIT BOARD
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Fig. 28