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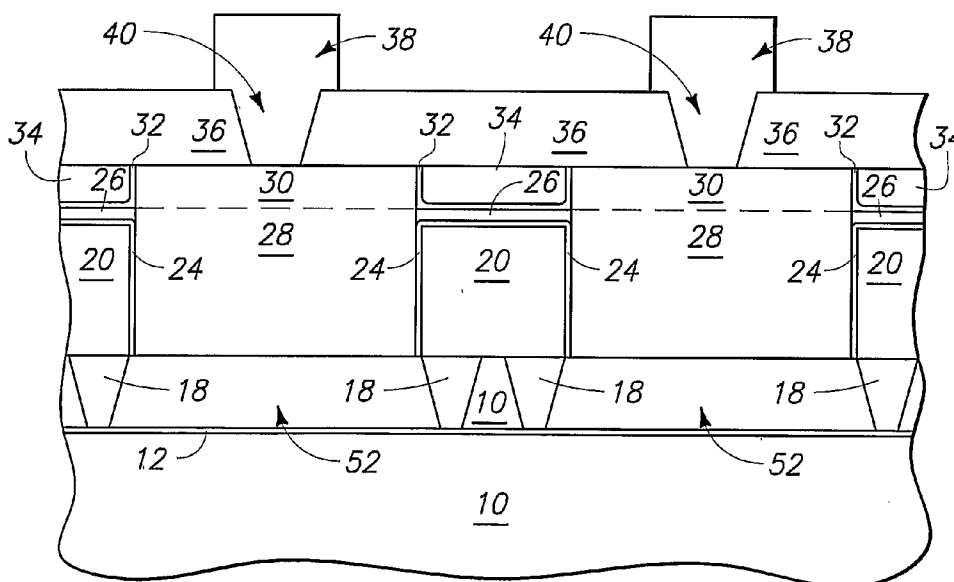
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(54) Title: INTEGRATED CIRCUIT MEMORY CELLS AND METHODS OF FORMING



(57) Abstract: An integrated circuit memory cell includes a combined first capacitor electrode and first transistor source/drain (28), a second capacitor electrode (20), a capacitor dielectric (24) between the first and second electrodes, and a vertical transistor (30) above and including the first source/drain. The second source/drain may be included in a digit line inner conductor (40) connecting a digit line (38) to a transistor channel of the vertical transistor. The channel may include a semiconductive upward extension of the combined first electrode and first source/drain. The memory cell may be included in an array of a plurality of such memory cells wherein the second electrode is a common electrode among the plurality. The memory cell may provide a straight-line conductive path between the first electrode and a digit line, the path extending through the vertical transistor.

WO 2005/064672 A3



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