

CLAIMS

I/we claim,

1. A method of forming a memory device, comprising:
forming an assembly comprising a stack of alternating insulative and conductive levels over control circuitry; the assembly including channel structures extending through the stack; the channel structures having upper and lower regions; the upper regions of the channel structures projecting above the stack; at least some of the lower regions of the channel structures being electrically coupled with bitlines and the control circuitry; and
forming a conductive structure over the upper regions of channel structures and electrically coupled with the channel structures.
2. The method of claim 1 wherein the electrical coupling to the control circuitry is through the bitlines.
3. The method of claim 1 wherein the conductive structure includes metal.
4. The method of claim 1 wherein the conductive structure includes conductively-doped semiconductor material; and further comprising out-diffusing dopant from the conductively-doped semiconductor material into the channel structures.

5. The method of claim 4 further comprising out-diffusing dopant from the conductively-doped semiconductor material into the channel structures.

6. The method of claim 4 wherein an uppermost of the conductive levels within the stack is a source-side select gate level; and wherein the out-diffused dopant extends downwardly to at least said uppermost of the conductive levels.

7. The method of claim 4 wherein the semiconductor material comprises silicon.

8. The method of claim 4 wherein the channel structures comprise a first semiconductor material, and wherein the semiconductor material of the conductive structure is a second semiconductor material.

9. The method of claim 8 wherein the first and second semiconductor materials comprise a same semiconductor composition as one another.

10. The method of claim 8 wherein the first and second semiconductor materials both comprise silicon.

11. The method of claim 8 wherein the first and second semiconductor materials comprise different semiconductor compositions relative to one another.

12. The method of claim 1 wherein the assembly includes memory cells along at least some of the conductive levels.

13. The method of claim 12 wherein the memory cells include charge-storage material.

14. The method of claim 1 further comprising forming an interconnect which extends through the conductive levels and which is coupled with the conductive structure; the forming of the interconnect comprising:

- forming an opening to pass through first and second levels and into a silicon substrate;

- forming an insulative liner within the opening;

- forming conductive pillar material within the opening, the silicon substrate, insulative liner and conductive pillar material together comprising an assembly;

- inverting the assembly;

- removing the silicon substrate and removing some of the insulative liner to expose a region of the conductive pillar material;
- and

- forming the conductive structure to directly contact the exposed region of the conductive pillar material.

15. A method of forming a memory device, comprising:
forming an assembly comprising channel structures extending through a stack of alternating insulative and conductive levels and into a first material under the stack;
inverting the assembly so that the first material is above the stack, and so that first regions of the channel structures are under the stack;
electrically coupling at least some of the first regions with control circuitry;
exposing second regions of the channel structures over the stack, the exposure of the second regions comprising removal of the first material; and
forming conductively-doped semiconductor material adjacent the exposed second regions of the channel structures.

16. The method of claim 15 wherein the first material is monocrystalline silicon of a monocrystalline silicon wafer.

17. The method of claim 15 wherein the electrical coupling to the control circuitry is through bitlines.

18. The method of claim 15 wherein the removing of the at least some of the first material removes all of the first material.

19. The method of claim 15 wherein the assembly includes memory cells along at least some of the conductive levels.

20. The method of claim 19 wherein the memory cells include charge-storage material.

21. The method of claim 20 wherein the charge-storage material is a charge-trapping material.

22. The method of claim 15 further comprising forming a conductive structure over the conductively-doped semiconductor material and at least some of the conductive structure being electrically coupled with the conductively-doped semiconductor material; the conductive structure and the conductively-doped semiconductor material together being a source structure.

23. The method of claim 22 further comprising:
forming an insulative material over the conductively-doped semiconductor material;
forming conductive interconnects to extend through the insulative material to the conductively-doped semiconductor material;
forming the conductive structure over the insulative material; and
wherein the electrical coupling of the conductive structure with the conductively-doped semiconductor material extends through the conductive interconnects.

24. The method of claim 22 further comprising out-diffusing dopant from the conductively-doped semiconductor material into the channel structures.

25. The method of claim 24 wherein an uppermost of the conductive levels within the stack is a source-side select gate level; and wherein the out-diffused dopant extends downwardly to at least said uppermost of the conductive levels.

26. The method of claim 15 wherein the channel structures comprise a first semiconductor material, and wherein the conductively-doped semiconductor material is a second semiconductor material.

27. The method of claim 26 wherein the first semiconductor material comprises silicon.

28. The method of claim 26 wherein the first and second semiconductor materials comprise silicon.

29. A memory device, comprising:
control circuitry;
a stack of alternating insulative and conductive levels over the control circuitry;
channel structures extending through the stack; the channel structures having upper regions and lower regions; the upper regions of the channel structures projecting above the stack and defining at least a portion of an undulating upper topography; at least some of the lower regions of the channel structures being electrically coupled with the control circuitry; and
a conductive source structure over the upper regions of the channel structures; a lower surface of the conductive source structure being conformal to the undulating upper topography and being directly against the upper regions of channel structures.
30. The memory device of claim 29 comprising memory cells along at least some of the conductive levels.
31. The memory device of claim 30 wherein the memory cells include charge-storage material.
32. The memory device of claim 31 wherein the charge-storage material includes charge-trapping material.
33. The memory device of claim 32 wherein the charge-trapping material includes silicon nitride.

34. The memory device of claim 29 wherein the conductive source structure comprises a metal-containing material over a conductively-doped semiconductor material.

35. The memory device of claim 34 wherein the conductively-doped semiconductor material comprises silicon.

36. The memory device of claim 34 wherein the metal-containing material is spaced from the conductively-doped semiconductor material by an insulative region; and wherein conductive interconnects pass through the insulative region to electrically couple the metal-containing material with the conductively-doped semiconductor material.

37. The memory device of claim 29 wherein the control circuitry includes CMOS circuitry.

38. A memory device, comprising:
control circuitry;
a stack of alternating insulative and conductive levels over the control circuitry;
channel structures extending through the stack; the channel structures having first regions vertically offset from second regions; the second regions of the channel structures projecting above the stack; at least some of the first regions of the channel structures being electrically coupled with the control circuitry; and
a conductive source structure over the second regions of the channel structures; the conductive source structure comprising a conductive material adjacent the second regions of channel structures; the second regions of the channel structures penetrating into the conductive material.

39. The memory device of claim 38 wherein the conductive material comprises conductively-doped semiconductor material.

40. The memory device of claim 39 wherein the conductively-doped semiconductor material is conductively-doped silicon.

41. The memory device of claim 39 wherein the conductive source structure includes a metal-containing material extending horizontally along the conductively-doped semiconductor material and electrically coupled with the conductively-doped semiconductor material.

42. The memory device of claim 41 wherein the metal-containing material includes one or both of aluminum and copper.

43. The memory device of claim 41 comprising an insulative material between the metal-containing material and the conductively-doped semiconductor material, and comprising conductive interconnects extending through the insulative material; wherein upper surfaces of the conductive interconnects are directly against the metal-containing material; and wherein lower surfaces of the conductive interconnects are directly against the conductively-doped semiconductor material.

44. The memory device of claim 38 comprising memory cells along at least some of the conductive levels.

45. The memory device of claim 44 wherein the memory cells include charge-storage material.

46. The memory device of claim 45 wherein the charge-storage material includes silicon nitride.

47. The memory device of claim 45 wherein an uppermost of the conductive levels within the stack is a source-side select gate level.