

MAGNETORESISTIVE RANDOM ACCESS MEMORY WITH REDUCED SWITCHING FIELD VARIATION

REFERENCE TO PRIOR APPLICATION

This application has been filed in the United States of America as patent application number 10/648,466 on August 25, 2003.

FIELD OF THE INVENTION

This invention relates to semiconductor memory devices and, more particularly, to the switching characteristics of an array of multi-layer magnetic memory cells.

BACKGROUND OF THE INVENTION

In the past, a variety of magnetic materials and structures have been utilized to form magnetoresistive materials for non-volatile memory elements, read/write heads for disk drives, and other magnetic type applications. Resistance changes due to relative changes in the magnetic states of constituent magnetic regions within these structures allow information to be stored, in the case of memories, or read, in the case of read heads. Memories made of magnetoresistive material, such as Magnetic Random Access Memory (hereinafter referred to as MRAM) has the potential to overcome some of the shortcomings associated within memories currently in production today. Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and Flash are the three dominant types of memories currently in use. Each of these memory devices

uses an electronic charge to store information and each has its own advantages and disadvantages. SRAM has fast read and write speeds, but it is volatile and requires large cell area. DRAM has high density, but it is also volatile and requires a refresh of the storage capacitor every few milliseconds. This requirement increases the complexity of the control electronics. FLASH is the major nonvolatile memory device in use today. FLASH uses charge trapped in a floating oxide layer to store information. Drawbacks to FLASH include high voltage requirements and slow program and erase times. Also, FLASH memory has a poor write endurance of 10^4 - 10^6 cycles before memory failure. In addition, to maintain reasonable data retention, the thickness of the gate oxide has to stay above the threshold that allows electron tunneling, thus restricting FLASH's scaling trends. MRAM has the potential to have the speed performance similar to DRAM without the need for refresh, have improved density performance over SRAM without the volatility, and have improved endurance and write performance over FLASH.

As mentioned above magnetoresistive devices and MRAM in particular rely on resistance changes resulting from changes in the magnetization directions of constituent magnetic layers in the material stack. Typically, MRAM devices comprise a magnetic layer whose magnetization direction is fixed, the fixed layer, and a magnetic layer, the free layer, whose magnetization direction is free to switch between two or more stable directions separated by a spacer layer of an oxide (Tunneling magnetoresistance) or conductor (Giant magnetoresistance). Typical MRAM architectures involve laying out the individual magnetoresistive elements at the intersection of a crosspoint of mutually perpendicular current lines. These lines need not be in contact with the element. Their purpose is mainly to provide the magnetic fields, by having current passed along their length, to switch the magnetization direction of the free layer, within the element. In the absence of these fields, the magnetization direction of the free layer is stable. This is the

procedure by which information is written to the memory. Reading information is typically accomplished by passing a small current through the element and comparing the resistance to a reference resistance.

For the successful operation of an MRAM device, it is required that the magnetic behavior of the free layers of an array of elements be very uniform. This is related to the crosspoint architecture mentioned above. The current lines each provide enough current to produce approximately half of the magnetic field required for the free layer to alter its state, i.e. half the switching field. Magnetic state is defined here as a stable direction of the magnetization of the free layer. The two half fields combine at the point of intersection of the current lines to provide enough field there so that the elements' free layer magnetic state will change. All other bits in the array are exposed to at most approximately half the switching field. The uniformity in the magnetic behavior or the switching field for the array of bits is essential so that the half fields produced do not inadvertently cause an unwanted bit to switch its state and, in addition, that the two half fields combine to switch all the bits in the array.

It would be highly advantageous and is the intention of the current application, therefore, to provide means of decreasing the variation in the switching field bit to bit.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and further and more specific objects and advantages of the instant invention will become readily apparent to those skilled in the art from the following detailed description of a preferred embodiment thereof taken in conjunction with the following drawings:

FIG. 1 is an enlarged, simplified side view of a multi-layer magnetic memory cell, in accordance with the preferred embodiment of the present invention;

FIG. 2 attached is a graph of the relative variation of a magnetic intrinsic anisotropy verses a thickness of a single bulk nickel iron cobalt (NiFeCo) layer;

5 Fig. 3 illustrates the relative variation of the switching field of patterned bits verses a thickness of a single patterned nickel iron cobalt (NiFeCo) layer;

FIG. 4 is a simplified view of a magnetic memory cell used to experimentally measure a magnetic anisotropy and a relative magnetic anisotropy variation of a magnetic layer;

10 FIG. 5 is a graph of a relative magnetic anisotropy variation of the magnetic intrinsic anisotropy illustrated in FIG. 4 versus thickness of a magnetic layer; and

FIG. 6 is a graph of a relative switching variation of the magnetic memory cell illustrated in FIG. 1 for aspect ratios of two and three versus different combinations of material stack.

15 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Turn now to FIG. 1, which illustrates a simplified sectional view of a scalable magnetoresistive tunneling junction memory cell 10 in accordance with the present invention. The scalable magnetoresistive tunneling junction memory cell 10 includes a supporting substrate 12 onto which a seed layer 14 is positioned. Supporting substrate 12 may be, for example, a semiconductor substrate or wafer and semiconductor control devices may then be formed thereon. Seed layer 14 is formed on supporting substrate 12 to aid in the formation and operation of the remaining layers of material. An anti-ferromagnetic layer 16 is then positioned on seed layer 14 and includes, for example,

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alloys of manganese (Mn) and one of Ni, Fe, Pt, Rh or combinations thereof. It will be understood that seed layer 14 is optional and is included in this preferred embodiment for illustrative purposes. Also, the positioning of anti-ferromagnetic layer 16 is for fabrication convenience with many other possible configurations available.

5 A first magnetic region 18 having a resultant magnetic moment vector 20 is positioned on the anti-ferromagnetic layer 16. A nonmagnetic separating layer 22 is placed on first magnetic region 18 and a second magnetic region 24 having a resultant magnetic moment vector 26 is positioned on nonmagnetic separating layer 22. Nonmagnetic separating layer 22 can be a dielectric material which behaves as a tunneling barrier to
10 produce a magnetic tunnel junction that exhibits tunneling magnetoresistance or it may be a conductive material such as copper to produce a layered metallic structure which exhibits giant magnetoresistance. It will be understood that nonmagnetic separating layer 22 can include multiple insulating layers, but is shown as one layer for illustrative purposes.

15 Anti-ferromagnetic layer 16 pins resultant magnetic moment vector 20 unidirectionally along a preferred magnetic axis unless sufficient magnetic field is supplied to overcome the pinning action of layer 16. Generally, anti-ferromagnetic layer 16 is thick enough to insure that spurious signals and normal cell writing signals will not switch resultant magnetic moment vector 20.

20 In the preferred embodiment, fixed magnetic region 18 includes a synthetic anti-ferromagnetic layer material which includes a tri-layer structure of an anti-ferromagnetic coupling spacer layer 28 sandwiched between a ferromagnetic layer 30 and a ferromagnetic layer 32. However, it will be understood that magnetic region 18 can include a synthetic anti-ferromagnetic layer material other than a tri-layer structure and the
25 use of a tri-layer structure in this embodiment is for illustrative purposes only. Further,

magnetic region 18 is a fixed ferromagnetic region, meaning that the magnetic moment vectors of layers 30 and 32 are not free to rotate in the presence of a moderate applied magnetic field and layer 32 is used as the reference layer.

A free magnetic region 24 includes a synthetic anti-ferromagnetic layer material which includes N ferromagnetic layers that are anti-ferromagnetically coupled, wherein N is a integer number greater than or equal to two. In the embodiment shown here for simplicity, N is chosen to be equal to two so that magnetic region includes a tri-layer structure which has an anti-ferromagnetic coupling spacer layer 34 sandwiched between a ferromagnetic layer 36 and a ferromagnetic layer 38. Ferromagnetic layers 36 and 38 each have thicknesses 40 and 42, respectively. Further, anti-ferromagnetic coupling spacer layer 34 has a thickness 44. It will be understood that the synthetic anti-ferromagnetic layered material in magnetic region 24 can include other structures with a different number of ferromagnetic layers and the use of a tri-layer structure in this embodiment is for illustrative purposes only. For example, a five-layer stack of a ferromagnetic layer/anti-ferromagnetic coupling spacer layer/ferromagnetic layer/anti-ferromagnetic coupling spacer layer/ferromagnetic layer could be used, wherein N is equal to three.

Anti-ferromagnetic coupling spacer layers 28 and 34 most often include elements Ru, Os, Re, Cr, Rh, and Cu, or combinations thereof. Further, ferromagnetic layers 30, 32, 36, and 38 most often include alloys of Ni, Fe, Co, or combinations thereof.

Ferromagnetic layers 36 and 38 each have a magnetic moment vector 46 and 48, respectively, that are usually held anti-parallel by coupling of anti-ferromagnetic coupling spacer layer 34. Also, magnetic region 24 has a resultant magnetic moment vector 26. When no magnetic field is applied, resultant magnetic moment vectors 20 and 26 are oriented along a preferred anisotropy easy-axis. Further, magnetic region 24 is a free

ferromagnetic region, meaning that resultant magnetic moment vector 26 is free to rotate in the presence of an applied magnetic field.

While anti-ferromagnetic coupling layers are illustrated between the ferromagnetic layers in magnetic regions 18 and 24, it will be understood that the ferromagnetic layers could be anti-ferromagnetically coupled through other means such as magnetostatic fields or other features. For example, for structures with a high aspect ratio, the ferromagnetic layers are anti-parallel coupled from magnetostatic flux closure. In this case, any nonmagnetic spacer layer that breaks the ferromagnetic exchange between layers will suffice. However, in the preferred embodiment, the adjacent ferromagnetic layers are anti-ferromagnetically coupled by sandwiching anti-ferromagnetic coupling material between each adjacent ferromagnetic layer. One advantage of using a synthetic anti-ferromagnetic layer material is that the anti-parallel coupling of the magnetic moment vectors prevents a vortex from forming at a given thickness where a vortex would be formed if using a single layer.

Further, during fabrication of scalable magnetoresistive tunneling junction memory cell 10, each succeeding layer (i.e. 14, 16, 30, etc.) is deposited or otherwise formed in sequence and each cell may be defined by selective deposition, photolithography processing, etching, etc. in any of the techniques known in the semiconductor industry. During deposition of at least the ferromagnetic layers 36 and 38, a magnetic field is provided to set an easy magnetic axis for these layers (induced anisotropy). This anisotropy axis can also be set subsequent to deposition by annealing in the presence of a magnetic field.

The structure of magnetic region 24 substantially impacts the variation in the switching for an array of MRAM devices. In the preferred embodiment, to minimize the variation in the switching field H_{sw} , the magnetic layer (i.e. layer 11) in magnetic region

24 adjacent to nonmagnetic spacer region 22 is formed to have a thickness greater than layer 38 and in the range of 40 Å to 120 Å. A thicker layer 36 has been found to significantly improve the magnetic properties of layer 36 so that H_{sw} is approximately equal from one MRAM device to another. In general, it has been found that the switching variation of the elements within the array is impacted by the quality of the magnetic material initially deposited on the nonmagnetic separating layer 22. Therefore, the essence of this patent is to optimize the material quality of layer 36, and retain acceptable switching characteristics by making layer 36 part of a SAF structure. As mentioned above SAF structures provide a reduction in the formation of magnetization vortices (where the magnetization direction is not uniaxial but circular) and a way to control the switching field. See United States Patent No. 6,531,723.

A significant degradation in the magnetic quality of magnetic layer 36 is seen starting at thicknesses below approximately 50 Å to 60 Å (See FIG. 2). This can be seen by an increase in the relative variation of the intrinsic material anisotropy normalized to the mean anisotropy. Intrinsic material anisotropy is an energy defining the preferred stable uniaxial magnetization direction. The magnitude of the switching field H_{sw} for an unbalanced free magnetic region is controlled in part by the intrinsic anisotropy (See United States Patent No. 6,531,723), and a larger variation in the intrinsic anisotropy will directly result from the increase in the variation of the magnetic switching field H_{sw} for patterned MRAM devices. Illustrated in FIG. 2 is the relative variation of the intrinsic material anisotropy measured for various thicknesses 40 within a range approximately from 20 Å to 60 Å for magnetic layer 36 deposited in a magnetic field on an aluminum oxide layer 22 and annealed in a magnetic field at 250 °C for 30 minutes. As shown, the relative variation of the intrinsic anisotropy decreases for thicker magnetic layers which

illustrates that magnetic memory cells grown with thicker magnetic layers positioned adjacent to the nonmagnetic spacer region will show improved magnetic properties.

Turn now to FIG. 3 which illustrates a graph of the relative variation of a magnetic switching field H_{sw} for an array of patterned magnetic elements having a single free magnetic layer (i.e. thickness 44 equals zero and thickness 42 equals zero) verses thickness of the layer, the layer being composed of nickel iron cobalt (NiFeCo) grown on an aluminum oxide nonmagnetic spacer layer 22. The size and shape of the elements are aspect ratio 2 ellipse shape with a width of 0.45 micrometers. As can be seen in Fig. 3, there is a minimum in the relative variation of the switching fields within the array beginning at approximately 40Å. Greater than 40Å, the relative variation is constant with thickness because it is dominated by variations in shape anisotropy from bit-to-bit that scale with the increasing moment. Below 40Å there is an increase in the relative variation with decreasing thickness. This behavior is due to the degradation in material quality shown in Figure 2. The poor magnetic properties of the thin magnetic layer directly increases the magnetic switching field variation from one MRAM device to another in the array of MRAM devices. The preferred embodiment addresses these shortcomings by making layer 36 thicker with better material quality while effectively making the whole stack thinner by anti-ferromagnetically coupling layer 38 to 36. The preferred embodiment has the material quality of a thick layer but the shape contribution and lack of vortex formation of a thin layer.

Turn now to FIG. 4 which illustrates a magnetic memory cell 50 used to experimentally measure a magnetic anisotropy and a relative magnetic anisotropy variation of SAF layers 72. In a preferred embodiment, cell 50 includes a conductive layer 52. An insulator layer 54 is positioned on conductive layer 52 and a magnetic layer 56 with a thickness 58 is positioned on insulator layer 54. An anti-ferromagnetic spacer layer

60 with a thickness 62 is positioned on magnetic layer 56 and a magnetic layer 64 with a thickness 66 is positioned on spacer layer 60. Further, an insulator layer 68 is positioned on magnetic layer 64 and a conductive layer 70 is positioned on insulator layer 68.

In this specific example, conductive layers 52 and 70 include tantalum (Ta) and insulator layers 54 and 68 include aluminum oxide (AlO). Further, in this specific example, magnetic layers 56 and 64 include nickel iron (NiFe) and spacer layer 60 includes ruthenium (Ru) wherein magnetic layers 56 and 64 are anti-ferromagnetically coupled. It will be understood that the materials included in layers 52, 54, 56, 60, 64, 68, and 70 of this specific example are chosen for simplicity and ease of discussion to illustrate a measurement result and that other materials could be chosen.

In the preferred embodiment, magnetic layers 56 and 64 are anti-ferromagnetically coupled by spacer layer 60. However, it will be understood that magnetic layers 56 and 64 can be magnetically coupled through other means. Further, cell 50 is illustrated as including two magnetic layers (i.e. layers 56 and 64) for simplicity and ease of discussion to show the experimental measurement.

Turn now to FIG. 5 which illustrates a graph of a relative magnetic anisotropy variation of the SAF structure 72 verses thickness 66 as illustrated in FIG. 4. In this illustration, thickness 66 is varied from approximately 20 Å to 120 Å wherein thickness 58 is approximately 40 Å. As shown, the relative magnetic anisotropy variation is approximately constant as a function of thickness 66. This result indicates that the variation depends substantially on thickness 58 (See FIG. 2) adjacent to tunneling barrier junction 54 and is independent of subsequent layers magnetic grown thereon (i.e. layer 64).

Turn now to FIG. 6 which illustrates the measured improvement of the switching distribution width (sigma) of patterned bits by depositing the thick layers of an unbalanced

SAF first on the tunnel barrier 22. Shown in FIG. 6 is a ratio of a variation for a thin magnetic layer 38 grown on a thick magnetic layer 36 divided by a variation of a thick magnetic layer 38 grown on a thin magnetic layer 36 as a function of the thin layer thickness for an array of aspect ratio 2 and 3 ellipse shaped bits of width 0.45 micrometers. For example, as thinner layer in 24 increases from 15 Å to 45 Å, the ratio of the sigmas from depositing the thick layer first on the tunnel barrier 22 to depositing the thin layer first on 22 increases from approximately 0.6 at 15 Å to 0.95 at 45 Å. The variation within an array can be reduced by as much as 40% by depositing the layer with good material quality on the tunnel barrier 22. This result indicates that for thicknesses below approximately 50Å the variation in the switching field for an array of elements is reduced when the thicker layer is deposited on the tunnel barrier 22. Various changes and modifications to the embodiments herein chosen for purposes of illustration will readily occur to those skilled in the art. For example, thickness is one method for improving the material quality. In addition improved material quality can be obtained from deposition of an amorphous alloy, such as CoFeB alloys, on top of the tunnel barrier. Also material quality can be improved through high temperature anneals and depositions. To the extent that such modifications and variations do not depart from the spirit of the invention, they are intended to be included within the scope thereof which is assessed only by a fair interpretation of the following claims.

Having fully described the invention in such clear and concise terms as to enable those skilled in the art to understand and practice the same, the invention claimed is:

CLAIMS

1. A multi-state, multi-layer magnetic memory device comprising:
a nonmagnetic spacer region with a surface and an opposed surface;
5 a free magnetic region positioned adjacent to the surface of the
nonmagnetic spacer region, the free magnetic region including a plurality of magnetic
layers; and
wherein a free magnetic layer positioned adjacent to the surface of the
nonmagnetic spacer region in the plurality of magnetic layers has improved material
10 quality.
2. A device as claimed in claim 1 wherein the thickness of the magnetic layer
positioned adjacent to the surface of the nonmagnetic spacer region in the plurality of
magnetic layers is in a range approximately from 40 Å to 120 Å and the improved
15 material quality is obtained through increasing the thickness.
3. A device as claimed in claim 1 wherein the magnetic layer positioned
adjacent to the surface of the nonmagnetic spacer region in the plurality of magnetic
layers is of a material having improved growth characteristics on the nonmagnetic
20 spacer.

4. A device as claimed in claim 3 wherein the magnetic layer positioned adjacent to the surface of the nonmagnetic spacer region in the plurality of magnetic layers is an amorphous magnetic alloy.

5 5. A device as claimed in claim 1 wherein the magnetic layer positioned adjacent to the surface of the nonmagnetic spacer region in the plurality of magnetic layers is deposited or annealed at temperatures greater than 100C.

6. A device as claimed in claim 1 wherein the free magnetic region includes at
10 least one layer of an anti-ferromagnetic coupling spacer material.

7. A device as claimed in claim 6 wherein the anti-ferromagnetic coupling spacer material includes at least one of copper (Cu), silver (Ag), gold (Au), chromium (Cr), ruthenium (Ru), rhenium (Re), osmium (Os), titanium (Ti), chromium (Cr), rhodium
15 (Rh), platinum (Pt), palladium (Pd), and alloys thereof.

8. A device as claimed in claim 1 wherein the free magnetic region includes at least one of nickel (Ni), iron (Fe), cobalt (Co), manganese (Mn), combinations thereof, and alloys thereof.

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9. A device as claimed in claim 1 wherein the free magnetic region includes a synthetic anti-ferromagnetic material region including N ferromagnetic layers which are anti-ferromagnetically coupled where N is a whole number greater than or equal to two.

10. A device as claimed in claim 9 wherein each N ferromagnetic layer is anti-ferromagnetically coupled by sandwiching a layer of an anti-ferromagnetic coupling material between each adjacent ferromagnetic layer in the N ferromagnetic layers.

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11. A device as claimed in claim 1 wherein a fixed magnetic region is positioned on the opposed surface of the nonmagnetic spacer region.

12. A device as claimed in claim 1 wherein the nonmagnetic spacer region
10 includes at least one of aluminum oxide (AlO), aluminum nitride (AlN), silicon oxide (SiO), and another dielectric material which form a tunneling barrier with each adjacent region.

13. A device as claimed in claim 1 wherein the nonmagnetic spacer is a
15 conductive material including at least one of copper (Cu), chromium (Cr), silver (Ag), and gold (Au).

14. A device as claimed in claim 9 wherein the one ferromagnetic layer of the synthetic anti-ferromagnetic material region that is positioned adjacent to the surface of
20 the nonmagnetic spacer is at least as thick as any of the other N ferromagnetic layers which comprise the synthetic anti-ferromagnetic material region.

15. A plurality of magnetic memory devices with a magnetic switching field and a magnetic switching field variation, each device comprising:

- a nonmagnetic spacer region with a surface and an opposed surface; and
- a free magnetic region, the free magnetic region being positioned on the

5 surface of the nonmagnetic spacer region, the free magnetic region includes a first magnetic layer with a thickness positioned adjacent to the nonmagnetic spacer region and a second magnetic layer with a thickness wherein the first and second magnetic layers are separated by a spacer region, wherein the thickness of the first magnetic layer is substantially greater than the thickness of the second magnetic layer, the thickness of

10 the first magnetic layer being chosen to obtain a desired magnetic switching variation.

16. A device as claimed in claim 15 wherein the thickness of the first magnetic layer is in a range approximately from 40 Å to 120 Å for each magnetic memory device in the plurality of magnetic memory devices.

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17. A device as claimed in claim 15 wherein the anti-ferromagnetic spacer region includes an anti-ferromagnetic coupling spacer material.

18. A device as claimed in claim 17 wherein the anti-ferromagnetic coupling

20 spacer material includes at least one of copper (Cu), silver (Ag), gold (Au), chromium (Cr), ruthenium (Ru), rhenium (Re), osmium (Os), titanium (Ti), chromium (Cr), rhodium (Rh), platinum (Pt), palladium (Pd), and alloys thereof.

19. A device as claimed in claim 15 wherein the thickness of the first magnetic layer is in a range approximately from a factor of one and one-half times the thickness of the second magnetic layer to a factor of three times the thickness of the second magnetic layer.

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20. A device as claimed in claim 15 wherein a fixed magnetic region is positioned on the opposed surface of the nonmagnetic spacer region.

21. A device as claimed in claim 20 wherein the nonmagnetic spacer region includes at least one of aluminum oxide (AlO), aluminum nitride (AlN), silicon oxide (SiO), and another suitable dielectric material which forms a tunneling barrier with each adjacent region.

22. A device as claimed in claim 20 wherein the nonmagnetic spacer is a conductive material including at least one of copper (Cu), chromium (Cr), silver (Ag), and gold (Au).

23. A method of fabricating a plurality of magnetic memory devices with a magnetic switching field variation, the method of fabricating each magnetic memory device in the plurality of magnetic memory devices comprising the steps of:

5 providing a nonmagnetic spacer region with a surface and an opposed surface; and

 positioning a free magnetic region, the free magnetic region being positioned on the surface of the nonmagnetic spacer region wherein the free magnetic region includes a plurality of magnetic layers and wherein a magnetic layer in the
10 plurality of magnetic layers positioned adjacent to the nonmagnetic spacer region has a thickness substantially greater than a thickness of the magnetic layers subsequently grown thereon to obtain a desired magnetic switching field variation.

24. A method as claimed in claim 23 wherein the thickness of the magnetic
15 layer positioned adjacent to the nonmagnetic spacer region in the plurality of magnetic layers is in a range approximately from 40 Å to 120 Å for each magnetic memory device in the plurality of magnetic memory devices.

25. A method as claimed in claim 23 herein the free magnetic region
20 includes at least one layer of an anti-ferromagnetic coupling spacer material.

26. A method as claimed in claim 23 wherein at least one layer of the anti-ferromagnetic coupling spacer material includes at least one of copper (Cu), silver (Ag), gold (Au), chromium (Cr), ruthenium (Ru), rhenium (Re), osmium (Os), titanium (Ti),
5 chromium (Cr), rhodium (Rh), platinum (Pt), palladium (Pd), and alloys thereof.

27. A method as claimed in claim 23 wherein the free magnetic region includes at least one of nickel (Ni), iron (Fe), cobalt (Co), and alloys thereof.

10 28. A method as claimed in claim 23 wherein the free magnetic region includes a synthetic anti-ferromagnetic material layer that includes N ferromagnetic layers which are anti-ferromagnetically coupled, where N is a whole number greater than or equal to two.

15 29. A method as claimed in claim 28 wherein each N ferromagnetic layer is anti-ferromagnetically coupled by sandwiching a layer of an anti-ferromagnetic coupling material between each adjacent ferromagnetic layer in the N ferromagnetic layers.

20 30. A method as claimed in claim 23 further including the step of providing a fixed magnetic region positioned adjacent to the opposed surface of the nonmagnetic spacer region.

31. A method as claimed in claim 23 wherein the nonmagnetic spacer region includes at least one of aluminum oxide (AlO), aluminum nitride (AlN), silicon oxide (SiO), and another suitable dielectric material which forms a tunneling barrier with each adjacent region.

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32. A method as claimed in claim 23 wherein the nonmagnetic spacer is a conductive material including at least one of copper (Cu), chromium (Cr), silver (Ag), and gold (Au).