supply voltage $V_{Hsupply}$ and low supply voltage $V_{Lsupply}$ are usually then at their high and low voltage level, respectively. A precharge control signal ϕ_{PCH} is applied to the gates of said precharge transistors T61, T62.

The sense amplifier further comprises an equalization transistor T50 having its source/drain terminals respectively coupled to one of bit lines BL, /BL and having its gate controlled by an equalization control signal ϕ_{EQL}. The equalization transistor T50 of the circuit illustrated in Fig. 1 is an N-MOS type transistor.

The sense amplifier further comprises two dedicated pass-gate transistors T71, T72, the gates of which are controlled by a decoding control signal Y_{DEC}. Each of the pass-gate transistors T71, T72 connects one of the bit lines BL, /BL to a global bit line IO, /IO, also called in-out line. The pass-gate transistors T71, T72 are used to transfer data between the bit lines BL, /BL and the global bit lines IO, /IO.

Although sense amplifiers are technically necessary, from an economical point of view the sense amplifiers can be considered as service circuits of the memory array and therefore as overhead that increases the area of the entire circuit and thus also its cost of fabrication.

Therefore, continuous efforts are made to minimize the area consumption of such sense amplifiers.

SHORT DESCRIPTION OF THE INVENTION

A~~The object of the invention is to propose a simplified and robust memory sense amplifier. For this purpose, the invention proposes,~~ according to a first aspect of the present invention, there is provided a differential sense amplifier for sensing data stored in a plurality of memory cells of a memory cell array, including:

- a first CMOS inverter having an output connected to a first bit line and an input connected to a second bit line complementary to the first bit line,
- a second CMOS inverter having an output connected to the second bit line and an input connected to the first bit line,

each CMOS inverter comprising :

- a pull-up transistor having a drain and a source, and
- a pull-down transistor having a drain and a source,

the pull-up transistor and the pull-down transistor of each CMOS inverter having a common drain,

wherein the sources of the pull-down transistors are electrically coupled and connected to a pull-down voltage source, without an intermediate transistor between the sources of the pull-down transistors and the pull-down voltage

source, or the sources of the pull-up transistors are electrically coupled and connected to a pull-up voltage source, without an intermediate transistor between the sources of the pull-up transistors and the pull-up voltage source, and wherein.

~~Other preferred, although non limitative, aspects of this sense amplifier are as follows:~~

- the pull-up and the pull-down transistors are multigate transistors having at least a first control gate and a second control gate, and wherein
    - the second control gates of the pull-up transistors are driven by a pull-up second control signal,
    - the second control gates of the pull-down transistors are driven by a pull-down second control signal.;

According to example embodiments:

- the differential sense amplifier is made on a semiconductor-on-insulator substrate comprising a thin layer of semiconducting material separated from a base substrate by an insulating layer, and wherein the second control gates are back control gates formed in the base substrate below the insulating layer; or
- the transistors are FinFET devices with independent double gates;
- the sense amplifier further comprises an equalization transistor having a source and a drain respectively coupled to one of the first and second bit lines;
- the equalization transistor is a multigate transistor having at least a first control gate and a second control gate connected together;
- the equalization transistor is a P-MOS type transistor physically arranged between the pull-up transistors;
- the sense amplifier has a pair of precharge transistors arranged to be respectively coupled to said first and second bit lines so as to precharge said first and second bit lines to a precharge voltage, wherein said precharge transistors are constituted by the pull-up transistors or by the pull-down transistors;
- the sense amplifier has a pair of pass-gate transistors arranged to connect said first and second bit lines to a first and a second global bit lines, respectively, so as to transfer data between the first and the second bit lines and the first and the second global bit lines, respectively, wherein
    - the pass-gate transistors are constituted by the pull-up transistors, and
    - the sources of the pull-down transistors are electrically coupled and connected to a pull-down voltage source, without an

intermediate transistor between the sources of the pull-down transistors and the pull-down voltage source; or

- the sense amplifier has a pair of pass-gate transistors arranged to connect said first and second bit lines to a first and a second global bit lines, respectively, so as to transfer data between the first and the second bit lines and the first and the second global bit lines, respectively, wherein
    - the pass-gate transistors are constituted by the pull-down transistors and
    - the sources of the pull-up transistors are electrically coupled and connected to a pull-up voltage source, without an intermediate transistor between the sources of the pull-up transistors and the pull-up voltage source;
- the sense amplifier further comprises a pair of precharge transistors wherein the precharge transistors are multigate transistors having at least a first control gate and a second control gate connected together;
- the sense amplifier further comprises a pair of pass gate transistors wherein the precharge transistors are multigate transistors having at least a first control gate and a second control gate connected together.

According to a second aspect, the invention relates to a method for controlling a sense amplifier according to the first aspect of the invention to perform operations for pre-charging the bit lines, sensing and writing-back data stored in a plurality of memory cells of a memory cell array, wherein to modify the operation performed by the differential sense amplifier, the pull-up second control signal and/or the pull-down second control signal are modified.

P~~O~~ther ~~p~~referred, although non limitative, embodiments~~aspects~~ of the method are as follows:

- during a precharge operation, a low pull-up second control signal is applied to the second control gates of the pull-up transistors so that the pull-up transistors are conducting and a low pull-down second control signal is applied to the second control gates of the pull-down transistors so that the pull-down transistors are not conducting; or
- during a precharge operation, a high pull-up second control signal is applied to the second control gates of the pull-up transistors so that the pull-up transistors are not conducting and a high pull-down second control signal is applied to the

CLAIMS

1. A differential sense amplifier for sensing data stored in a plurality of memory cells ~~(C)~~ of a memory cell array, including:

- a first CMOS inverter having an output connected to a first bit line ~~(BL)~~ and an input connected to a second bit line ~~(/BL)~~ complementary to the first bit line,
- a second CMOS inverter having an output connected to the second bit line ~~(/BL)~~ and an input connected to the first bit line ~~(BL)~~,

each CMOS inverter comprising :

- a pull-up transistor ~~(M21, M22)~~ having a drain and a source, and
- a pull-down transistor ~~(M31, M32)~~ having a drain and a source,

the pull-up transistor ~~(M21, M22)~~ and the pull-down transistor ~~(M31, M32)~~ of each CMOS inverter having a common drain,

characterised in that

the sources of the pull-down transistors ~~(M31, M32)~~ are electrically coupled and connected to a pull-down voltage source, without an intermediate transistor between the sources of the pull-down transistors ~~(M31, M32)~~ and the pull-down voltage source, or the sources of the pull-up transistors ~~(M21, M22)~~ are electrically coupled and connected to a pull-up voltage source, without an intermediate transistor between the sources of the pull-up transistors ~~(M21, M22)~~ and the pull-up voltage source ; and

wherein the pull-up ~~(M21, M22)~~ and the pull-down ~~(M31, M32)~~ transistors are multigate transistors having at least a first control gate and a second control gate, and wherein

- the second control gates of the pull-up transistors ~~(M21, M22)~~ are driven by a pull-up second control signal ~~(ϕ_{PBG})~~,
- the second control gates of the pull-down transistors ~~(M31, M32)~~ are driven by a pull-down second control signal ~~(ϕ_{NBG})~~.

2. The differential sense amplifier according to claim 1, wherein the differential sense amplifier is made on a semiconductor-on-insulator substrate comprising a thin layer of semiconducting material separated from a base substrate by an insulating layer, and wherein the second control gates are back control gates formed in the base substrate below the insulating layer.

3. The differential sense amplifier according to claim 1, wherein the transistors are FinFET devices with independent double gates.

4. The differential sense amplifier according to any one of claims 1 to 3, further comprising an equalization transistor ~~(M50)~~ having a source and a drain respectively coupled to one of the first and second bit lines ~~(BL, /BL)~~.

5. The differential sense amplifier according to claim 4, wherein the equalization transistor ~~(M50)~~ is a multigate transistor having at least a first control gate and a second control gate connected together.

6. The differential sense amplifier according any one of claims 4 to 5, wherein the equalization transistor ~~(M50)~~ is a P-MOS type transistor physically arranged between the pull-up transistors ~~(M21, M22)~~.

7. The differential sense amplifier according to any one of claims 1 to 6, having a pair of precharge transistors arranged to be respectively coupled to said first and second bit lines ~~(BL, /BL)~~, so as to precharge said first and second bit lines ~~(BL, /BL)~~ to a precharge voltage, wherein said precharge transistors are constituted by the pull-up transistors ~~(M21, M22)~~ or by the pull-down transistors ~~(M31, M32)~~.

8. The differential sense amplifier according to any one of claims 1 to 7, having a pair of pass-gate transistors arranged to connect said first and second bit lines ~~(BL, /BL)~~ to a first and a second global bit lines ~~(IO, /IO)~~, so as to transfer data between the first and the second bit lines ~~(BL, /BL)~~ and the first and the second global bit lines ~~(IO, /IO)~~, respectively, wherein

- the pass-gate transistors are constituted by the pull-up transistors ~~(M21, M22)~~ and
- the sources of the pull-down transistors ~~(M31, M32)~~ are electrically coupled and connected to a pull-down voltage source, without an intermediate transistor between the sources of the pulldown transistors ~~(M31, M32)~~ and the pull-down voltage source.

9. The differential sense amplifier according to any one of claims 1 to 7, having a pair of pass-gate transistors arranged to connect said first and second bit lines

~~(BL, /BL)~~ to a first and a second global bit lines ~~(IO, /IO)~~, so as to transfer data between the first and the second bit lines ~~(BL, /BL)~~ and the first and the second global bit lines ~~(IO, /IO)~~, respectively, wherein

- the pass-gate transistors are constituted by the pull-down transistors ~~(M31, M32)~~ and
- the sources of the pull-up transistors ~~(M21, M22)~~ are electrically coupled and connected to a pull-up voltage source, without an intermediate transistor between the sources of the pullup transistors ~~(M21, M22)~~ and the pull-up voltage source.

10. The differential sense amplifier according to any one of claims 1 to 6 further comprising a pair of precharge transistors ~~(M61, M62)~~ wherein the precharge transistors ~~(M61, M62)~~ are multigate transistors having at least a first control gate and a second control gate connected together.

11. The differential sense amplifier according to any one of claims 1 to 7 further comprising a pair of pass gate transistors ~~(M71, M72)~~ wherein the precharge transistors ~~(M71, M72)~~ are multigate transistors having at least a first control gate and a second control gate connected together.

12. A method for controlling a differential sense amplifier according to any one of claims 1 to 9 to perform operations for pre-charging the bit lines ~~(BL, /BL)~~, sensing and writing-back data stored in a plurality of memory cells ~~(C)~~ of a memory cell array

wherein to modify the operation performed by the differential sense amplifier, the pull-up second control signal ~~(ϕ_{PBG})~~ and/or the pull-down second control signal ~~(ϕ_{NBG})~~ are modified.

13. The method according to claim 12, wherein during a precharge operation, a low pull-up second control signal ~~(ϕ_{PBG})~~ is applied to the second control gates of the pull-up transistors ~~(M21, M22)~~ so that the pullup transistors ~~(M21, M22)~~ are conducting and a low pull-down second control signal ~~(ϕ_{NBG})~~ is applied to the second control gates of the pull-down transistors ~~(M31, M32)~~ so that the pull-down transistors ~~(M31, M32)~~ are not conducting.

14. The method according to claim 12, wherein during a precharge operation, a high pull-up second control signal (ϕ_{PBG}) is applied to the second control gates of the pull-up transistors (M21, M22) so that the pull-up transistors (M21, M22) are not conducting and a high pull-down second control signal (ϕ_{NBG}) is applied to the second control gates of the pull-down transistors (M31, M32) so that the pull-down transistors (M31, M32) are conducting.

15. The method according to any one of claims 12 to 14, wherein during a sensing operation, a high pull-down second control signal (ϕ_{NBG}) is applied to the second control gates of the pull-down transistors (M31, M32) so that the pull-down transistors (M31, M32) are conducting and a high pull-up second control signal (ϕ_{PBG}) is applied to the second control gates of the pull-up transistors (M21, M22) so that the pull-up transistors (M21, M22) are not conducting.

16. The method according to any one of claims 12 to 14, wherein during a sensing operation, a low pull-down second control signal (ϕ_{NBG}) is applied to the second control gates of the pull-down transistors (M31, M32) so that the pull-down transistors (M31, M32) are not conducting and a low pull-up second control signal (ϕ_{PBG}) is applied to the second control gates of the pull-up transistors (M21, M22) so that the pull-up transistors (M21, M22) are conducting.

17. The method according to any one of claims 12 to 16, wherein during a write back operation, a low pull-up second control signal (ϕ_{PBG}) is applied to the second control gates of the pull-up transistors (M21, M22) so that the pull-up transistors (M21, M22) are conducting and a high pull-down second control signal (ϕ_{NBG}) is applied to the second control gates of the pull-down transistors (M31, M32) so that the pulldown transistors (M31, M32) are conducting.

18. A method for controlling a differential sense amplifier according to claim 8 to perform a read operation, wherein a high pull-down second control signal (ϕ_{NBG}) is applied to the second control gates of the pull-down transistors (M31, M32) so as to turn the pull-down transistors (M31, M32) into depletion mode.

19. A method for controlling a differential sense amplifier according to claim 9 to perform a read operation, wherein a low pull-up second control signal (ϕ_{PBG}) is

applied to the second control gates of the pull-up transistors ~~(M21, M22)~~ so as to turn the pull-up transistors ~~(M21, M22)~~ into depletion mode.

20. A semiconductor memory ~~(120)~~ incorporating a memory cell array ~~(122)~~ characterized in that it comprises at least one differential sense amplifier according to any one of the claims 1 to 11.