ABSTRACT

WAFER LEVEL INTEGRATION MODULE WITH INTERCONNECTS

A method and apparatus for manufacturing an integrated circuit (IC) device 90 is disclosed. A wafer 10 is first provided having a first or top surface and a second or bottom surface. The wafer may be a blank polished or unpolished silicon wafer or the like. High aspect ratio micro-structures 16 that are specifically designed to provide a die level interconnect configuration and mapping, are provided on the first blank surface 12 of the wafer. The wafer with pre-formed conductive interconnect microstructures 16 are further processed for device fabrication, for example, at the wafer fabrication facilities. Once the front side 12 devices are fabricated, the silicon material 20 is then removed from a second side 14 of the device wafer 10, opposite the first side, to expose the high temperature conductive interconnect microstructures 16. Contacts are formed on the second side of the device wafer using conductive metal. These contacts are electrically connected to the interior of the microstructures and thereby electrically connect with the functional device 26. The dies 90(1),90(2) are separated along the separation zones 88 between the dies to produce individualized functional and packaged dies, each of which serves as a fully packaged IC device 90.

FIG. 9