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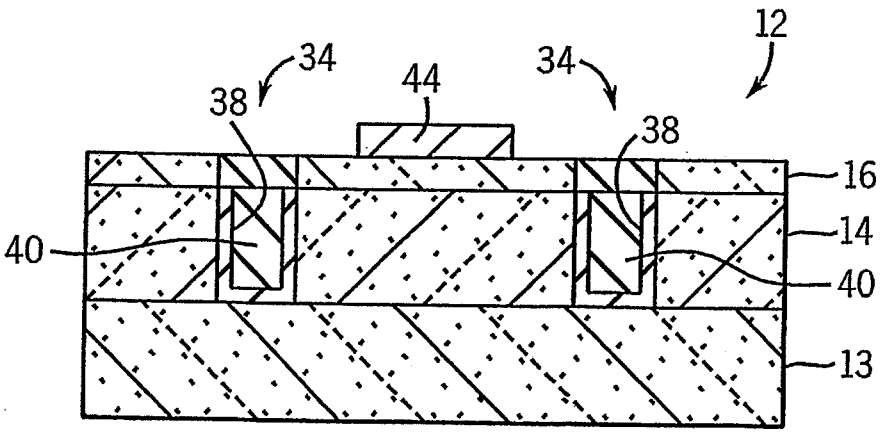
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(54) Title: SHALLOW TRENCH ISOLATION FOR STRAINED SILICON PROCESSES



(57) Abstract: A method of manufacturing an integrated circuit (IC) utilizes a shallow trench isolation (STI) technique. The shallow trench isolation technique is used in strained silicon (SMOS) process. The liner for the trench is formed from a semiconductor or metal layer which is deposited in a low temperature process which reduces germanium outgassing. The low temperature process can be a CVD process.

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