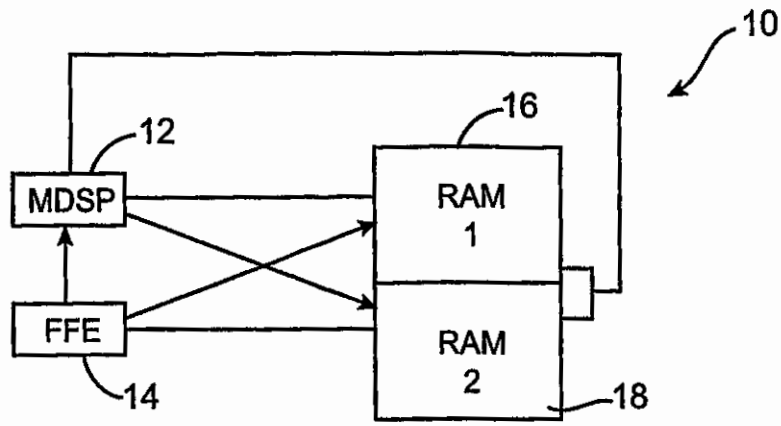


FIG. 1
(PRIOR ART)

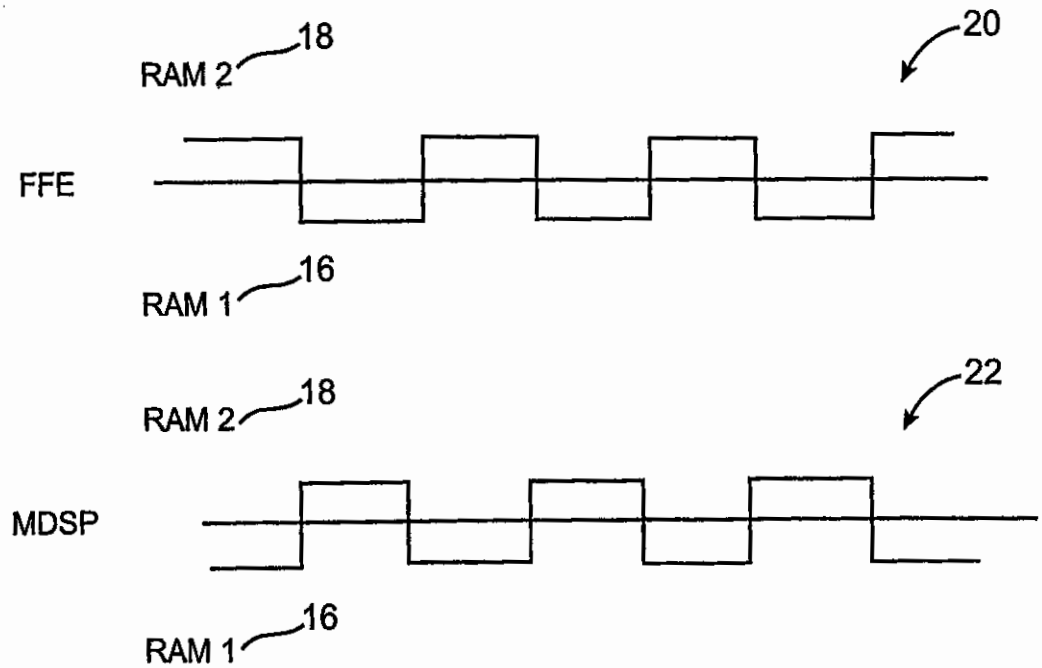


FIG. 2
(PRIOR ART)

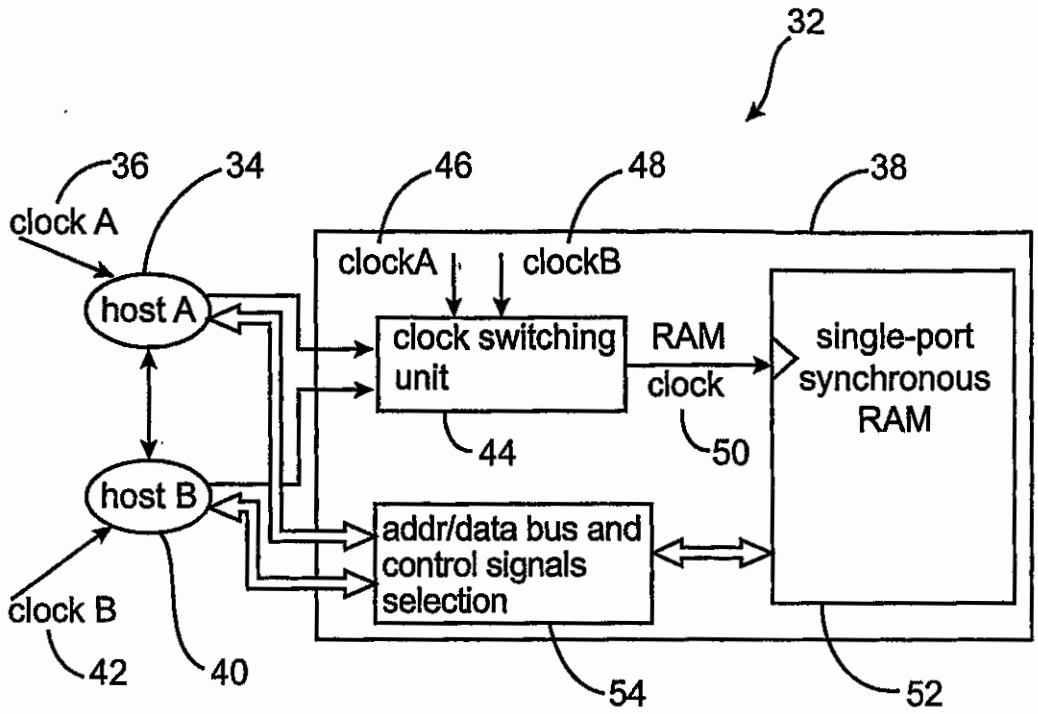

32
36
34
46
48
38
clock A
clockA
clockB
host A
clock switching unit
RAM clock
single-port synchronous RAM
44
50
host B
addr/data bus and control signals selection
clock B
42
40
54
52

FIG. 3

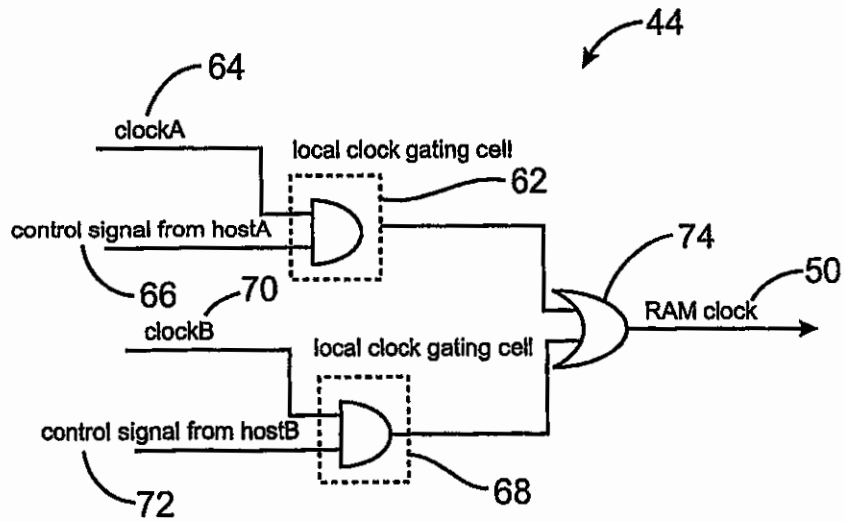

44
64
clockA
local clock gating cell
62
control signal from hostA
74
50
66
70
RAM clock
clockB
local clock gating cell
control signal from hostB
72
68

FIG. 4

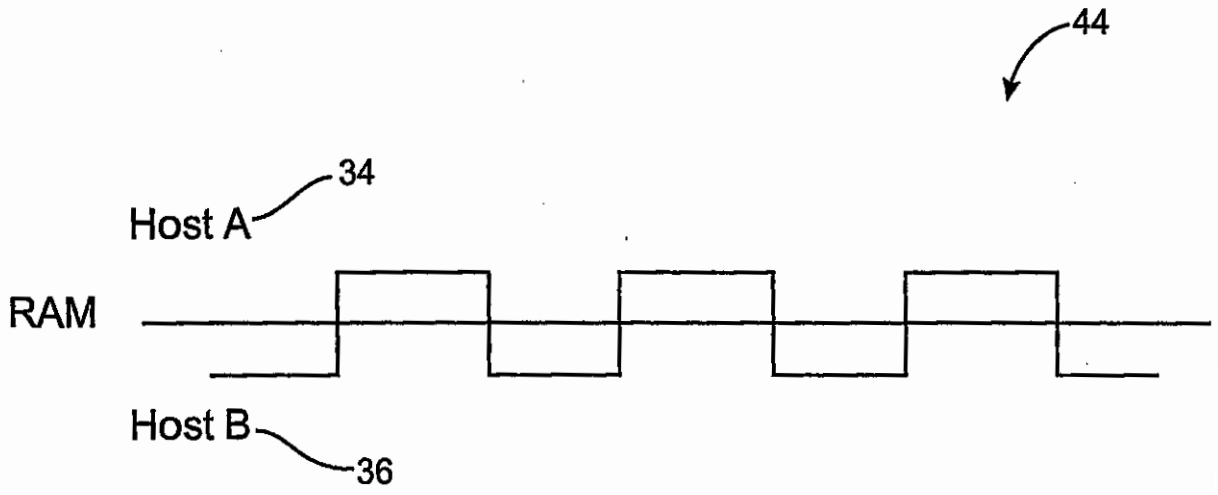


FIG. 5

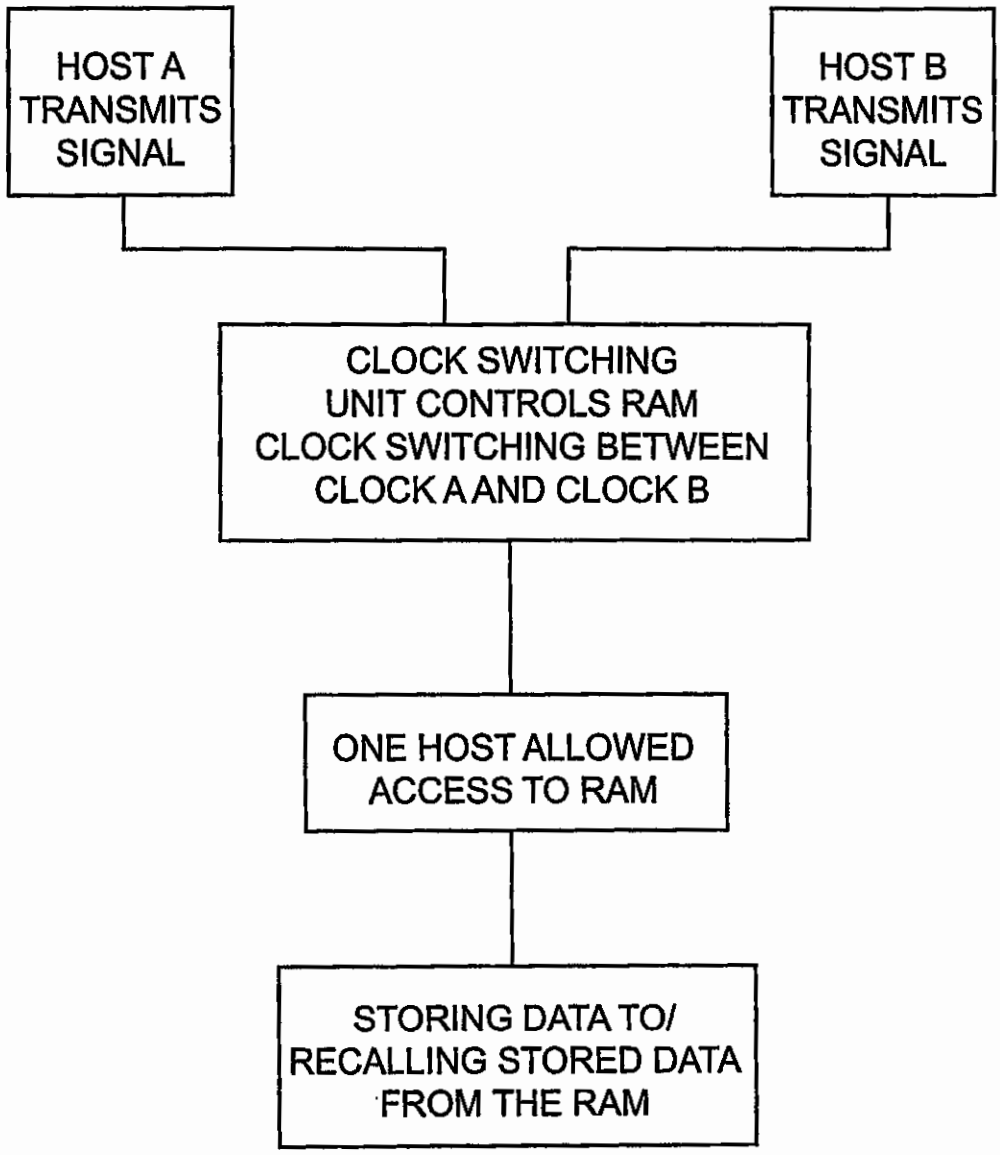

HOST A TRANSMITS SIGNAL
HOST B TRANSMITS SIGNAL
CLOCK SWITCHING UNIT CONTROLS RAM CLOCK SWITCHING BETWEEN CLOCK A AND CLOCK B
ONE HOST ALLOWED ACCESS TO RAM
STORING DATA TO/ RECALLING STORED DATA FROM THE RAM

FIG. 6