ABSTRACT

DUAL GATE AND DOUBLE POLY CAPACITOR ANALOG PROCESS INTEGRATION

A method for integrating the dual gate and double poly capacitor processes to fabricate an analog capacitor integrated circuit device is described. An isolation region is provided separating a first active area from a second active area in a semiconductor substrate. A first gate oxide layer is formed overlying the semiconductor substrate in both active areas. A first polysilicon layer is deposited overlying the first gate oxide layer and the isolation region. An capacitor dielectric layer comprising an oxide layer and a nitride layer is deposited overlying the first polysilicon layer. The capacitor dielectric layer and first polysilicon layer are etched away where they are not covered by a mask to form a first polysilicon gate electrode in the first area and a polysilicon capacitor bottom plate and overlying capacitor dielectric overlying the isolation region. The first gate oxide layer is removed in the second area and a thinner second gate oxide layer is formed in the second area. A second polysilicon layer is deposited overlying the second gate oxide layer, bottom capacitor plate and capacitor dielectric, and the first polysilicon gate electrode. The second polysilicon layer is etched away where it is not covered by a mask to form a second polysilicon gate electrode in the second area and to form a top capacitor plate overlying the bottom capacitor plate having the capacitor dielectric layer therebetween.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)