# A METHOD AND APPARATUS FOR DETECTING AND CONCEALING DATA ERRORS IN STORED DIGITAL DATA

The present invention relates to a method and apparatus for using less reliable memory devices for temporary storage of multibit digital data.

It is often necessary to temporarily store multibit digital data during processing of that data. Memory devices are used for such storage. In general, it is imperative that the data retrieved from such memory devices be an exact replica of the data previously stored. However, in some applications, while it is highly desirable that the retrieved data be a replica of the previously stored data, it is not imperative.

One example of such an application is the processing of audio data in digital form, such as in video camcorders, tapeless telephone answering machines or tapeless audio recorders. This application does not require the absolute fidelity which, for example, a computer storage device requires. In such devices, an analog audio signal is represented by a sequence of multibit digital samples, each having a binary value representing the value of the corresponding analog audio signal. Such samples may, for example, be produced by an analogtodigital converter coupled to an analog audio signal source, or by a digital CD player. During the processing of this audio signal, the series of digital samples representing the audio signal is stored in a memory device, and later retrieved for subsequent processing.

In the applications described above, which do not require absolute fidelity of retrieved data to the previously stored data, memory devices which are not perfect, termed audio read/write memory (ARAM) devices, may be used. These lessthanperfect memory devices are less expensive than perfect memory devices. Because some infidelity in the retrieved samples is permissible, the use of such memory devices will allow for less expensive audio equipment without a noticeable degradation in performance. Prior such systems provided no handling for errors caused by data storage and retrieval errors.

However, this resulted in seriously degraded performance when an error occurred. It is desirable that some way of handling errors resulting from the use of such memory devices be provided.

In accordance with principles of the present invention, a method and apparatus detects and conceals errors in stored digital samples. A multibit digital input sample is received and an error detecting code corresponding to that input sample, and having a predetermined number of bits, is calculated. Then a multibit digital storage sample is generated by substituting the error detecting code for the predetermined number of bits of the input sample. The storage sample is then stored in a memory device. A previously stored sample is retrieved from the memory device and is analyzed to detect whether an error has occurred. If an error is detected, a substitute sample which conceals the error via some means, such as interpolation is produced for the retrieved sample, otherwise the retrieved sample is produced.

Apparatus incorporating this invention may use less than perfect memory devices, such as ARAMs, for storage of digital samples for which absolute fidelity is not required. This results in a lower costs, while not noticeably degrading the performance for such systems.

In the drawing:

Fig. 1 is a block diagram of apparatus according to the present invention for writing data into a memory device;

Fig. 2 is a block diagram of apparatus according to the present invention for reading previously written data from the memory device;

Fig. 3 is a more detailed block diagram of a portion of the read apparatus illustrated in Fig. 2; and

Fig. 4 and Fig. 5 are waveform diagrams useful in understanding the operation of the portion of the read apparatus illustrated in Fig. 3.

Fig. 1 is a block diagram of apparatus according to the present invention for writing data into a memory device. In Fig. 1, a data source 10 generates, in a known manner, a stream of

successive multibit digital samples, each consisting of a plurality of bits arranged in a known manner from a least significant bit (LSB) to a most significant bit (MSB). The digital samples are produced, successively, at an output terminal of the data source 10. The output terminal of the data source 10, with the exception of the LSB, is coupled to respective input terminals of an error detecting code (EDC) generator 30 and a memory device 20. An output terminal from the EDC generator 30 is supplied to the LSB input terminal of the memory device 20 input terminal, in place of the LSB from the digital data source.

The EDC generator 30 may be any one of known generators of one of more error detecting code bits, and in the illustrated embodiment is a parity generator 30. In general, the number of error detecting code bits generated by the EDC generator 30 are substituted for the same number of LSBs in the word from data source 10 before being stored in the memory device 20. The remainder of the application will refer to the parity generator 30 and single parity bit, but one skilled in the art will understand that any one of the known error detecting code generators, generating any number of error detecting code bits, may be used in its place.

In operation, the memory device 20 is a lessthanperfect memory device, and may include some memory locations which produce erroneous results when data is retrieved from those locations. To provide error detection for the memory device 20, without increasing the required memory capacity, the resolution of the digital data represented by the digital data stream is reduced (e.g. by one data bit), and an error detection code, (e.g. in the form of a parity bit), is substituted for that data bit. For example, for a 16bit digital audio signal, the LSB is stripped from each sample, resulting in an audio signal having a resolution of 15bits. As described above, for some audio applications, such as telephone answering machines, this loss of resolution is unnoticeable by a user.

The parity generator 30 generates, in a known manner, a parity bit for the full sized (16 bit) digital sample

supplied to its input terminal (less any bits that will be discarded). In the illustrated embodiment, the parity bit is an odd parity bit, although an even parity bit may also be used. This parity bit is appended to the reduced resolution (15 bit) digital audio signal sample as its LSB. The nature of the parity bit is that it has the values logic '1' and logic '0' about equally. The DC offset resulting from appending this bit to a digital sample as the LSB, thus, is negligible, even during silent periods. In addition, the use of the parity bit as the LSB provides a desirable dithering function. This parity encoded digital sample is stored in the memory device 20 at locations controlled in a known manner by a memory controller (not shown).

Fig. 2 is a block diagram of apparatus according to the present invention for reading previously written data from the memory device 20. In Fig. 2, the memory device 20 is the same memory device illustrated in Fig. 1. An output terminal of the memory device 20 is coupled to respective input terminals of an error detector 60 and an error corrector 40. The error detector 60 corresponds to the error detecting code generator 30 (of Fig. 1) and may be any circuit which provides an indication of the integrity of the data encoded by the error detecting code generator 30. In the illustrated embodiment, the error detecting code generator is a parity generator, and the error detector is a parity check circuit 60. A multibit output terminal of the error corrector 40 produces a stream of successive errorcorrected multibit digital samples (represented by the thick signal line) in a manner described in more detail below, and is coupled to a corresponding input terminal of utilization circuitry 50. An output terminal of the error detector 60 is coupled to a control input terminal of the error corrector 40.

In operation, the memory device 20 retrieves data signal samples from locations in the memory device 20 controlled in a known manner by the memory controller (not shown). The retrieved samples may have bits which are not the same as those of the previously stored sample. The error detector 60 performs a data integrity check on the retrieved sample and generates an

error signal when an error has been detected in the retrieved sample. This error signal is supplied to the error corrector 40, which performs a correction function, described in more detail below, in response to the error signal. The error corrector 40 produces a stream of successive multibit digital samples which either represent the originally stored data signal or reduce the noise introduced into the signal by errors in the memory device 20 (e.g. by linear interpolation between the last good data sample and the next good data sample). The error corrector 40 supplies that sample stream to the utilization circuitry 50. The combination of the error detector 60 and error corrector 40 provides a correction function in the event that a digital sample is retrieved from a defective location in the memory device 20. The utilization circuitry 50 processes the error corrected data stream. For example, in a tapeless sound recorder, the utilization circuitry may include a digitaltoanalog converter, audio amplifier and speaker.

Fig. 3 is a more detailed block diagram of the error corrector 40 illustrated in Fig. 2, and Fig. 4 and Fig. 5 are waveform diagrams useful in understanding the operation of the portion of that apparatus. In Fig. 3, thick signal lines represent signal paths carrying multibit digital signals, and thin signal lines represent signal paths carrying either single bit digital signals, or clock signals. In Fig. 3, an input terminal 48 is coupled to the output terminal of the memory 20 (of Fig. 2). Input terminal 48 is coupled to an input terminal of the parity check circuit 60 and a data input terminal of a first latch 41. An output terminal of the first latch 41 is coupled to a data input terminal of a second latch 42 and a first input terminal of an adder 43. An output terminal of the second latch 42 is coupled to a first data input terminal of a multiplexer 44 and a second input terminal of the adder 43. An output terminal of the adder 43 is coupled to a second data input terminal of the multiplexer 44 through a dividebytwo circuit 45. The combination of the adder 43 and dividebytwo circuit 45 forms an averaging circuit 46. An output terminal of the multiplexer 44 is coupled to an output terminal 49. The output

terminal 49 is coupled to the input terminal of the utilization circuitry 50 (of Fig. 2).

The parity error output terminal of the parity check circuit 60 is coupled to an error input terminal E of a control circuit 47. A clock generator (not shown) is coupled to a clock input terminal C of the control circuit 47. A first strobe output terminal S1 of the control circuit 47 is coupled to a control input terminal of the first latch 41; a second strobe output terminal S2 of the control circuit 47 is coupled to a control input terminal of the second latch 42, and a multiplexer control signal output terminal SEL of the control circuit 47 is coupled to a control input terminal of the multiplexer 44.

The operation of the apparatus illustrated in Fig. 3 will be explained in conjunction with the waveform diagrams illustrated in Fig. 4 and Fig. 5. In operation, a clock generator (not shown) produces a clock signal in synchronism with the digital data samples produced by the memory 20 in a known manner. Referring to Fig. 4, the sequence of samples is illustrated in the top line, DATA IN. The first illustrated sample, is S0, the next is S1, and so forth. The error signal at the error input terminal E of the control circuit 47 is illustrated on the second line, ERROR, of Fig. 4. When this signal is low, it indicates that no error has occurred in the corresponding sample, and if the signal is high, it indicates that a parity error has been detected by the parity check circuit 60.

The error signal for each sample is evaluated by the control circuit 47. When the error signal indicates that no error has occurred, the control circuit 47 provides a strobe signal, STROBE 1, illustrated on the third line of Fig. 4, to the first latch 41. At the falling edge of the first strobe signal, STROBE 1, the first latch 41 latches the signal from the input data input terminal 48, and supplies it to its output terminal in a known manner. The output from the first latch 41 is illustrated as the fourth line in Fig. 4.

In a similar manner, the control circuit 47 supplies a second strobe signal, STROBE 2, illustrated on the fifth line of Fig.

4, to the second latch 42. In response to the falling edge of the second strobe signal, STROBE 2, the second latch 42 latches the signal from the output terminal of the first latch 41, and supplies it to its output terminal in a known manner. The output from the second latch 42 is illustrated as the sixth line on Fig. 4.

In addition, the control circuit 47 also supplies the multiplexer control signal, SELECT, illustrated as the seventh line in Fig. 4, to the control input terminal of the multiplexer 44. When the multiplexer control signal, SELECT, is low, the multiplexer 44 is conditioned to pass the signal from the output terminal of the second latch 42 to the output terminal 49. When the multiplexer control signal, SELECT, is high, the multiplexer 44 is conditioned to pass the signal from the output terminal of the averaging circuit 46 to the output terminal 49.

So long as no parity errors are detected by the parity check circuit 60, the control circuit 47 continually supplies the first and second strobe signals (STROBE 1 and STROBE 2) to the first and second latches, 41 and 42, respectively, and the multiplexer control signal is maintained low, conditioning the multiplexer 44 to pass the signal from the second latch 42 to the output terminal 49. In this operating mode, the first and second latches, 41 and 42, act as pipeline registers and the input samples, DATA IN, are passed through the error handler 40 delayed, but without any changes.

If, however, the error signal, ERROR, at the error input terminal E of the control circuit 47 indicates that a parity error has occurred, the sample currently at the input terminal 48 is invalid. In this case, no strobe signal STROBE 1 is supplied to the first latch 41, and it continues to hold the most recent good sample. However, the second strobe signal, STROBE 2, is still supplied to the second latch, regardless of the state of the error signal ERROR from the control circuit 47. In addition, the multiplexer control signal SELECT is maintained low to condition the multiplexer 44 to pass the signal from the second latch 42 to the output terminal 49.

Referring to Fig. 4, the error signal ERROR is low during the sample time for sample S0, 401, indicating that sample S0 is a good sample. In response, the trailing edge 402 of the first strobe signal, STROBE 1, latches the good sample S0 from the input terminal 48 (DATA INPUT) into the first latch 41, and it appears at its output terminal, as illustrated in the waveform LATCH 41. At the same time, the trailing edge 403 of the second strobe signal STROBE 2 latches the previous symbol (unlabeled) from the first latch 41 into the second latch 42 and it appears at its output terminal as illustrated in waveform LATCH 42. Also, the multiplexer control signal SELECT is low at that sample period 408, and the output signal from the second latch 42 is supplied to the utilization circuitry 50.

Sample S1, however, is found by the parity check circuit 60 to have bad parity, and the error signal, ERROR, is made high for the duration of sample S1, at 404, to indicate this. While the error signal, ERROR, is high, the control circuit 47 does not generate a first strobe signal STROBE 1. Thus, there is no strobe signal at 410 in the sample period after the trailing edge 402. This prevents the bad sample S1 from being latched into the first latch 41. Instead, the previous good sample, S0, remains at the output of the first latch 41.

The second latch 42, however, continues to receive the second strobe signal, STROBE 2, and it latches the signal from the output terminal of the first latch 41 to its output terminal in the normal fashion. For example, the trailing edge 406 of the second strobe signal, STROBE 2 causes the second latch 42 to latch the signal S0 which remained at the output terminal of the first latch 41 and supply it to its output terminal, LATCH 42.

If a single isolated sample is bad, that is if the next sample after a bad sample is a good sample, as indicated at 412 of the parity error signal ERROR from the parity check circuit 60, then both the first latch 41 and the second latch 42, again receive strobe signals in the normal manner. For example, in Fig. 4, after the bad sample, S1, the trailing edge 414 of the first strobe signal, STROBE 1, causes the first latch 41 to latch the next succeeding

good sample S2 at the data input terminal 48 and supply it to its output terminal LATCH 41, while the trailing edge 416 of the second strobe signal STROBE 2 causes the second latch 42 latch the signal S0 and supply it to its output terminal LATCH 42. The output signal from the first latch 41 is the most recent good sample S2, and the output signal from the second latch 42 is the previous good signal S0. As described above, the intervening bad sample was not latched. At this time, the averaging circuit 46 produces a signal which is the average of the value of the two signals, S0 and S2, latched by the first and second latches, 41 and 42, respectively. When the first good sample after a bad sample has been latched into the first latch 41, the multiplexer control signal supplied to the multiplexer 44 for this sample period, at 418, conditions the multiplexer 44 to couple the signal from the averaging circuit 46 to the output terminal 49. In this manner, if an isolated sample is bad, it is replaced with a sample having the average of the two good samples surrounding it.

Fig. 5 is a waveform diagram illustrating the operation of the circuit illustrated in Fig. 3 responding to different input signal conditions. In Fig. 5, two samples in a row, S1 and S2, have parity errors detected. The operation of the circuit of Fig. 3, up to the reception of the second bad sample S2, is similar to the operation of that circuit illustrated in Fig. 4 and that operation is not described in detail below. Time 502 of the parity error signal ERROR, indicates that the sample S2 also contains a parity error. Because sample S2 is also bad, then, as before, no first strobe signal STROBE 1 is supplied to the first latch 41. Thus, at 504 of the first strobe signal STROBE 1, no strobe signal occurs, and the previous good sample S0 remains in the first latch 41. However, at 506 of the second strobe signal STROBE 2, the second latch 42 relatches the last good sample S0 from the first latch 41, and supplies it to its output terminal LATCH 42. At this time, both the first latch 41 and the second latch 42 contain the last good sample S0. At time 510, the multiplexer control signal SELECT is maintained low, and the multiplexer 44 is conditioned to continue to pass the signal from the second latch 42 to the output terminal

44. This will continue so long as bad samples are received at the input terminal 48.

At time 508, the parity error signal ERROR is low, indicating that the next sample, S3 does not contain a parity error. As described above, in response, the trailing edge 512 of the first strobe signal STROBE 1 latches the most recent good sample S3 into latch 41, which passes it to its output terminal LATCH 41. At this time, the first latch 41 contains the most recent good sample S3, and the second latch 42 contains the last good sample S0. Also at this time, the averaging circuit 46 produces a signal which is the average of those two samples. As before, when a first good sample is latched into the first latch 41 after a bad sample had been previously received, the multiplexer control signal SELECT, at 514, is made high, which conditions the multiplexer 44 to couple the signal from the averaging circuit 46 to the output terminal 49. In this manner, if a series of bad samples is received, the last good sample is repeated at the output terminal, until another good sample is received. Then, one sample containing the average of the last received good sample and the newly received good sample is produced before the error corrector 40 resumes its normal operational mode.

The present invention has been described with reference to an embodiment fabricated from discrete components. One skilled in the art will understand that the invention may also be practiced by the use of a microprocessor programmed to access a memory device 20 and execute a program to process data samples as described above.

Claims:

1. A method for concealing errors in stored digital samples, comprising the steps of:

receiving a multibit digital input sample;

storing a multibit storage sample representing said input sample in a memory (20);

retrieving said stored multibit sample from said memory (20);

calculating an error detecting code, corresponding to said input sample, containing a predetermined number of bits;

forming said storage sample by substituting said predetermined number of error detecting code bits for said predetermined number of least significant bits of said input sample;

examining said retrieved sample to detect an error;

if an error is detected, producing a substitute sample for said retrieved sample, otherwise producing said retrieved sample.

2. The method of claim 1 wherein the step of producing a substitute sample comprises the steps of:

if a single error is detected, producing a substitute sample comprising the average of a previous correct sample and a current correct sample; and

if more than one consecutive error is detected, repeatedly producing a substitute sample comprising a previous correct sample until a next correct sample is received, then producing a substitute sample comprising the average of the previous correct sample and the next correct sample.

3. The method of claim 1 wherein the step of producing a substitute sample comprises the steps of:

storing a previous correct sample;

when an error is detected, producing the substitute sample comprising the previous correct sample;

then when a current correct sample is received, producing the substitute sample comprising the average of the previous correct sample and the current correct sample.

4. The method of claim 1 wherein the step of calculating an error detecting code comprises the step of calculating a parity bit corresponding to the input sample.

5. The method of claim 4 wherein the step of examining a retrieved sample to detect an error comprises the step of determining the parity of the retrieved storage sample and if it is not a predetermined parity, detecting an error.

6. An apparatus for concealing errors in stored digital samples, comprising:

a source (10) of a multibit digital input sample;

a memory device (20) for storing a storage sample representing said input sample and retrieving a previously stored storage sample;

an error detecting code generator (30), coupled to said input sample source (10), generating an error detecting code having a predetermined number of bits;

said memory device (20) storing said storage sample comprising said input sample in which said error detecting code has been substituted for said predetermined number of least significant bits of said input sample;

an error detector (60), coupled to said memory device (20), for detecting an error in said retrieved sample; and

an error corrector (40), coupled to said memory device (20) and said error detector (60) for producing substitute samples

if an error is detected and producing said retrieved storage sample otherwise.

7. The apparatus of claim 6 wherein said memory device (20) is a memory device with known imperfect memory locations.

8. The apparatus of claim 6 wherein said error detecting code generator (30) is a parity generator.

9. The apparatus of claim 8 wherein said error detector (60) is a parity error checker.

10. The apparatus of claim 6 wherein said error corrector (40) comprises:

a first latch (41), coupled to said memory device (20), for holding a current correct sample;

a second latch (42), coupled to said memory device (20), for holding a previous correct sample;

an averaging circuit (46), responsive to said first (41) and second (42) latches;

a multiplexer (44), having a first data input responsive to said second latch (42), a second data input coupled to said averaging circuit (46), and an output producing the substitute sample; and

a control circuit (47), responsive to said error detector (60), for conditioning said multiplexer (44) to couple said averaging circuit (46) to said output when a current good sample is received after bad sample has been received, and for conditioning said multiplexer (44) to couple said second latch (42) to said output otherwise.

11. The apparatus of claim 10 wherein said control circuit (47) further comprises:

circuitry, responsive to said error detector (60), for generating a strobe signal for said first latch (41) when a sample is retrieved from said memory device (20) and said error detector (60) does not detect an error; and

circuitry for generating a strobe signal for said second latch (42) when a sample has been retrieved from said memory device (20).