CONTROL GATE

ABSTRACT

A method for forming a semiconductor device is disclosed. The method includes providing a substrate prepared with a second gate structure. An inter-gate dielectric is formed on the substrate and over the second gate. A first gate is also formed. The first gate is adjacent to and separated from the second gate by the inter-gate dielectric. The substrate is patterned to form a split gate structure with the first and second adjacent gates. The split gate structure is provided with an e-field equalizer adjacent to the first gate. The e-field equalizer improves uniformity of e-field across the first gate during operation.

Fig. 3f