T13.

[0043] Each of the gate stack structures ST1 and ST2 may include the upper stack structure UST forming the cell structure CS. The cell structure CS may be disposed in the cell region R1. An end portion of the cell structure CS may extend toward the contact region R2 to provide a pad region connected to contact plugs 171 shown in FIG. 2A. The cell structure CS is penetrated by the channel structure CH in the cell region R1.

[0044] The first and second dummy structures DS1 and DS2 may be spaced apart from each other in the horizontal direction by the second and third trenches T12 and T13. The first dummy structure DS1 adjacent to the cell structure CS may be spaced apart from the cell structure CS in the horizontal direction by the first trench T11. One second dummy structure adjacent to the first dummy structure DS1 among the second dummy structures DS2 may be spaced apart from the first dummy structure DS1 in the horizontal direction by the second trench T12. The second dummy structures DS2 may be spaced from each other in the horizontal direction by the third trenches T13. A portion of the upper stack structure UST may form each of the first and second dummy structures DS1 and DS2.

[0045] Referring to FIG. 1B, the lower stack structure LST extends from the cell region R1 to the contact region R2 to surround each of the grooves G11 to G15, and forms the gate stack structures ST1 and ST2. The lower stack structure LST is penetrated by the channel structures CH

in the cell region R1.

[0046] The grooves G11 to G15 are disposed in the contact region R2 and spaced apart from each other. The grooves G11 to G15 may extend to different depths in the lower stack structure LST. The grooves G11 to G15 may be sequentially disposed in the first direction I. However, embodiments of the present disclosure are not limited thereto. For example, the grooves G11 to G15 may be arranged in various configurations in the horizontal direction. The slit 151 may extend through each of the groves G11 to G15. Each of the grooves G11 to G15 may include a first part disposed in the first gate stack structure ST1 and a second part disposed in the second gate stack structure ST2.

[0047] The lower stack structure LST may include connection parts disposed in the contact region R2. For example, the lower stack structure LST may include first connection parts LP1 and a second connection part LP2. The first connection parts LP1 may be parts of the lower stack structure LST, which are disposed between adjacent grooves G11 to G15. The second connection part LP2 may be a part of the lower stack structure LST, which extends in the first direction I towards the first connection parts LP1 from the cell region R1. The second connection part LP2 may be connected to the first connection parts LP1. Each of the grooves G11 to G15 is surrounded by a sidewall defined by first and second connection parts.

[0048] FIGS. 2A and 2B illustrate cross-sections of the semiconductor memory device in accordance with an embodiment of the present

the first connection part LP1 shown in FIG. 2A, may have vertical or substantially vertical sidewalls.

[0056] The first trench T11 is disposed between the cell region R1 shown in FIG. 1A and the grooves G11 to G15, and extends in the third direction III to penetrate the second upper layers 105[m+1] to 105[n]. The first trench T11 overlaps with the first upper layers 105[k+1] to 105[m]. The uppermost first upper layer 105[m] may be a bottom surface of the first trench T11.

[0057] The second trench T12 extends in the third direction III to penetrate the second upper layers 105[m+1] to 105[n] and the first upper layers 105[k+1] to 105[m] between the first trench T11 and the grooves G11 to G15. The second trench T12 may overlap with the lower stack structure LST, and the uppermost lower layer 105[k] may be a bottom surface of the second trench T12.

[0058] The lower layers 105[1] to 105[k] may constitute the gate stack structure ST1. Portions of the respective first upper layers 105[k+1] to 105[m] constituting the cell structure CS and portions of the respective second upper layers 105[m+1] to 105[n] may constitute the gate stack structure ST1. The first dummy structure DS1 may overlap with the first upper layers 105[k+1] to 105[m] of the cell structure CS. The first dummy structure DS1 may be configured with other portions of the respective second upper layers 105[m+1] to 105[n]. Each of the second dummy structures DS2 may overlap with the lower stack structure LST. Each of the second dummy structures DS2 may be configured with other

structure LST and are disposed on the first patterns P1. The first sidewall S1 of the first groove G11 may be sidewalls of the second patterns P2. The second sidewall S2 and the third sidewall S3 of the first groove G11 may face each other and extend from the first sidewall S1. The second sidewall S2 may have the first stepped structure SW1 shown in FIG. 4A, and the third sidewall S3 may have the second stepped structure SW2 shown in FIG. 4A.

[0073] A second groove G12 may include fourth to sixth sidewalls S4 to S6. The second groove G12 may be surrounded by first patterns P1 and second patterns P2. The fourth sidewall S4 of the second groove G12 may be comprise faces of the first patterns P1. The fifth sidewall S5 and the sixth sidewall S6 of the second groove G12 may face each other and extend from the fourth sidewall S4. The fifth sidewall S5 may have the first stepped structure SW1 shown in FIG. 4A, and the sixth sidewall S6 may have the second stepped structure SW2 shown in FIG. 4A. The second groove G12 may further include seventh to ninth sidewalls S7 to S9 extending toward the upper stack structure UST respectively from the fourth to sixth sidewalls S4 to S6. The seventh to ninth sidewalls S7 to S9 comprise faces of the second patterns P2.

[0074] Each of the first sidewall S1, the fourth sidewall S4, and the seventh sidewall S7 may be formed to have a gradient greater than that of each of the first stepped structure SW1 and the second stepped structure SW2. For example, the gradient of each of the first sidewall S1, the fourth sidewall S4, and the seventh sidewall S7 may be vertical or

conductive layer 105A described with reference to FIG. 3, and each of the second material layers may be formed as the interlayer insulating layer 105B described with reference to FIG. 3. In another embodiment, the first material layers and the second material layers may be formed of materials having different etch rates. In an example, each of the first material layers may be formed as a sacrificial layer replaced with the conductive layer 105A described with reference to FIG. 3 in a subsequent process, and each of the second material layers may be formed as the interlayer insulating layer 105B. In another example, each of the first material layers may be formed as the conductive layer 105A described with reference to FIG. 3, and each of the second material layers may be formed as a sacrificial layer replaced with the interlayer insulating layer 105B in a subsequent process. Each of the first sacrificial layers may include a nitride layer, and each of the second sacrificial layers may include a doped silicon layer.

[0086] Subsequently, a first mask pattern 311 may be formed on the stack structure 300. Before the first mask pattern 311 is formed, processes for forming the channel structures CH shown in FIGS. 1A and 1B in the cell region R1 of the stack structure 300 may be performed.

[0087] The first mask pattern 311 may include a photoresist pattern. The first mask pattern 311 may include a first opening OP1 and second openings OP2, which open the contact region R2. The first opening OP1 may be disposed between the cell region R1 and the second openings OP2. In other words, the first opening OP1 may be formed closer to the cell

illustrating a fifth mask pattern 319. FIG. 11B illustrates a cross-section of the stack structure 300 taken along line C-C' shown in FIG. 11A. FIG. 11C illustrates a cross-section of the stack structure 300 taken along line D-D' shown in FIG. 11A.

[00114] Referring to FIGS. 11A to 11C, the fifth mask pattern 319 may be formed on the stack structure 300. Before the fifth mask pattern 319 is formed, the fourth mask pattern 317 shown in FIGS. 10A and 10B may be removed. The fifth mask pattern 319 may include a photoresist pattern.

[00115] The fifth mask pattern 319 may be formed to cover the first trench T11, the second trench T12, and the first to third grooves G11 to G13. The fifth mask pattern 319 may include a seventh opening OP7 and an eighth opening OP8. The seventh opening OP7 exposes the second preliminary groove PG2 shown in FIGS. 10A and 10B, and the eighth opening OP8 exposes the third preliminary groove PG3 shown in FIGS. 10A and 10B. The seventh opening OP7 and the eighth opening OP8 are spaced apart from each other.

[00116] At least some of the lower layers 305[1] to 305[k] are etched using the fifth mask pattern 319 as an etch mask. The first and second upper layers 305[k+1] to 305[n] exposed by the seventh and eighth openings OP7 and OP8 may be etched as well. In particular, a vertical etch process, e.g. an isotropic etching, may be performed to extend the depth of the trenches downwards by several layers while preserving the stepped shape of the trenches.

[00131] Each of the gate stack structures ST11 and ST12 may be penetrated by channel structures CH disposed in the cell region R1. Although not shown in FIGS. 13A and 13B, a sidewall of each of the channel structures CH may be surrounded by a memory layer. The channel structures CH and the memory layer may be formed with the same material layers as described with reference to FIGS. 1A and 1B.

[00132] Each of the gate stack structures ST11 and ST12 may have an upper stack structure UST' that overlaps with a lower stack structure LST'. The upper stack structure UST' and the lower stack structure LST' are penetrated by a slit 451.

[00133] Referring to FIG. 13A, the upper stack structure UST' may be divided into a cell structure CS and dummy structures DS, which are separated from each other by a first trench T21 and second trenches T22, which are disposed in the contact region R2.

[00134] The first trench T21 may be disposed between the cell region R1 and the second trenches T22. The second trenches T22 may respectively open the grooves G21 to G25 shown in FIG. 13B. The first trench T21 and the second trenches T22 may penetrate the upper stack structure UST'.

[00135] Each of the gate stack structures ST11 and ST12 may include the upper stack structure UST' forming the cell structure CS. The cell structure CS may be disposed in the cell region R1. An end portion of the cell structure CS may extend toward the contact region R2 to provide a pad region connected to contact plugs 471 shown in FIG. 14A.

[00148] Each of the cell structure CS and the dummy structures DS may overlap with the lower stack structure LST', and be configured with some of the upper layers 405[k+1] to 405[n]. The cell structure CS and the lower layers 405[1] to 405[k] may constitute the gate stack structure ST11. The flatness in the contact region R2 can be improved by the dummy structures DS.

[00149] Each of the grooves G21 to G25 and the first and second trenches T21 and T22 may be filled with a gap fill insulating layer 441. Each of the grooves G21 to G25 and the first and second trenches T21 and T22 may include stepped sidewalls facing each other. The stepped structures formed in the first trench T21 and the grooves G21 to G25 may provide pad regions connected to contact plugs 471.

[00150] Each of the upper layers 405[k+1] to 405[n] and the lower layers 405[1] to 405[k] may be comprise a conductive layer 105A and an interlayer insulating layer 105B as described with reference to FIG. 3.

[00151] The conductive layers included in the upper layers 405[k+1] to 405[n] may be first select lines connected to first select transistors, and the conductive layers included in the lower layers 405[1] to 405[k] may be word lines connected to memory cells or second select lines connected to second select transistors.

[00152] FIG. 15 is a sectional view illustrating stepped structures shown in FIGS. 14A and 14B. A first stepped structure SW11 and a second stepped structure SW12, which are shown in FIG. 15, may be formed in each of the grooves G21 to G25 and the first and second

section of the stack structure 500 taken along line Ca-Ca' shown in FIG. 21A. FIG. 21C illustrates a cross-section of the stack structure 500 taken along line Da-Da' shown in FIG. 21A.

[00190] Referring to FIGS. 21A to 21C, the fourth mask pattern 519 may be formed on the etch stop pattern 513 to cover the stack structure 500. Before the fourth mask pattern 519 is formed, the third mask pattern 517 shown in FIGS. 20A and 20B may be removed. The fourth mask pattern 519 may include a photoresist pattern.

[00191] The fourth mask pattern 519 may be formed to cover the cell region R1, the first trench T21, and the first to third grooves G21 to G23. The fourth mask pattern 519 may include a fifth opening OP15. The fifth opening OP15 exposes the second and third preliminary grooves PG22 and PG23 shown in FIGS. 20A and 20B. The fifth opening OP15 may extend in the horizontal direction parallel to the first trench T21. For example, the fifth opening OP15 may extend in the second direction II. A portion of the etch stop pattern 513 may be exposed by the fifth opening OP15.

[00192] At least some of the layers 505 are etched by a vertical etch process using a combination of the fourth mask pattern 519 and the etch stop pattern 513 as an etch mask. The stepped structures Se exposed in each of the regions in which the second openings OP12 and the fifth opening OP15 overlap with each other are moved to a fourth depth d14 and a fifth depth d15, which are deeper than the third depth d13.

[00193] The fourth groove G24 is etched to the fourth depth d14 in

[00196] It can be challenging to fully cure the photoresist layer when it has a substantial thickness, which leads to errors in an etching process. For example, uncured portions of the mask may be removed by vertical etching, causing uneven sidewalls and mismatch between the mask and the trenches. In general, thicker layers of photoresist are problematic in a photocuring operation which has limitations of a depth of focus. However, these issues are substantially reduced by using a combination of hard mask and photoresist materials as described above.

[00197] FIGS. 22A and 22B are plan and sectional views illustrating a process of forming a gap fill insulating layer 521. Dashed lines shown in FIG. 22A represent a layout of the first to fifth grooves G21 to G25. FIG. 22B illustrates a cross-section of the stack structure 500 taken along line Ca-Ca' shown in FIG. 22A.

[00198] Referring to FIG. 22A, each of the first to fifth grooves G21 to G25 is surrounded by the lower layers 505[1] to 505 [k] shown in FIG. 22B. The lower layers 505[1] to 505 [k] shown in FIG. 22B may surround each of the first to fifth grooves G21 to G25, to define first to fourth sidewalls 1W' to 4W' of each of the first to fifth grooves G21 to G25. The first sidewall 1W' and the second sidewall 2W' face each other in the first direction I, and the third sidewall 3W' and the fourth sidewall 4W' face each other in the second direction II. The stepped structures of each of the first to fifth grooves G21 to G25 may be respectively formed at lower portions of the first sidewall 1W' and the second sidewall 2W', which are adjacent to a bottom surface of a groove.

[00224] Each of the upper grooves TG1 and TG2 and the grooves G31 to G35 may be filled with a gap fill insulating layer 641. Each of the upper grooves TG1 and TG2 and the grooves G31 to G35 may stepped sidewalls. The stepped sidewalls may have steps formed by the thin films 605[1] to 605[n] constituting the gate stack structure ST21, and provide pad regions connected to contact plugs 671. Each of the contact plugs 671 may extend in the third direction III to penetrate the gap fill insulating layer 641.

[00225] Each of the second upper groove TG2 and the grooves G31 to G35 may include a first stepped structure and a second stepped structure, which have different gradients and face each other. The first stepped structure and the second stepped structure may be the same structures described with reference to FIG. 4A.

[00226] The first upper groove TG1 may include third stepped structures that face each other and are symmetrical to each other. The third stepped structure may be the same as the structure described with reference to FIG. 4B.

[00227] Conductive layers constituting the thin films 605[1] to 605[k] included in the gate stack structure ST21 may include word lines connected to memory cells and select lines connected to select transistors. For example, conductive layers included in the second upper layers 605[m+1] to 605[n] of the gate stack structure ST21 may be used as first select lines, and conductive layers included in the first upper layers 605[k+1] to 605[m] and the lower layers 605[1] to 605[k] of the gate

(SRAM) 1111, a CPU 1112, a host interface 1113, an error correction code (ECC) 1114, and a memory interface 1115. The SRAM 1111 is used as an operational memory of the CPU 1112, the CPU 1112 performs overall control operations for data exchange of the memory controller 1110, and the host interface 1113 includes a data exchange protocol for a host connected with the memory system 1100. The ECC 1114 detects and corrects errors in data read from the memory device 1120, and the memory interface 1115 interfaces with the memory device 1120. In addition, the memory controller 1110 may further include a ROM for storing code data for interfacing with the host, and the like.

[00269] The memory system 1100 configured as described above may be a memory card or a Solid State Drive (SSD), in which the memory device 1120 is combined with the controller 1110. For example, when the memory system 1100 is an SSD, the memory controller 1100 may communicate with an external entity (e.g., the host) through various interface protocols, such as a Universal Serial Bus (USB) protocol, a Multi-Media Card (MMC) protocol, a Peripheral Component Interconnection (PCI) protocol, a PCI-Express (PCI-E) protocol, an Advanced Technology Attachment (ATA) protocol, a Serial-ATA (SATA) protocol, a Parallel-ATA (PATA) protocol, a Small Computer System Interface (SCSI) protocol, an Enhanced Small Disk Interface (ESDI) protocol, and an Integrated Drive Electronics (IDE) protocol.

[00270] FIG. 32 is a block diagram illustrating a configuration of a computing system in accordance with an embodiment of the present

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a lower stack structure having a cell region and a contact region extending in a horizontal direction from the cell region, wherein the lower stack structure includes lower layers stacked on each other, and the lower layers include first patterns and second patterns disposed on the first patterns;

a first groove surrounded by the second patterns in the contact region, the first groove overlapping with the first patterns; and

a second groove surrounded by the first patterns and the second patterns in the contact region,

wherein the first groove has a first sidewall defined along sidewalls of the second patterns and a second sidewall and a third sidewall, which extend from the first sidewall and face each other,

wherein the second groove has a fourth sidewall, a fifth sidewall, a sixth sidewall and a seventh sidewall, the fourth sidewall defined along sidewalls of the first patterns, the fifth sidewall and the sixth sidewall extending from the fourth sidewall and facing each other, the seventh sidewall defined along sidewalls of the second patterns aligned above the fourth sidewall, and

wherein each of the second sidewall and the fifth sidewall has a first stepped structure, and each of the third sidewall and the sixth sidewall has a second stepped structure.

2. The semiconductor memory device of claim 1, wherein the first stepped structure and the second stepped structure have different gradients.

3. The semiconductor memory device of claim 1, wherein each of the first sidewall and the fourth sidewall has a gradient greater than those of the first stepped structure and the second stepped structure.

4. The semiconductor memory device of claim 1, wherein the second groove includes an eighth sidewall and a ninth sidewall extending from the seventh sidewall and facing each other, and

wherein the eighth sidewall and the ninth sidewall are defined along sidewalls of the second patterns aligned above the fifth and sixth sidewalls.

5. The semiconductor memory device of claim 1, further comprising an upper stack structure including first upper layers stacked on the lower stack structure and second upper layers stacked on the first upper layers.

6. The semiconductor memory device of claim 5, further comprising:

a first trench penetrating the second upper layers between the cell region and the first groove, the first trench overlapping with the first upper layers;

a second trench penetrating the second upper layers and the first upper layers between the first trench and the first groove, the second trench overlapping with the lower stack structure; and

third trenches penetrating the second upper layers and the first upper layers to respectively open the first and second grooves.

7. The semiconductor memory device of claim 6, wherein the upper stack structure is separated into a cell structure overlapping with the cell region and a dummy structure overlapping with the contact region by the first trench, the second trench, and the third trenches.

8. The semiconductor memory device of claim 6, wherein the first trench has sidewalls that face each other to be symmetrical to each other, and

each of the second and third trenches has sidewalls that face each other and have different gradients.

9. The semiconductor memory device of claim 6, wherein one of both sidewalls of each of the second and third trenches has the first stepped structure, and the other of both the sidewalls of each of the second and third trenches has the second stepped structure.

10. The semiconductor memory device of claim 6, wherein end portions of the second upper layers, which extend toward a sidewall of the first trench from the cell region, form a third stepped structure,

wherein an upper portion of the first stepped structure has the third stepped structure.

11. The semiconductor memory device of claim 5, further comprising:

a first upper groove surrounded by the second upper layers between the cell region and the first groove, the first upper groove having sidewalls that face each other and are symmetrical to each other, the first upper groove overlapping with the first upper layers; and

a second upper groove surrounded by the second upper layers and the first upper layers between the first upper groove and the first groove, the second upper groove having sidewalls facing each other, the second upper groove overlapping with the lower stack structure,

wherein the first upper layers and the second upper layers extend to the contact region from the cell region to surround each of the first and second grooves.

12. The semiconductor memory device of claim 11, wherein the sidewalls of the second upper groove have different gradients.

13. The semiconductor memory device of claim 11, wherein one of the sidewalls of the second upper groove has the first stepped structure, and the other of the sidewalls of the second upper groove has the second stepped structure.

14. The semiconductor memory device of claim 5, wherein each of the lower layers, the first upper layers, and the second upper layers is formed in a stacking structure of an interlayer insulating layer and a conductive layer.

15. The semiconductor memory device of claim 5, further comprising channel structures penetrating the upper stack structure and the lower stack structure in the cell region.

16. The semiconductor memory device of claim 1, wherein the first stepped structure and the second stepped structure are symmetrical to each other.

17. The semiconductor memory device of claim 1, further comprising:

an upper stack structure including upper layers stacked on the lower stack structure;

a first trench penetrating the upper layers between the cell region and the first groove, the first trench overlapping with the lower stack structure; and

second trenches penetrating the upper layers to respectively open the first and second grooves.

18. The semiconductor memory device of claim 17, wherein the upper stack structure is separated into a cell structure and dummy structures by the first trench and the second trenches, the cell structure overlapping with the cell region, the dummy structures overlapping with the contact region.

19. The semiconductor memory device of claim 17, wherein each of the first and second trenches has sidewalls that face each other to be symmetrical to each other.

20. The semiconductor memory device of claim 17, wherein one of the sidewalls of each of the first and second trenches has the first stepped structure, and the other of the sidewalls of each of the first and second trenches has the second stepped structure.

21. The semiconductor memory device of claim 17, wherein each of the lower layers and the upper layers is formed in a stacking structure of an insulating layer and a conductive layer.

22. The semiconductor memory device of claim 17, further comprising channel structures penetrating the upper stack structure and the lower stack structure in the cell region.

23. A semiconductor memory device comprising:

a stack structure including conductive layers stacked in a vertical direction, the stack structure having a cell region and a contact region extending in a horizontal direction from the cell region; and

grooves formed in the stack structure in the contact region, the grooves being spaced apart from each other in the horizontal direction, the grooves having bottom surfaces disposed at different heights,

wherein each of the grooves is surrounded by a first stepped structure, a second stepped structure, and a sidewall defined by connection parts of the conductive layers,

wherein the first stepped structure and the second stepped structure face each other, and

wherein the sidewall in each of the grooves includes a lower portion and an upper portion, the lower portion extending from the first stepped structure to the second stepped structure, the upper portion aligned above the lower portion and including an uppermost layer of the conductive layers.

24. A semiconductor memory device comprising:

a stack structure including conductive layers stacked in a vertical direction, the stack structure having a cell region and a contact region extending in a horizontal direction from the cell region; and

grooves formed in the stack structure in the contact region, the grooves being spaced apart from each other in the horizontal direction, the grooves having bottom surfaces disposed at different heights,

wherein each of the grooves is surrounded by a first stepped structure, a second stepped structure, and a sidewall defined by connection parts of the conductive layers,

wherein the first stepped structure and the second stepped structure face each other in a first direction,

wherein the connection parts connect the first stepped structure and the second stepped structure, and

wherein the first stepped structure is asymmetric to the second stepped structure in the first direction.

25. The semiconductor memory device of claim 23, wherein the sidewall has a gradient greater than those of the first stepped structure and the second stepped structure.

26. The semiconductor memory device of claim 23, wherein the first stepped structure and the second stepped structure are symmetrical to each other.