

明 細 書

熱電素子の製造方法

技 術 分 野

この発明はゼーベック効果を利用した発電装置に用いる熱電素子、あるいはペルチェ効果を利用した冷却装置に用いる熱電素子の製造方法に関し、特に小型で多数の熱電対で構成される熱電素子の製造方法に関する。

背 景 技 術

熱電素子の熱電対は、その両端に温度差を与えることにより電圧を発生する。これがゼーベック効果であり、この電圧を電気エネルギーとして取り出すことようにしたものが熱電発電装置である。このような熱電発電装置によれば、熱エネルギーから電気エネルギーへの変換が直接できるため、廃熱利用に代表されるような熱エネルギーの有効的な利用方法として注目されている。

一方、熱電対に電流を流すと一端で発熱、他端で吸熱が起こる。これがペルチェ効果であり、この吸熱現象を利用して冷却装置が得られる。このような冷却装置は、機構部品を含まずかつ小型化も可能なことから、ポータブルな冷蔵庫あるいはレーザや集積回路などの局部冷却器として活用されている。

このように、熱電素子は構造が簡単で他の発電装置や冷却装置に比べて小型化にも有利な条件を備えており、有用性が高い。例えば、発電装置としては酸化還元電池のような電解液の漏洩や消耗の問題がないことから、電子式の腕時計などの携帯型電子機器への応用が期待される。

この熱電素子における従来の一般的な構造およびその製造方法は、たとえば、特開昭63-20880号公報あるいは特開平8-43555号公報に開示されている。ここで開示されているのは、発電用の熱電素子であるが、基本構造は冷却用の

熱電素子も同様である。そこで、以下の説明は煩雑さを避けて、発電用の熱電素子について行うものとする。

上記公報に開示されている従来の熱電素子は、多数の熱電対が平面的に形成されるようにp型とn型の熱電半導体を交互に規則的に配置し、それによって形成される熱電対を電氣的に直列に接続するものである。

このように熱電対を平面的に設けることにより熱電素子が板状になり、その表と裏とはそれぞれ熱電対の温接点が位置する面と冷接点が位置する面となる。そして、その熱電素子の発電は板状の素子の表裏の温度差によって行われる。

ところで、現在、熱発電の性能指数が最も高いと言われているBiTe系材料を用いた熱電対の出力電圧は、1対あたり $400\mu\text{V}/^{\circ}\text{C}$ ほどである。

このような熱電対を電子時計のような室温近辺で使用される携帯型電子機器に用いる場合、機器の内部での温度差はあまり期待できない。たとえば腕時計の場合、体温と外気温とにより生じる時計内部での温度差はせいぜい 2°C である。

そのため、電子時計の時計駆動に必要な1.5V以上の電圧を得るためには、およそ2000対以上のBiTe系の熱電対が必要となる。

さらに、腕時計の場合は、元々の内容積が小さい上に機械部品や電気回路部品を収納しなくてはならないので、使用する熱電発電素子は非常に小さいことが必須条件となる。

従来において、このような熱電対の数が多くかつ小型である熱電素子の製造方法としては、前述の特開昭63-20880号公報に開示された方法がある。

その方法は、まず薄い板状のp型とn型の熱電半導体をそれぞれの間に断熱材を挟みながら次々に積み重ねて接合した積層体を形成する。続いて、その積層体に一定間隔で溝を形成し、その後、この溝に断熱材を充填し、同一熱電材料の連結部を除去することにより、断熱材に囲まれ孤立したn型及びp型の熱電対を形成する。

そして、この熱電対同志を電氣的に直列接続して熱電素子を完成する。

また、特開平 8-43555 号公報に開示された方法では、まず板状の p 型と n 型の熱電半導体を別々の基板に接合した上で、それぞれの熱電半導体に縦方向と横方向とに細かい間隔で多数の溝入れ加工を行う。

この溝入れ加工により基板上に柱状の熱電半導体が規則的に立った、剣山状の形状のものができる。この剣山状のものを、n 型の熱電半導体によるものと p 型の熱電半導体によるものとを準備し、柱状の熱電半導体が互いに間にはいり合うように組み合わせ、絶縁性物質をその熱電半導体間に充填する。

最後に、上記基板を除去して、熱電対同志を電氣的に直列接続して熱電素子を完成する。

しかしながら、これらの熱電素子の製造方法によると、熱電半導体の材料そのものが非常に脆いために、熱電半導体を薄い板状に形成する工程や溝入れ加工により剣山状に形成する工程などにおいて、熱電半導体材料の破損が起こりやすいという問題がある。

特に、腕時計内に収容可能な超小型の熱電素子に 2000 対以上という多数の熱電対を形成しようとする、板状の熱電半導体の厚みや柱状の熱電半導体の太さを $100\mu\text{m}$ 程度以下にする必要があり、上述した脆弱性の問題はきわめて深刻となる。

そこでこの発明は、このような従来の熱電素子の製造方法による問題を解決するためになされたものであり、その目的は小型でかつ出力電圧を大きくするために多数の熱電対を有する熱電素子を、容易かつ効率よく製造する方法を提供することにある。

発明の開示

この発明による熱電素子の製造方法は、上記の目的を達成するため、次の各工程

を有する。

それぞれ厚さ方向の一部を残して同一ピッチで複数本の溝が平行に形成された n 型の熱電半導体の溝入りブロックおよび p 型の熱電半導体の溝入りブロックを作製する溝入りブロック作製工程、

該工程によってそれぞれ作製された n 型の熱電半導体の溝入りブロックと p 型の熱電半導体の溝入りブロックとを互いにその溝を形成した面が対向するように嵌合させる嵌合工程、

該工程によって互いに嵌合された前記 n 型の熱電半導体の溝入りブロックと p 型の熱電半導体の溝入りブロックの嵌合部の空隙に接着性のある絶縁部材を充填して固着し、一体化ブロックを形成する固着工程、

該工程によって形成された一体化ブロックにおける前記 n 型の熱電半導体と p 型の熱電半導体とが互いに嵌合している嵌合部以外の部分を除去して、n 型および p 型の熱電半導体素片を露出させる熱電半導体素片露出工程、

このような工程によって、熱電素子を製造することにより、脆弱性の問題がある熱電半導体材料をつねに塊（ブロック）として扱って加工するため、熱電半導体材料を破損することなく細密な加工を行なうことができ、極めて小さい多数の熱電半導体素片による多数の熱電対からなる熱電素子を容易に効率よく作製することが可能になる。

さらに、上記固着工程によって形成された一体化ブロックに、上溝入りブロック作製工程によって形成された溝の方向と交差する方向に複数本の溝加工を厚さ方向の一部を残して施す第 2 の溝加工工程と、該工程における溝加工部に絶縁部材を充填し固化させる固化工程とを行なった後、

該工程において絶縁部材を充填し固化させた一体化ブロックにおける n 型の熱電半導体と p 型の熱電半導体とが互いに嵌合している嵌合部以外の部分を除去して、

n型およびp型の熱電半導体素片を露出させる熱電半導体素片露出工程を行なうようにするとよい。

このようにすれば、同じ大きさの熱電素子を構成する熱電対の数が大幅に増加し、熱電発電素子として使用する場合の出力電圧を高めることができる。

さらにまた、上述の溝入りブロック作製工程と嵌合工程と固着工程とによって、2個の一体化ブロックを作製し、そのそれぞれに上記溝入りブロック作製工程で形成された溝の方向と交差する方向に同一ピッチで複数本の溝加工を厚さ方向の一部を残して施し、2個の溝入り一体化ブロックとする溝加工工程と、

その2個の溝入り一体化ブロックを互いに溝加工された面が対向するように嵌合させる第2の嵌合工程と、

該工程によって互いに嵌合された2個の溝入り一体化ブロックの嵌合部の空隙に接着性のある絶縁部材を充填して固着し、第2の一体化ブロックとする第2の固着工程とを行なった後、

その第2の一体化ブロックの上記嵌合部以外の厚さ部分を除去して、n型およびp型の熱電半導体素片を露出させる熱電半導体素片露出工程を行なうようにするとさらによい。

このようにすれば、同じ大きさの熱電素子を構成する熱電対の数がさらに大幅に増加し、熱電発電素子として使用する場合の出力電圧を一層高めることができる。

これらの熱電素子の製造方法において、上記溝入りブロック作製工程として、n型の熱電半導体ブロックおよびp型の熱電半導体ブロックに、それぞれ同一ピッチで複数本の溝加工を厚さ方向の一部を残して施す溝加工によって、上記n型の熱電半導体の溝入りブロックおよびp型の熱電半導体の溝入りブロックを作製する工程を採用することができる。

あるいは、上記溝入りブロック作製工程として、それぞれ溝入りブロックの成形

型を用いて、n型の熱電半導体材料とp型の熱電半導体材料を個別に成形および焼結することによって、上記n型の熱電半導体の溝入りブロックおよびp型の熱電半導体の溝入りブロックを作製する工程を採用することもできる。

これらの熱電素子の製造方法において、上記熱電半導体素片露出工程後に、露出されたn型とp型の熱電半導体素片を交互に直列に接続する電極を形成する電極形成工程を行えば、熱電素子を完成することができる。

あるいはまた、n型の熱電半導体ブロックとベースとを接合したn型の熱電半導体複合ブロックと、p型の熱電半導体ブロックとベースとを接合したp型の熱電半導体複合ブロックとを用意し、その各熱電半導体複合ブロックに対して、熱電半導体ブロックおよびp型の熱電半導体ブロックに、それぞれ同一ピッチで複数本の溝加工を前記各ベースとの界面付近までの深さで施す溝加工工程によって、n型の熱電半導体複合ブロックとp型の熱電半導体複合ブロックとを作製し、その対の熱電半導体複合ブロックを使用して、上述した嵌合工程、固着工程、溝加工工程、固化工程等を実施したり、さらにそれらの工程によって2個の一体化ブロックを作製し、それらに第2の溝加工を施して互いに嵌合させ、第2の一体化ブロックとした後、上記各ベースの部分を除くして、n型およびp型の熱電半導体素片を露出させる熱電半導体素片露出工程を行なうようにしてもよい。

このようにすることにより、熱電半導体材料を無駄なく利用することができる。

この場合、上記各ベースとして、熱電半導体ブロックの固着面より大きな面積を有するものを用い、嵌合工程において、n型の熱電半導体複合ブロックとp型の熱電半導体複合ブロックのそれぞれ熱電半導体ブロックが存在しない部分のベース間にスペーサを介挿し、該ベース間の間隔を略熱電半導体ブロックの厚さに相当する間隔に制御（規制）するとよい。

図面の簡単な説明

第1図から第6図は、この発明による熱電素子の製造方法の第1実施例を説明するための各製造工程を示す斜視図ある。

第7図および第8図は、それぞれ第3図一体化ブロック3における仮想線で囲んで示すAの部分の異なる接着例を示す拡大図である。

第9図は、同じく第1実施例における電極構成を説明するための完成した熱電素子の平面図である。

第10図から第14図は、この発明による熱電素子の製造方法の第2実施例を説明するための各製造工程を示す斜視図ある。

第15図から第17図は、この発明による熱電素子の製造方法の第3実施例を説明するための後半の製造工程を示す斜視図である。

第18図は、同じく第3実施例における電極構成を説明するための完成した熱電素子の平面図である。

第19図から第21図は、この発明による熱電素子の製造方法の第4実施例を説明するための一部の製造工程を示す斜視図である。

第22図から第24図は、この発明による熱電素子の製造方法の第5実施例を説明するための前半の製造工程を示す斜視図である。

第25図および第26図は、この発明による熱電素子の製造方法の第6実施例を説明するための一部の製造工程を示す斜視図である。

第27図から第29図は、この発明による熱電素子の製造方法の第7実施例を説明するための一部の製造工程を示す断面図である。

第30図および第31図は、この発明による熱電素子の製造方法の第8実施例のを説明するための一部の製造工程を示す断面図である。

第32図および第33図は、この発明による熱電素子の製造方法の第9実施例のを説明するための一部の製造工程を示す断面図である。

第34図は、熱電半導体の溝入りブロックを射出成形によって作製する場合に使用する金型の一例を示す断面図である。

発明を実施するための最良の形態

以下、この発明による熱電素子の製造方法を実施するための最良の形態としての各実施例を説明する。

〔第1実施例：第1図～第9図〕

まず、この発明による熱電素子の製造方法の第1実施例を第1図から第9図を参照して説明する。

この第1実施例では、まず第1図に示すように、n型熱電半導体ブロック1とp型熱電半導体ブロック2とを用意する。この両ブロック1と2は厚さを含む全てのサイズが同一であるのが望ましい。そして、両ブロックを区別し易くするために、n型熱電半導体ブロック1には、その全表面に斜線を施して示す。以後の各図においても同様である。

続いて第2図に示すように、溝入りブロック作製工程として第1の溝加工工程を実施し、n型熱電半導体ブロック1に一定のピッチで複数本の縦溝16を厚さ方向の一部15を残して平行に形成し、縦隔壁17を所定の間隔で形成したn型溝入りブロック11を作製する。同様にp型熱電半導体ブロック2にも、上記と同じ一定のピッチで複数本の縦溝26を厚さ方向の一部25を残して平行に形成し、縦隔壁27を所定の間隔で形成したp型溝入りブロック21を作製する。

このとき、n型溝入りブロック11とp型溝入りブロック21とを嵌合可能にするために、両ブロック11、21の縦隔壁17、27を櫛型に形成し、かつ縦溝16と26のピッチを同一にすると共に、接着用のスペースを確保するため各縦溝16、26の幅が縦隔壁17、27の幅より若干広くなるようにする。また、縦溝16と縦溝26の深さを等しくするのが望ましい。

この第1の溝加工工程におけるn型熱電半導体ブロック1およびp型熱電半導体ブロック2への縦溝16, 26の加工は、例えば、ワイヤソーを用いた研磨加工又はダイシングソーを用いた研削加工により行う。

なお、この第1実施例においては、n型熱電半導体ブロック1としてBiTeSeの焼結体を、p型熱電半導体ブロック2としてBiTeSbの焼結体を用い、大きさはともに12mm×12mm×4mmとした。そして、各溝入りブロック11, 21には、厚さ4mmに対して深さ3mmで、ピッチ寸法120μm、幅70μmの縦溝16, 26を形成しているものとする。したがって、縦隔壁17, 27の幅は50μmとなる。

この熱電半導体の溝入りブロック11, 12を作製する方法としては、上述のように機械加工によって細かい溝加工をする方法に限らず、射出成形等の成形加工によって作製することも可能であるが、その場合の溝入りブロック作製工程の例については、後で説明する。

次に、第3図に示す嵌合工程と固着工程を実施して、n型溝入りブロック11とp型溝入りブロック21で、互いに縦溝16, 26に相手側の縦隔壁27, 17を挿入し合って嵌合させ、その嵌合部の空隙に接着性のある絶縁材を充填して固着し、一体化ブロック3を形成する。

この一体化ブロック3を形成する工程は、n型溝入りブロック11とp型溝入りブロック21を嵌合させて絶縁材によって固着する工程であるが、その接着層には2つのブロックの接合の他に、n型溝入りブロック11とp型溝入りブロック21との間の電氣的絶縁性を確保する作用を持たせる必要がある。

たとえば、ワイヤソーを用いた研磨加工によって縦溝16, 26の内壁が非常に平滑に加工できた場合には、単に流動性の高い接着剤中に固着前の一体化ブロック3を部分的に浸漬し、毛細管現象により接着剤を縦溝16, 26と縦隔壁27, 1

7との隙間に充填すれば絶縁性は確保できる。

一方、縦溝16, 26の内壁がやや粗面となった場合には、確実に絶縁性を保つために、第3図の一体化ブロック3の仮想線で示した部分Aを拡大して第7図又は第8図に示すようにして絶縁性を確保する。

第7図に示す方法は、n型溝入りブロック11の縦隔壁17および縦溝16の表面に絶縁膜31を形成し、これにp型溝入りブロック21を嵌合させ、その縦隔壁27および縦溝26の表面と絶縁膜31との隙間に、接着剤を上述のように毛細管現象を利用して充填し硬化させて接着層32とし、一体化ブロック3を完成する。

絶縁膜31としては、酸化シリコン、酸化アルミニウム、窒化シリコンなどの無機膜、あるいはポリイミドなどの有機膜の何れをも用いることができる。

なお、絶縁膜31はp型溝入りブロック21の縦隔壁27および縦溝26の表面に形成してもよい。さらに、n型溝入りブロック11およびp型溝入りブロック21の双方の互いに嵌合する表面に形成すれば、一層確実に絶縁性を確保できる。

第8図に示す方法は、絶縁性スペーサ33を分散させた接着剤を用いて一体化ブロック3を作製する方法である。たとえば絶縁性スペーサ33として平均粒径8 μ mの球形のガラスビーズをエポキシ接着剤に5重量%添加する。この結果、ガラスビーズは接着層32内にほぼ均一に分散され、n型溝入りブロック11とp型溝入りブロック21とはこのガラスビーズよりなる絶縁性スペーサ33によって空間的に強制的に隔てられ、電気的な絶縁が確保されることになる。

このように、嵌合工程と固着工程を実施し、第3図に示したように完成した一体化ブロック3に対し、つぎに第4図に示すように第2の溝加工工程を実施して、横溝46を形成する。このように、一体化ブロック3に横溝46を形成した第4図に示すブロックを溝入り一体化ブロック4と称す。

横溝46の加工は、第3図によって説明した第1の溝加工工程における溝加工方

向と交差する方向に、複数本の横溝 4 6 を所定のピッチで厚さ方向の一部 4 5 を残して形成し、所定の間隔を置いて横隔壁 4 7 を形成することになる。なお、この工程での横溝 4 6 は、第 1 の溝加工工程で形成した縦溝 1 6, 2 6 と任意の角度で交差する方向に形成すればよいが、第 4 図に示すように直交させるのが最適である。

この実施例では、横溝 4 6 は第 4 図に示すように一体化ブロック 3 の p 型溝入りブロック 2 1 側の面から形成する。しかし、これとは逆に n 型溝入りブロック 1 1 側の面から形成してもよいし、あるいは、第 3 図に示した一体化ブロック 3 の前面側又は背面側から嵌合部分に形成しても構わない。

横溝 4 6 の深さは、一体化ブロック 3 での n 型溝入りブロック 1 1 と p 型溝入りブロック 2 1 の嵌合部分を切断する所まで形成するのが好ましい。

横溝 4 6 の幅は縦溝 1 6, 2 6 とは異なり、なるべく狭くするのがよい。これは次の工程で判るとおり、熱電素子としての発電能力に寄与するのは横隔壁 4 7 の部分であり、横溝 4 6 の領域をできるだけ小さくするのが素子性能面から好ましいからである。

したがって、この第 1 実施例ではピッチ $120\ \mu\text{m}$ 、幅 $40\ \mu\text{m}$ 、深さ $4\ \text{mm}$ の横溝 4 6 を形成する。なお、溝幅 $40\ \mu\text{m}$ はワイヤソー加工での溝幅としてのほぼ限界値である。

この工程に続いて、第 5 図に示す固化工程を実施する。すなわち、第 4 図に示した溝入り一体化ブロック 4 の各横溝 4 6 に絶縁性の樹脂（絶縁部材）を充填して硬化し、絶縁樹脂層 5 4 を形成する。この絶縁樹脂層 5 4 で固めたブロックを溝入り一体化ブロック 4' とする。

その後、この絶縁樹脂層 5 4 で固めた溝入り一体化ブロック 4' に対して、熱電半導体素片露出工程を実施し、前述の第 1 および第 2 の溝加工工程において溝加工されずに残された部分（第 5 図に a, b で示す厚さの部分）を、上下面からの研磨

あるいは研削によって除去し、n型熱電半導体とp型熱電半体の第3図に示した縦溝16、26と縦隔壁27、17との嵌合部分で且つ横溝46が形成された部分のみを残すように仕上げ、第6図に示す熱電素子ブロック5を得る。

この熱電素子ブロック5には、多数のn型熱電半導体素片51およびp型熱電半導体素片52が絶縁樹脂層54によって互いに絶縁されて一体に固着され、その各上下面を露出している。

最後に、第6図に示した熱電素子ブロック5のn型熱電半導体素片51とp型熱電半導体素片52を交互に電氣的に直列に接続するように、その上下面に電極を形成する電極形成工程を実施して、第9図に示す熱電素子6を得る。

第9図はその熱電素子6を真上方向から見た平面図であり、その上面側と下面側とに種々の電極を形成している。

実線の円形で示す上面電極61aと破線の円形で示す下面電極62aが、隣り合ったn型熱電半導体素片51とp型熱電半導体素片52とを直列に接続し、多数の熱電対を形成する電極である。また、L字状の上面電極61bと下面電極62bとは熱電素子80の周縁部で必要な電極で、無駄な意味はあるがn型またはp型の熱電半導体素片を並列に接続している。各熱電半導体素片51、52は接着層32および絶縁樹脂層54によって互いに絶縁されている。なお、小さい破線の円形で示す下面電極63、64は外部への電圧取り出し電極である。

これらの電極は、いずれも図5に示した熱電素子ブロック5の上面と下面とに金(Au)膜を真空蒸着法、スパッタリング法、または無電解メッキ法などにより形成し、フォトリソグラフィ技術とエッチング技術によってその金膜をパターンニングして形成する。

なお、電極を形成する熱電素子ブロック5の上面と下面とが、前述のような研削だけでは表面粗さとして問題となる場合には、ラッピングなどでより平滑な表面と

するのよく、それによって各電極の断線などの不良の発生を防止できる。

また、電極としては、金膜だけでなく他の金属膜、たとえばCu膜、Al膜、Ni膜、Fe膜、あるいはこれらの組み合わせよりなる積層膜（例えばAl/Ni膜）なども利用できる。また、電極の形成方法も、印刷法やマスク蒸着法、あるいはガラスやセラミックなどの絶縁性の板状材料にあらかじめ電極をパターンニングしておき、それを板状材料ごと張り付けるなどの方法も用いることができる。

上述してきたこの発明の第1実施例によれば、第2図及び第4図に示した第1及び第2の溝加工工程において、熱電半導体材料による非常に薄い縦隔壁17、27や横隔壁47が形成され、その隔壁はきわめて薄くて脆いことにはなるが、全体としては一体のブロックとなっており、個々の隔壁を持って移動したり重ねるなどの微妙な操作をする必要がなく、ブロック全体として操作すればよいので、従来の特開昭63-20880号公報に開示されている方法に比べて、脆弱性の問題を解決でき、且つ容易に効率よく小型で多数の熱電対を有する熱電素子を作製することができる。

また、従来の特開平8-43555号公報に開示されている方法の場合には、一体のブロックが示されているが、熱電半導体を別の基体に接着して柱状に加工しているために、依然脆さの問題が深刻で製造は困難を極める。これに対して、本発明の第1実施例によれば、常に熱電半導体を一体のブロックの状態で加工する製造方法であり、脆性材である熱電半導体材料の微細加工や組立てが容易にできるのである。したがって、小型でかつ出力電圧を大きくするために多数の熱電対を有する熱電素子を、容易にかつ効率よく製造することができる。

なお、熱電素子を構成する熱電対の数は少なくなるが、上述した第1実施例における第2の溝加工工程と、その溝加工部（第4図の横溝47）に絶縁部材を充填して固化させ、第5図の絶縁樹脂層48を形成する固化工程とを省略して、第3図に

示した一体化ブロック 3 から直接熱電半導体素片露出工程を実施してもよい。

その場合は、第 3 図に示した嵌合工程および固着工程によって作製された一体化ブロック 3 に対して、その上下面から研削加工等を行なって、n 型溝入りブロック 11 および p 型溝入りブロック 21 の縦隔壁 17、27 と縦溝 26、16 とが嵌合した部分以外の部分を除去して、n 型および p 型の熱電半導体素片を露出させた熱電素子ブロックを作製する。

その後、電極形成工程を実施して、その熱電素子ブロックの露出された n 型と p 型の熱電半導体素片 (n 型溝入りブロック 11 の縦隔壁 17 および p 型溝入りブロック 21 の縦隔壁 27 による) を交互に直列に接続する電極を、熱電素子ブロックの上面および下面に形成すれば、熱電素子を得ることができる。

〔第 2 実施例：第 10 図～第 14 図〕

次に、この発明による熱電素子の製造方法の第 2 実施例を、第 10 図～第 14 図を用いて説明する。これらの図において、前述の第 1 実施例の第 1 図～第 5 図と対応する部分には同一の符号を付している。

この第 2 実施例では、まず第 10 図に示すように、n 型熱電半導体ブロック 1 とベース 10 とを接合した n 型熱電半導体複合ブロック 12、および p 型熱電半導体ブロック 2 とベース 20 とを接合した p 型熱電半導体複合ブロック 22 とを用意する。なお、n 型熱電半導体ブロック 1 と p 型熱電半導体ブロック 2 は厚さを含む全てのサイズが等しいのが望ましい。

それぞれの熱電半導体ブロック 1、2 とベース 10、20 との接合は、接着剤あるいはワックスにより行なう。また、ベース 10、20 としてはガラス、セラミックス、プラスチック、金属など、ある程度の硬度を有する材料ならば種々のものを用いることができる。

続いて、これらの熱電半導体複合ブロック 12、22 に対して、その熱電半導体ブ

ロック 1, 2 の部分に、それぞれ第 1 実施例における第 1 の溝加工工程と同様な溝加工を実施して、第 11 図に示すように櫛型に縦溝 16, 26 と縦隔壁 17, 27 を形成し、n 型溝入り複合ブロック 13 と p 型溝入り複合ブロック 23 とを作製する。縦溝 16, 26 のピッチと幅については第 1 実施例と同じであるが、深さについてはおおむね熱電半導体ブロック 1 又は 2 とベース 10 又は 20 との界面付近までとする。すなわち、この界面の少し手前まで、丁度界面まで、あるいは少しベース 10 又は 20 に切り込むまでの何れかを状況により選択する。

その後、この n 型溝入り複合ブロック 13 と p 型溝入り複合ブロック 23 とを、互いに溝加工された面が対向するように嵌合させる嵌合工程と、その互いに嵌合された n 型溝入り複合ブロック 13 と p 型溝入り複合ブロック 23 の嵌合部の空隙に接着性のある絶縁部材を充填して固着し、第 12 図に示す一体化ブロック 3' を作製する固着工程を実施する。

次いで、この一体化ブロック 3' に対して第 13 図に示すように、第 1 実施例の第 4 図で示した第 2 の溝加工工程と同様に溝加工を施し、横溝 46 と横隔壁 47 を形成して溝入り一体化ブロック 14 を作る。このとき、横溝 46 は一方の複合ブロック側から他方の複合ブロックのベース 10 又は 20 との界面付近までの深さで、第 1 の溝加工で形成した縦溝 16, 26 および縦隔壁 17, 27 と交差する方向（この実施例では直交する方向）に形成する。

そして、第 14 図に示すように、溝加工部である横溝 46 に絶縁性の樹脂（絶縁部材）を充填して固化させる固化工程を実施し、絶縁樹脂層 54 を形成する。この絶縁樹脂層 54 で固めたブロックを溝入り一体化ブロック 14' とする。

その後、この第 14 図に示す溝入り一体化ブロック 14' に対して、上下のベース 10 及び 20 の部分を除去する熱電半導体素片露出工程を実行し、第 1 実施例の第 6 図に示したのと同じ熱電素子ブロック 5 を得る。なお、横溝 46 を形成する前

に、加工する側のベース（第13図に示した例ではベース20）を除去しておいてもよい。

さらに、この熱電素子ブロック5のn型熱電半導体素片51とp型熱電半導体素片52を交互に電氣的に直列に接続するように、その上下面に電極を形成する電極形成工程を実施すれば、第9図に示したのと同じ熱電素子6を得ることができる。

この第2実施例によれば、前述の第1実施例において、最終的に研磨して除去される熱電半導体ブロック1、2の溝加工をせずに残す部分（第2図に示した部分15、25）の代わりに、ベース10、20を用いて各縦隔壁17、27および横隔壁47を一体的に支持するようにしたことにより、熱電半導体材料の上面又は下面近傍部分も有効に利用できるため、熱電半導体材料が無駄になる部分を少なくすることができ、材料の利用効率が大幅に向上するという利点がある。

その他の効果は第1実施例と同様である。

〔第3実施例：第15図～第18図〕

つぎに、この発明による熱電素子の製造方法の第3実施例を、第15図～第18図を用いて説明する。なお、この第3実施例の前半の工程は第1図から第3図によって説明した第1実施例の工程と同様であるので、これらの図を用いて簡単に説明する。

この第3実施例では、第1図に示したn型の熱電半導体ブロック1及びp型の熱電半導体ブロック2をそれぞれ2個ずつ用意し、そのそれぞれに第2図に示したように第1の溝加工を施して、同一ピッチで複数本の深さと高さが等しい縦溝16、26及び縦隔壁17、27を平行に形成して、n型溝入りブロック11とP型溝入りブロック21を2組作製する。

この場合も、その2組のn型溝入りブロック11とP型溝入りブロック21を、後述する成形加工による溝入りブロック作製工程によつて作製することもできる。

その各n型溝入りブロック11とP型溝入りブロック21とを第3図に示したようにそれぞれ嵌合させる嵌合工程と、その嵌合部の空隙にそれぞれ接着性のある絶縁部材を充填して固着し、一体化ブロックとする第1の固着工程とを実行して2個の一体化ブロック3を作製する。

その後、2個の一体化ブロック3の一方には、第3図におけるP型溝入りブロック21側から、他方にはn型溝入りブロック11側から、それぞれ第1の溝加工工程の加工方向と交差する方向（この実施例では直交する方向）に同一ピッチで平行な複数本の溝加工を施す第2の溝加工工程を実施し、第15図に示すように、複数の深さと高さが等しい横溝46と横隔壁47を形成した一对の溝入り一体化ブロック43A、43Bを作製する。

この場合の横溝46と横隔壁47は互いに嵌合できるように、第1実施例における第2図で説明した縦溝16、26と縦隔壁17、27と同様な仕様にする。すなわち、第15図に示す溝入り一体化ブロック43Aと43Bにおいて、横溝46のピッチを同一にし、且つ横溝46の幅が横隔壁47の幅よりも広くなるようにする。

そして、この2個の溝入り一体化ブロック43Aと43Bを、第16図に示すように、互いにその横溝46と横隔壁47とを嵌合させて組み合わせる第2の嵌合工程と、その嵌合部の空隙に接着性のある絶縁部材を充填して一体化し固着する第2の固着工程とを実施する。この一体化したブロックを二重一体化ブロック44とする。

なお、この溝入り一体化ブロック43Aと43Bの接合と固着に関しては、前述した第1実施例における第3図と第7図および第8図によって説明した方法を適用する。

その後、この二重一体化ブロック44に対して熱電半導体素片露出工程を実施する。すなわち、二重一体化ブロック44の上下面から研磨あるいは研削を行なって、

第16図にdで示す厚さ部分以外の部分を除去し、n型熱電半導体とp型熱電半導体の縦溝16、26および横溝46と縦隔壁17、27および横隔壁47のすべてが嵌合している領域を残すように仕上げて、第17図に示すようにn型熱電半導体素片51とp型熱電半導体素片52とが交互に整列した熱電素子ブロック50を得る。

この実施例において、溝入り一体化ブロック43Aと43Bの一体化に際しての好ましい製造条件として、第17図に示すように、n型熱電半導体素片51とp型熱電半導体素片52とが市松模様状に規則的に配列されるようにする必要がある、そのために相互の位置合わせをする。このような位置合わせは、外形に基準面を設けて、その面を基準に治具を用いて組み合わせればよい。

このような位置合わせを行なうと、以下に説明する電極配線において、第18図に示すように電極形状や配置が統一単純化され、配線工程が容易になる。また、そればかりでなく、第9図の左右の端部にある直列接続に寄与しない熱電半導体素片が無くなることによって、熱電半導体の利用効率が向上する。

そして、第17図に示した熱電素子ブロック50のn型熱電半導体素片51とp型熱電半導体素片52を交互に電氣的に直列に接続するように、その上下面に電極を形成する電極形成工程を実施して、第18図に示す熱電素子60を得る。

第18図はその熱電素子60を真上方向から見た平面図であり、その上面側と下面側とに各電極を形成している。

熱電素子ブロック50上面に形成した実線の円形で示す上面電極61と下面に形成した破線の円形で示す下面電極62は、隣り合ったn型熱電半導体素片51とp型熱電半導体素片52とを直列に接続して多数の熱電対を形成する電極であり、下面電極63と64は外部への電圧取り出し電極である。

これらの電極61～64は、いずれも第17図に示した熱電発電素子ブロック5

0の上面と下面とに金膜を真空蒸着法、スパッタリング法、無電解メッキ法などにより形成し、フォトリソグラフィ技術とエッチング技術によって、その金膜をパターンニングして形成する。なお、この電極の材料としては、金に限らず前述した第1実施例において例示したような種々の材料を使用することができる。

また、電極61～64を形成する上面と下面とは、第1実施例と同様に、表面粗さが問題となる場合には、ラッピング法などにより平滑面とすれば断線不良を防止できる。

したがって、この第3実施例の製造方法によれば、第1または第2実施例において必要であった第9図に示したL字状の上面電極61bと下面電極62bとが不要になり、配線工程が容易で且つかつ熱電半導体材料も有効に利用できるという利点がある。

また、この第3実施例の熱電素子によれば、単位体積あたりの熱電半導体素片の数を第1あるいは第2実施例での熱電素子の約2倍にすることができるため、より小型で高出力電圧の熱電素子が得られることになる。

なお、この第3実施例の製造方法では、第15図に示した横溝46の加工の前に、第3図に示した一体化ブロック3の溝加工面側をあらかじめ削って、n型熱電半導体とp型熱電半導体の縦溝16、26及び縦隔壁17、27の嵌合部分を露出させるようにしてもよい。

このようにしてから横溝46を形成すれば、第16図に示した第2の嵌合工程を行なったときに、n型熱電半導体とp型熱電半導体の縦溝16、26及び横溝46と縦隔壁17、27及び横隔壁47とがその全体で嵌合する。そのため、熱電半導体素片露出工程において、縦隔壁17、27の高さ全体に相当する部分を残して熱電半導体素片とすることができ、結果として熱電半導体材料の利用効率が向上する。

〔第4実施例：第19図～第21図〕

次に、この発明の第4実施例を、第19図から第21図を用いて説明する。なお、この第4実施例の前半の工程は第10図から第12図によって説明した第2実施例の工程と同様であるので、これらの図を用いて簡単に説明する。

この第4実施例では、第10図に示したn型の熱電半導体ブロック1とベース10とを接合したn型の熱電半導体複合ブロック12と、p型の熱電半導体ブロック2とベース20とを接合したp型の熱電半導体複合ブロック22とを2個ずつ用意する。

そして、その各熱電半導体複合ブロック12，22に対して、第11図に示したように、そのn型の熱電半導体ブロック1およびp型の熱電半導体ブロック2の部分に、それぞれ同一ピッチで複数本の溝加工を各ベース10，20との界面付近までの深さで施す第1の溝加工工程を実施し、櫛形に縦溝16，26と縦隔壁17，27を形成し、n型溝入り複合ブロック13とP型溝入り複合ブロック23を二組作製する。なお、n型溝入り複合ブロック13の縦溝16とP型溝入り複合ブロック23の縦溝26とはその位置を1/2ピッチずらしておくことが好ましい。

このようにそれぞれ溝加工された二組のn型の熱電半導体複合ブロック13とp型の熱電半導体複合ブロック23とをそれぞれ互いにその溝加工された面が対向するように嵌合させる第1の嵌合工程と、それによって互いに嵌合された二組のn型の熱電半導体複合ブロック13とp型の熱電半導体複合ブロック23の嵌合部の空隙にそれぞれ接着性のある絶縁部材を充填して固着する第1の固着工程とを実施して、第12図に示したような一体化ブロック3'を2個作製する。

その2個の一体化ブロック3'の一方はp型の熱電半導体ブロック側のベース20を除去し、他方はn型の熱電半導体ブロック側のベース10を除去して、第19図に示すように、それぞれ上面あるいは下面にn型熱電半導体の縦隔壁17とp型

熱電半導体の縦隔壁27が露出した一対の一体化ブロック142A, 142Bとを得る。

そして、この一対の一体化ブロック142A, 142Bに、ベース10又は20を除去した側の面から、前述の第2実施例において第13図によって説明した第2の溝加工工程と同様な工程を実施して、第1の溝加工工程の加工方向と交差する方向（この実施例では直交する方向）に同一ピッチで複数本の溝加工を除去していない方のベース20又は10との界面付近までの深さで施し、複数の横溝46および横隔壁47を形成した2個の溝入り一体化ブロック143Aと143Bを作製する。なお、一方の溝入り一体化ブロック143Aの横溝46と他方の溝入り一体化ブロック143Bの横溝46とは、その位置を1/2ピッチずらして形成することが好ましい。

この2個の溝入り一体化ブロック143Aと143Bとを、互いに溝加工された面が対向するように嵌合させる第2の嵌合工程と、その互いに嵌合された2個の溝入り一体化ブロック143Aと143Bの嵌合部の空隙に接着性のある絶縁部材を充填して固着する第2の固着工程とを実施して、第21図に示す二重一体化ブロック144を得る。

この場合も、前述の第3実施例で説明したのと同様に、2個の溝入り一体化ブロック143Aと143Bを嵌合させる際に、第17図に示したようにn型熱電半導体素片51とp型熱電半導体素片52と市松模様状に配列されるように、相互の位置関係を制御する必要がある。

この位置合わせに関しては、第3実施例で説明したように、外形基準で行なうことができる。また、この第4実施例においては、ベース10および20としてガラスなどの透明部材を用いれば、顕微鏡を用いて各熱電半導体素片51, 52を直接観察しながら、精密に位置合わせを行なうこともできる。

そして、この二重一体化ブロック144のベース10および20を除去すると、第3実施例の第17図に示した熱電素子ブロック50と同様な熱電素子ブロックとなる。これに第18図で説明した電極61～64を同様に設けることによって、第18図に示した熱電素子60と同様な熱電素子が得られる。

なお、この実施例では、2個の一体化ブロック3'に第2の溝加工を行なう前に、第19図に示したようにそれぞれ横溝46の加工を施す側のベース20又は10を除去して、横溝46の加工を行った一对の溝入り一体化ブロック143Aと143Bとを嵌合したとき、その熱電半導体の全体が互いに嵌合できるようにしたので、残っている熱電半導体をすべて無駄なく熱電半導体素片として利用できる。

しかし、これは必須ではないので、ベース10又は20を除去せずに第2の溝加工（横溝加工）を行なった後に、ベース10又は20を除去するようにしてもよい。

〔第5実施例：第22図～第24図〕

次に、この発明の第5実施例について第22図から第24図を用いて説明する。

この第5実施例の製造方法では、まず、第22図に示すように、2枚の大きなベース（以下、大ベースと記す）110、120に、それぞれn型の熱電半導体ブロック1又はp型の熱電半導体ブロック2を第2実施例の場合と同様にして固着し、一对のn型熱電半導体複合ブロック91とp型熱電半導体複合ブロック92を作製する。

すなわち、この実施例で使用する大ベース110、120は、熱電半導体ブロック1、2の固着面積より大きな面積を有する。

そして、第1の溝加工工程により、第2実施例と同様にその各半導体ブロック1、2に縦溝16、26および縦隔壁17、27を形成し、第23図に示すn型溝入り複合ブロック181とp型溝入り複合ブロック182を作製する。このとき形成する縦溝16、26は、いずれも大ベース110又は120の一部に切り込む深さと

することが好ましい。これは後述する第24図で行なう嵌合工程で、n型およびp型熱電半導体を効率よく利用できるようにするように、スペーサ190の効果を引き出すためである。

そして、第24図に示すように、第23図に示したn型溝入り複合ブロック181とp型溝入り複合ブロック182とを組み合わせることで嵌合させて第1の嵌合工程を行なう。この時、大ベース110と120を利用してスペーサ190を挿入することにより、2枚の大ベース110と120との間の間隔Dを熱電半導体ブロック1, 2の厚さに相当する熱電半導体の縦隔壁17, 27の高さに正確に制御（規制）する。

たとえば、n型熱電半導体ブロック1と、p型熱電半導体ブロック2と、スペーサ190との厚さを同一にすることで、第24図に示すようにベース110と120との間の間隔Dを一定に保つことができ、n型およびp型の熱電半導体よりなる縦隔壁17, 27を凹凸無なく配列させることができる。

すなわち、このスペーサ190を用いることで、形成される縦溝26の深さに均一性がない場合でも、n型およびp型熱電半導体を互いに凹凸の無いように配列させることができ、n型およびp型熱電半導体が無駄に研磨あるいは研削されることがなくなるので、その利用効率を高めることができる。

このスペーサ190を用いた第1嵌合工程の後、n型溝入り複合ブロック181とp型溝入り複合ブロック182の嵌合部の空隙に接着性のある絶縁部材を充填して固着し、第24図に示す一体化複合ブロック193を得る。

その後、第2実施例における第13図に示した溝入り一体化ブロック14と同様に、第2の溝加工を行なって横溝および横隔壁を形成した溝入り一体化ブロックを作製し、その各横溝に絶縁性の樹脂を充填して硬化し、第14図に示した絶縁樹脂層54と同様な絶縁樹脂層を形成する。そして、各大ベース110, 120を除去

すると、第6図に示したのと同様な熱電素子ブロックが得られる。さらに、第9図に示したようにその熱電素子ブロックの上下面に各電極を形成して各熱電半導体素片を交互に直列に接続すれば、熱電素子6を得ることができる。

〔第6実施例：第25図および第26図〕

次に、上記第5実施例の一体化複合ブロックを使用するこの発明の第6実施例を第25図および第26図を用いて説明する。

この第6実施例の製造方法では、前述の第5実施例において第22図から第24図によって説明した各工程と同様にして、2個の一体化複合ブロック193を作製する。

その後、その2個の一体化複合ブロック193に対して、前述の第4実施例における第19図に示した工程と同様にして、それぞれ第2の溝加工を行なう側の大ベース110又は120を除去して、第2の溝加工（横溝加工）を行ない、第25図に示すように互いに嵌合し得る複数の横溝46と横隔壁47を形成した一对の溝付き一体化複合ブロック203A、203Bを作製する。

その後、第26図に示すように、この一对の溝付き一体化複合ブロック203Aと203Bをスペーサー190を用いて、大ベース110と120の間の間隔を一定（残っている熱電半導体の高さと同じ値）に保持して互いに嵌合させ、その嵌合部の空隙に接着性のある絶縁部材を充填して、二重一体化ブロック213を得る。

この二重一体化ブロック213の各大ベース110及び120を除去することにより、n型およびp型の熱電半導体素片51、52を露出させると、第3実施例の第17図に示したのと同様な熱電素子ブロックが得られる。

さらに、第18図に示したように、その熱電素子ブロックの上下面に電極81～84を形成して、各熱電半導体素片51、52を交互に直列に接続することにより、

熱電素子60を得ることができる。

これら第3, 第4, 第6実施例で作製した熱電素子60は12mm×12mmのブロックの外周部を除去して、10mm×10mm×2mmの大きさとした場合、熱電対が約3400対集積化される。

この熱電素子60に1.5℃の温度差を与えたところ、2.0Vの開放電圧が得られた。

このため、この熱電素子80は腕時計などの小型携帯型電子機器の中に十分に収納可能な大きさであり、かつ得られた開放電圧は腕時計を駆動するには十分な値であり、昇圧回路と組み合わせることによって種々の携帯型機器の駆動も可能である。

〔第7実施例：第27図～第29図〕

次に、この発明の第7実施例について第27図から第29図を用いて説明する。

この第7実施例の製造方法では、まず、第1実施例の第1図に示したn型熱電半導体ブロック1とp型熱電半導体ブロック2とを用意し、その各熱電半導体ブロック1, 2の少なくともベースとの接合面およびその反対側の面（後の電極形成工程において電極を形成する面）に、メッキ、蒸着あるいはスパッタなどにより、第27図に示すように金属被覆層223を形成する。こうして、被覆n型熱電半導体ブロック221と被覆p型熱電半導体ブロック222とを得る。

この金属被覆層223は、Ni（ニッケル）、Cu（銅）、Au（金）等の単一層、あるいはこれらを積層した複合層とする。この金属被覆層223を設ける目的は、後述する各種の配線用電極と熱電半導体との電気的な接続を良好にするためである。そのために、金属被覆層223形成する時あるいは形成後に適度の熱処理を施して、金属被覆層223とn型またはp型熱電半導体ブロック1, 2とのオーミックな接続をより確実にすることが望ましい。

また、金属被覆層223の厚さは、0.1～50μm程度の範囲にあればよいが、

後の工程において、被覆n型熱電半導体ブロック221と被覆p型熱電半導体ブロック222との高さの揃えを、この金属被覆層223の面を研磨工程などで若干除去して行なう場合が考えられる。そのため、金属被覆層223があまり薄すぎると研磨代が少なすぎて扱いにくくなり、また、厚すぎると応力的な問題が発生しやすくなる。したがって、好ましい厚さは2~10 μ mであり、この程度の厚さの膜の形成方法としては、電解あるいは無電解のメッキ法が最適である。

この実施例ではNiとAuの合計5 μ mの厚さの積層膜を電解メッキ法により形成するものとする。

第27図以降の工程は、第2、第4、第5、第6実施例に準じたいずれかの製造方法を選択して行なう。この第7実施例においては、ほぼ第5実施例に準じた工程をとるものとして説明していく。

このため、第28図は第23図に対応する。すなわち、大ベース110に被覆n型熱電半導体ブロック221を接合したn型熱電半導体複合ブロックと、大ベース120に被覆p型熱電半導体ブロック222を接合したp型熱電半導体複合ブロックとを用意し、ダイシングソーを用いた研削加工やワイヤーソーによる研磨加工により縦溝16、26と縦隔壁17、27を形成する。こうして被覆n型溝入り複合ブロック231と被覆p型溝入り複合ブロック232を得る。このとき、縦隔壁17、27の上下両端には金属被覆層223が金属層233となって残ることになる。

各被覆熱電半導体ブロック221、222と大ベース110又は120との接合は、接着剤あるいはワックスにより行なう。また、ベース110、120は、ガラス、セラミックス、プラスチック、金属などある程度の硬度を有する材料ならばいずれでも用いることができる。

縦溝26のピッチと幅と深さについてはほぼ第23図において説明したとおりであるが、深さについては若干異なる。この実施例の場合には被覆熱電半導体ブロッ

ク 2 2 1 または 2 2 2 と大ベース 1 1 0 又は 1 2 0 との界面丁度までか、さらに少し大ベース 1 1 0 又は 1 2 0 に切り込むまでのいずれかで縦溝 2 6 を形成する。

このようにする理由は、被覆 n 型溝入り複合ブロック 2 3 1 と被覆 p 型溝入り複合ブロック 2 3 2 との組み合わせ工程の際に、両ブロックの金属層 2 3 3 同志が同一面を形成できるようにするためである。

続いて、第 5 実施例の第 2 4 図によって説明したのと同様に、この被覆 n 型溝入り複合ブロック 2 3 1 と被覆 p 型溝入り複合ブロック 2 3 2 とを組み合わせさせて嵌合させ、その嵌合部の空隙に接着性のある絶縁部材を充填し、第 2 9 図に示す接着層 3 2 を形成して固着した一体化複合ブロックを得る。

その後、その一体化複合ブロックに第 2 の溝加工を行なって横溝および横隔壁を形成した溝入り一体化ブロックを作製し、その各横溝に絶縁性の樹脂を充填して硬化し、第 5 図に示した絶縁樹脂層 5 4 と同様な絶縁樹脂層を形成する。

そして、各大ベース 1 1 0, 1 2 0 を除去して、第 6 図に示したような熱電素子ブロックを得る。さらに、その熱電素子ブロックの上下面に第 2 9 図に示すように各電極 8 1, 8 2 を形成して n 型熱電半導体素片 5 1 と p 型熱電半導体素片 5 2 を交互に直列に接続すれば、熱電素子 8 0 を得ることができる。

第 2 9 図は、この第 7 実施例の熱電素子 8 0 の断面形状であり、第 9 図、第 1 8 図の平面図に対応するものである。ここで、上面電極 8 1 と下面電極 8 2 としては通常は既に述べたような蒸着膜などを用いるが、この実施例での特徴は銀ペーストのような導電性ペーストを用いることができる。

一般に、導電性ペーストとこの発明で用いるような半導体との電氣的な接続は、接触抵抗が高くなって問題となりやすいため、導電性ペーストはこの発明のような構成においては配線用電極には適さない。しかしながら、この第 7 実施例で示すように金属層 2 3 3 を設けることにより、このような接触抵抗を無視できるレベルま

で低減でき、導電性ペーストを上面電極 8 1 や下面電極 8 2 として使用できる。

このように導電性ペーストが使用できると、スクリーン印刷によるパターンニングで電極を形成できるため、生産性が非常に高くなる利点がある。

〔第 8 実施例：第 3 0 図および第 3 1 図〕

次に、この発明の第 8 実施例について第 3 0 図および第 3 1 図を用いて説明する。

この第 8 実施例の製造方法の説明の出発点は、第 1 ～第 5 実施例で示した配線工程の前の段階の熱電素子ブロック（例えば、第 6 図に示した熱電素子ブロック 5）である。したがって、ここまでの各工程は上記各実施例の場合と同様である。

このような熱電素子ブロックを形成した後、上述の第 7 実施例の場合と同様な金属層 2 3 3 を n 型熱電半導体素片 5 1 および p 型熱電半導体素片 5 2 の少なくとも配線電極形成面に形成する。

これにより、第 3 0 図に断面図として示すような熱電素子ブロック 2 5 3 を得る。

この実施例における金属層 2 3 3 の形成方法としては、メッキ法が好ましく、Ni、Au、Cu などの単層膜やこれらの積層膜を形成する。とくに、熱電半導体素片 5 1、5 2 の面と接着層 3 2 及び絶縁樹脂層 5 4 の面とで触媒となる Pd（パラジウム）の付着率に選択性があることを利用して、熱電半導体素片 5 1、5 2 の露出面への選択的なメッキを行なえる無電解メッキ法が最適である。

なお、出発点となる配線工程前の熱電素子ブロック（例えば第 6 図に示した熱電素子ブロック 5）の最外周部の熱電半導体素片の側面にはこの金属層 2 3 3 を形成しないのが好ましい。そのため、この実施例では、熱電素子ブロックの外周面（側面）に接着層 3 2 又は絶縁樹脂層 5 4 と同じ材質による被覆層 2 5 4 形成している。

第 3 1 図は、第 3 0 図に示した熱電素子ブロック 2 5 3 に第 7 実施例で述べたように、導電性ペーストを用いて上面電極 8 1 と下面電極 8 2 を形成し、熱電素子 8 0 として完成したものである。

このように金属膜233を後から形成しても、第7実施例と同様に導電性ペーストを使用でき、スクリーン印刷によるパターンニングで電極を形成できるので、生産性が非常に高くなる利点がある。

〔第9実施例：第32図および第33図〕

次に、この発明の第9実施例について第32図および第33図を用いて説明する。

第32図に示すのはこの第9実施例によって作製した仮熱電素子270であり、これは上述してきた各実施例で説明した熱電素子6, 60, 80と概ね同じ物であり、工程的にも殆ど同じ工程で作製される。ただし、前述の各実施例における接着層32及び絶縁樹脂層54に代わって仮固定層271を設けている。

これまでの実施例では、接着層32及び絶縁樹脂層54を最終的な熱電素子の構成要素の一部としたのに対し、この第9実施例では、この絶縁樹脂層54の部分を取り除いたものを最終的な熱電素子の構成要素とする。

したがって、接着層32及び絶縁樹脂層54に代わって、n型熱電半導体素片51とp型熱電半導体素片52を仮固定し、後で除去可能な仮固定層271を形成する。この仮固定層271の形成は、接着層32及び絶縁樹脂層54の形成と同様に、対の溝入りブロックの嵌合工程後の嵌合部の空隙、および第4図、第13図等にした横溝47を形成した後その溝47への仮固定材料の充填により行なう。その仮固定材料としては、接着性があり且つ熱あるいは溶剤により除去可能なワックスなどを用いる。

この第9実施例の製造工程は、第32図に示した仮熱電素子270の上下面全体に第33図に示すようにエポキシ樹脂などの接着性のある樹脂を塗布して絶縁固定層284を形成し、その仮熱電素子270を放熱板281と吸熱板282とによって挟んで絶縁固定層284により一体化して固定する。

この放熱板281と吸熱板282としては、熱伝導度のよい物質すなわち金属や

セラミックスを用いる。

特に金属を選んだ場合、絶縁固定層 284 を薄くすると上面電極 81 や下面電極 82 と放熱板 281 や吸熱板 282 との間の事故的な短絡の恐れが生じることがあるため、金属表面に絶縁性の酸化膜を形成するような処理を行なうとよい。

そして、第 33 図に示すように、仮熱電素子 270 を放熱板 281 および吸熱板 282 に固定した後、仮固定層 271 を熱あるいは溶剤により除去し、この領域を空隙 283 にした熱電素子 280 を得る。

この実施例の熱電素子 280 の構造によれば、空隙 283 内の空気は熱伝導率が極めて小さいため、放熱板 281 側と吸熱板 282 側との間の熱電半導体以外による熱伝導が大幅に抑制されて、熱電素子としての性能が向上する。

なお、上述の実施例では、n 型と p 型の熱電半導体の溝入りブロックの嵌合部に設ける接着層 32 と、その対の溝入りブロックを一体化した後形成する横溝に設ける絶縁樹脂層 54 の両方に代えて仮固定層 271 を設けたが、そのいずれか一方のみを仮固定層 271 に代えて、仮熱電素子 270 を放熱板 281 と吸熱板 282 とによって挟んで絶縁固定層 284 により一体化して固定した後、その仮固定層 271 を除去して、接着層 32 又は絶縁樹脂層 54 が残るようにしてもよい。

このようにすることにより、熱電素子としての性能を向上させながら、十分な強度を保つことが可能になる。

また、第 33 図の熱電素子 280 は、これを発電用として使用する場合には吸熱板 282 が低温側となる。

[熱電半導体の溝入りブロック作製工程の他の例：第 34 図]

ここで、熱電半導体の溝入りブロック作製工程の他の例を第 34 図によって説明する。

前述の第 1 実施例あるいは第 3 実施例では、n 型および p 型の熱電半導体の溝入

りブロック作製工程では、n型およびp型の熱電半導体ブロック1および2に、ワイヤーソーなどを使用する機械加工によって複数の溝を平行に形成して、n型溝入ブロック11およびp型溝入りブロック21を作製した。

しかし、このn型溝入ブロック11およびp型溝入りブロック21を、溝入りブロックの成型型（金型）を使用して、n型の熱電半導体材料とp型の熱電半導体材料を個別に成形した後、それを焼結して作製することもできる。

この溝入りブロック作製工程では、まず、平均粒径1 μ m程度の熱電半導体材料の微粉末（p型の例では、第1実施例と同じBiTeSb結晶の微粉末）に対して、有機バインダとして、例えば、エチレン酢酸ビニル／ポリブチルメタクリレート／ポリスチレン共重合体、アタクチックポリプロピレン、パラフィンワックス、フタル酸ジブチルからなる混合物を添加し、加圧ニーダーにて混練して射出成形用組成物を作成する。微粉末と有機バインダとの混合比は、微粉末100重量部に対して有機バインダ5～15重量部程度が適当である。

このようにして作製した射出成形用組成物を射出成形機を用いて成形するが、この時の金型の断面図を第34図に示す。

ここで、射出成形用組成物は、ノズル304から固定金型303のスプール306および中間金型302のゲート307を通して、可動金型301に溝入ブロックの形状に形成された金型成形部308に加圧して充填される。

こうして、金型成形部308に形成された成形体は、可動金型301を中間金型302から移動分離させた後に、エジェクタピン305で押し出して取り出す。金型成形部308の寸法は成形体の焼結による収縮を考慮して、溝入りブロックの寸法に対して約20%大きく設計する。

その成形体をアルミナ製の平板上に並べ、真空炉中で400℃で1時間保持して有機バインダをほぼ除去した仮焼結体を得る。最後に、やはりアルミナ製の平板上

に仮焼結体を並べ、これを水素フロー雰囲気電気炉中にて、470℃の温度で3時間の焼成を行ってn型又はp型の熱電半導体よりなる焼結体を得る。この焼結体が前述のn型溝入りブロック11又はp型溝入りブロック21である。

〔補足説明〕

以上、熱電素子の製造方法の様々な実施例について述べてきたが、いずれも熱電半導体素片51、52が全てマトリックス状に並列された構造を前提としてきた。すなわち、縦溝加工のあとに必ず横溝加工を施し、その後に熱電半導体素片露出工程を行ない、さらに配線などの電極を形成して熱電素子を完成していた。

しかしながら、熱電対の数が比較的少なくても利用可能である場合には、上述した各実施例において、横溝加工を実施することなく熱電半導体素片露出工程を行ない、配線などの電極を形成して熱電素子として完成させてもよい。

このような工程を行った場合には、n型とp型の熱半導体の薄い層が交互に配列され、その各層が直列接続された構造の熱電素子が得られることになる。

この本発明による熱電素子の製造方法が、このような構造の熱電素子に対しても十分に有効であることは明白である。

また、上述した各実施例の説明では、縦溝や横溝の加工をワイヤソー又はダイシングソーで加工すると説明したが、ワイヤソーを用いる研磨加工によって溝加工を行なう場合には、実際には縦溝や横溝の底面は円弧状になる。

そしてn型溝入りブロックとp型溝入りブロックとを組み合わせるときの場合は、縦溝の底面が円弧状で縦隔壁の先端部が矩形状であっても、その間に接着層の接着剤が充填されるので特に問題を生じない。

さらに、一体化ブロック形成後、横溝を形成するときにワイヤソーを用いると、その底面は円弧状となるが、横溝に絶縁性樹脂を充填するため、これもなんら問題を生じない。

したがって、以上の説明で明らかなように、この発明の熱電素子の製造方法によれば、熱電半導体部材に精密な機械加工あるいは熱電半導体材料による精密な成形加工を行なって、 n 型及び p 型の熱電半導体の溝入りブロックを作製し、それを組み合わせて嵌合させて一体化する工程により、熱電半導体部材を常に一つの塊（ブロック）として扱うので、熱電半導体を薄い板状に形成する工程や細かい溝入れ加工により熱電半導体を剣山状にする工程などのような熱電半導体材料の破損が起こりやすい加工を行わずに、多数の熱電半導体素片からなる熱電対を有する熱電素子を作製することができる。

したがって、超小型で高出力電圧の熱電発電素子を容易かつ効率的に作製でき、腕時計などの携帯型電子機器において温度差発電が利用できるようになる。

産業上の利用可能性

この発明による熱電素子の製造方法によれば、超小型で多数の熱電対を形成した高出力電圧の熱電素子を容易かつ効率的に作製できる。そのため、その熱電素子を小型の熱電発電装置として使用すれば高い出力電圧が得られるようになるので、腕時計などの小型の携帯型電子機器に内蔵して、温度差発電による電源として使用することが可能になる。

また、この熱電素子を用いて小型の高性能な冷却装置を作製することもでき、ポータブルな冷蔵庫あるいはレーザや集積回路などの局部冷却器として極めて有用である。

請求の範囲

1. それぞれ厚さ方向の一部を残して同一ピッチで複数本の溝が平行に形成された n 型の熱電半導体の溝入りブロックおよび p 型の熱電半導体の溝入りブロックを製作する溝入りブロック作製工程と、

該工程によってそれぞれ作製された n 型の熱電半導体の溝入りブロックと p 型の熱電半導体の溝入りブロックとを互いにその溝を形成した面が対向するように嵌合させる嵌合工程と、

該工程によって互いに嵌合された前記 n 型の熱電半導体の溝入りブロックと p 型の熱電半導体の溝入りブロックの嵌合部の空隙に接着性のある絶縁部材を充填して固着し、一体化ブロックを形成する固着工程と、

該工程によって形成された一体化ブロックにおける前記 n 型の熱電半導体と p 型の熱電半導体とが互いに嵌合している嵌合部以外の部分を除去して、n 型および p 型の熱電半導体素片を露出させる熱電半導体素片露出工程と、

を有することを特徴とする熱電素子の製造方法。

2. それぞれ厚さ方向の一部を残して同一ピッチで複数本の溝が平行に形成された n 型の熱電半導体の溝入りブロックおよび p 型の熱電半導体の溝入りブロックを製作する溝入りブロック作製工程と、

該工程によってそれぞれ作製された n 型の熱電半導体の溝入りブロックと p 型の熱電半導体の溝入りブロックとを互いにその溝を形成した面が対向するように嵌合させる嵌合工程と、

該工程によって互いに嵌合された前記 n 型の熱電半導体の溝入りブロックと p 型の熱電半導体の溝入りブロックの嵌合部の空隙に接着性のある絶縁部材を充填して固着し、一体化ブロックを形成する固着工程と、



該固着工程で形成された一体化ブロックに、前記溝入りブロック作製工程によって形成された溝の方向と交差する方向に複数本の溝加工を厚さ方向の一部を残して施す第2の溝加工工程と、

該工程における溝加工部に接着性のある絶縁部材を充填し固化させる固化工程と、
該工程において絶縁部材を充填し固化させた一体化ブロックにおける前記n型の熱電半導体とp型の熱電半導体とが互いに嵌合している嵌合部以外の部分を除去して、n型およびp型の熱電半導体素片を露出させる熱電半導体素片露出工程と、
を有することを特徴とする熱電素子の製造方法。

3. それぞれ厚さ方向の一部を残して同一ピッチで複数本の溝が平行に形成されたn型の熱電半導体の溝入りブロックおよびp型の熱電半導体の溝入りブロックを二組作製する溝入りブロック作製工程と、

該工程によってそれぞれ作製された二組のn型の熱電半導体の溝入りブロックとp型の熱電半導体の溝入りブロックとを、各組ごとに互いにその溝を形成した面が対向するように嵌合させる第1の嵌合工程と、

該工程によって互いに嵌合された二組のn型の熱電半導体の溝入りブロックとp型の熱電半導体の溝入りブロックの嵌合部の空隙にそれぞれ接着性のある絶縁部材を充填して固着し、2個の一体化ブロックとする第1の固着工程と、

その2個の一体化ブロックのそれぞれに前記溝入りブロック作製工程で形成された溝の方向と交差する方向に同一ピッチで複数本の溝加工を厚さ方向の一部を残して施し、2個の溝入り一体化ブロックとする溝加工工程と、

その2個の溝入り一体化ブロックを互いに溝加工された面が対向するように嵌合させる第2の嵌合工程と、

該工程によって互いに嵌合された2個の溝入り一体化ブロックの嵌合部の空隙に接着性のある絶縁部材を充填して固着し、第2の一体化ブロックとする第2の固着



工程と、

その第2の一体化ブロックの前記嵌合部以外の厚さ部分を除去して、n型およびp型の熱電半導体素片を露出させる熱電半導体素片露出工程と、
を有することを特徴とする熱電素子の製造方法。

4. 請求の範囲第1項乃至第3項のいずれか一項に記載の熱電素子の製造方法において、

前記溝入りブロック作製工程が、n型の熱電半導体ブロックおよびp型の熱電半導体ブロックに、それぞれ同一ピッチで複数本の溝加工を厚さ方向の一部を残して施す溝加工によって、前記n型の熱電半導体の溝入りブロックおよび前記p型の熱電半導体の溝入りブロックを作製する工程である熱電素子の製造方法。

5. 請求の範囲第1項乃至第3項のいずれか一項に記載の熱電素子の製造方法において、

前記溝入りブロック作製工程が、それぞれ溝入りブロックの成型型を用いて、n型の熱電半導体材料とp型の熱電半導体材料を個別に成形した後焼結することによって、前記n型の熱電半導体の溝入りブロックおよび前記p型の熱電半導体の溝入りブロックを作製する工程である熱電素子の製造方法。

6. 請求の範囲第1項乃至第5項のいずれか一項に記載の熱電素子の製造方法において、前記熱電半導体素片露出工程後に、前記露出されたn型とp型の熱電半導体素片を交互に直列に接続する電極を形成する電極形成工程を有することを特徴とする熱電素子の製造方法。

7. n型の熱電半導体ブロックとベースとを接合したn型の熱電半導体複合ブロックと、p型の熱電半導体ブロックとベースとを接合したp型の熱電半導体複合プロ



ックとを用意し、その各熱電半導体複合ブロックに対して、前記n型の熱電半導体ブロックおよびp型の熱電半導体ブロックに、それぞれ同一ピッチで複数本の溝加工を前記各ベースとの界面付近までの深さで施す第1の溝加工工程と、

該工程においてそれぞれ溝加工されたn型の熱電半導体複合ブロックとp型の熱電半導体複合ブロックとを互いにその溝加工された面が対向するように嵌合させる嵌合工程と、

該工程にによって互いに嵌合された前記n型の熱電半導体複合ブロックとp型の熱電半導体複合ブロックの嵌合部の空隙に接着性のある絶縁部材を充填して固着し、一体化ブロックを形成する固着工程と、

該固着工程で形成された一体化ブロックに、前記第1の溝加工工程における溝加工方向と交差する方向に複数本の溝加工を、前記ベースとの界面付近までの深さで施す第2の溝加工工程と、

該工程における溝加工部に絶縁部材を充填し固化させる固化工程と、

該工程において絶縁部材を充填し固化させた一体化ブロックにおける前記各ベースの部分除去して、n型およびp型の熱電半導体素片を露出させる熱電半導体素片露出工程と、

を有することを特徴とする熱電素子の製造方法。

8. 請求の範囲の第7項記載の熱電素子の製造方法において、

前記n型の熱電半導体複合ブロックとp型の熱電半導体複合ブロックの前記各ベースとして、前記熱電半導体ブロックの固着面より大きな面積を有するものを用い、

前記嵌合工程において、前記n型の熱電半導体複合ブロックとp型の熱電半導体複合ブロックのそれぞれ熱電半導体ブロックが存在しない部分のベース間にスペーサを介挿し、該ベース間の間隔を略前記熱電半導体ブロックの厚さに相当する間隔に制御することを特徴とする熱電素子の製造方法。



9. n型の熱電半導体ブロックとベースとを接合したn型の熱電半導体複合ブロックと、p型の熱電半導体ブロックとベースとを接合したp型の熱電半導体複合ブロックとを2個ずつ用意し、その各熱電半導体複合ブロックに対して、前記n型の熱電半導体ブロックおよびp型の熱電半導体ブロックに、それぞれ同一ピッチで複数本の溝加工を前記各ベースとの界面付近までの深さで施す第1の溝加工工程と、

該工程においてそれぞれ溝加工された二組のn型の熱電半導体複合ブロックとp型の熱電半導体複合ブロックとをそれぞれ互いにその溝加工された面が対向するように嵌合させる第1の嵌合工程と、

該工程によって互いに嵌合された二組の前記n型の熱電半導体複合ブロックとp型の熱電半導体複合ブロックの嵌合部の空隙にそれぞれ接着性のある絶縁部材を充填して固着し、2個の一体化ブロックを形成する第1の固着工程と、

その2個の一体化ブロックのそれぞれに前記第1の溝加工工程の加工方向と交差する方向に同一ピッチで複数本の溝加工を前記ベースとの界面付近までの深さで施し、2個の溝入り一体化ブロックとする第2の溝加工工程と、

その2個の溝入り一体化ブロックを互いに溝加工された面が対向するように嵌合させる第2の嵌合工程と、

該工程によって互いに嵌合された2個の溝入り一体化ブロックの嵌合部の空隙に接着性のある絶縁部材を充填して固着し、第2の一体化ブロックとする第2の固着工程と、

その第2の一体化ブロックにおける前記各ベースの部分を除くして、n型およびp型の熱電半導体素片を露出させる熱電半導体素片露出工程と、

を有することを特徴とする熱電素子の製造方法。

10. 請求の範囲の第9項記載の熱電素子の製造方法において、

前記n型の熱電半導体複合ブロックとp型の熱電半導体複合ブロックの前記各ベ



ースとして、前記熱電半導体ブロックの固着面より大きな面積を有するものを用い、

前記第1の嵌合工程において、互いに嵌合させる前記n型の熱電半導体複合ブロックとp型の熱電半導体複合ブロックのそれぞれ熱電半導体ブロックが存在しないベース間にスペーサを介挿し、該ベース間の間隔を略前記熱電半導体ブロックの厚さに相当する間隔に制御し、

前記第2の嵌合工程において、互いに嵌合させる前記2個の溝入り一体化ブロックのそれぞれ熱電半導体ブロックが存在しない部分のベース間にスペーサを介挿し、該ベース間の間隔を略前記熱電半導体ブロックの厚さに相当する間隔に制御することを特徴とする熱電素子の製造方法。

11. 請求の範囲第7項乃至第10項に記載の熱電素子の製造方法において、

前記熱電半導体素片露出工程後に、前記露出されたn型とp型の熱電半導体素片を交互に直列に接続する電極を形成する電極形成工程を有することを特徴とする熱電素子の製造方法。

12. 請求の範囲第1項、第2項又は第7項のいずれか一項に記載の熱電素子の製造方法において、

前記各嵌合工程において、前記互いに嵌合させる対のブロックの少なくとも一方の嵌合面に絶縁膜を形成することを特徴とする熱電発電素子の製造方法。

13. 請求の範囲第1項、第2項又は第7項のいずれか一項に記載の熱電素子の製造方法において、

前記固着工程において、前記嵌合部の空隙に充填する絶縁部材が、絶縁性スペーサを分散した接着性のある絶縁部材であることを特徴とする熱電素子の製造方法。

14. 請求の範囲第3項又は第9項記載の熱電素子の製造方法において、



前記第1の嵌合工程および第2の嵌合工程の少なくとも一方において、互いに嵌合させる対のブロックの少なくとも一方の嵌合面に絶縁膜を形成することを特徴とする熱電発電素子の製造方法。

15. 請求の範囲第3項又は第9項記載の熱電素子の製造方法において、

前記第1の固着工程および第2の固着工程の少なくとも一方において、前記嵌合部の空隙に充填する絶縁部材が、絶縁性スペーサを分散した接着性のある絶縁部材であることを特徴とする熱電素子の製造方法。

16. 請求の範囲第7項乃至第10項に記載の熱電素子の製造方法において、

前記n型の熱電半導体ブロックと前記前記p型の熱電半導体ブロックを、それぞれ前記ベースに接合する前に、その各熱電半導体ブロックの前記ベースとの接合面およびその反対側の面にそれぞれ金属被覆層を形成することを特徴とする熱電素子の製造方法。

17. 請求の範囲第16項に記載の熱電素子の製造方法において、

前記熱電半導体素片露出工程後に、前記露出されたn型とp型の熱電半導体素片を交互に直列に接続する電極を、前記金属被覆層上に導電性ペーストを用いて形成する電極形成工程を有することを特徴とする熱電素子の製造方法。

18. 請求の範囲第1項、第2項、第3項、第7項、第9項のいずれか一項に記載の熱電素子の製造方法において、

前記熱電半導体素片露出工程後に、前記露出されたn型とp型の熱電半導体素片の各電極形成面に金属層を形成する金属層形成工程と、その金属層上に前記n型とp型の熱電半導体素片を交互に直列に接続する電極を形成する電極形成工程とを有することを特徴とする熱電素子の製造方法。



19. 請求の範囲第18項記載の熱電素子の製造方法において、

前記電極形成工程において、前記電極を導電性ペーストを用いて形成することを特徴とする熱電素子の製造方法。

20. 請求の範囲第1項記載の熱電素子の製造方法において、

前記固着工程において、嵌合部の空隙に充填する絶縁部材として熱あるいは溶剤で除去可能なものを使用して仮固定層を形成し、

前記熱電半導体素片露出工程後に、前記露出されたn型とp型の熱電半導体素片を交互に直列に接続する電極を形成して仮熱電素子とする電極形成工程と、

その仮熱電素子の前記電極の形成面の一方側に放熱板を他方側に吸熱板をそれぞれ絶縁固定層を介して固定する工程と、

該工程の後に前記仮固定層を加熱するか溶剤を用いて除去する工程とを有することを特徴とする熱電素子の製造方法。

21. 請求の範囲第2項又は第7項に記載の熱電素子の製造方法において、

前記固着工程で前記嵌合部に充填する絶縁部材、および前記固化工程で前記溝加工部に充填する絶縁部材部の少なくとも一方として、熱あるいは溶剤で除去可能なものを使用して仮固定層を形成し、

前記熱電半導体素片露出工程後に、前記露出されたn型とp型の熱電半導体素片を交互に直列に接続する電極を形成して仮熱電素子とする電極形成工程と、

その仮熱電素子の前記電極の形成面の一方側に放熱板を他方側に吸熱板をそれぞれ絶縁固定層を介して固定する工程と、

該工程の後に前記仮固定層を加熱するか溶剤を用いて除去する工程とを有することを特徴とする熱電素子の製造方法。

22. 請求の範囲第3項又は第9項に記載の熱電素子の製造方法において、



前記固第1の固着工程又は第2の固着工程においてそれぞれ前記嵌合部に充填する絶縁部材として、熱あるいは溶剤で除去可能なものを使用して仮固定層を形成し、

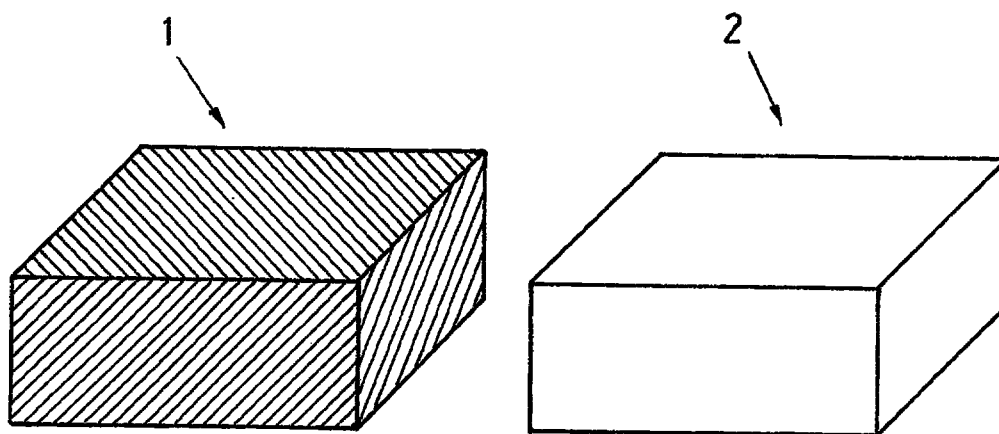
前記熱電半導体素片露出工程後に、前記露出されたn型とp型の熱電半導体素片を交互に直列に接続する電極を形成して仮熱電素子とする電極形成工程と、

その仮熱電素子の前記電極の形成面の一方側に放熱板を他方側に吸熱板をそれぞれ絶縁固定層を介して固定する工程と、

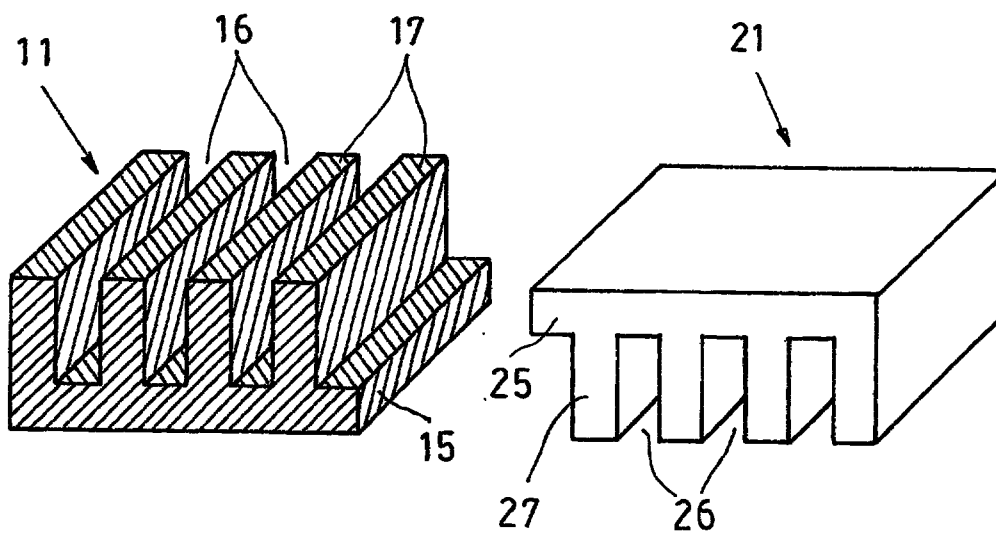
該工程の後に前記仮固定層を加熱するか溶剤を用いて除去する工程とを有することとを特徴とする熱電素子の製造方法。



第1図

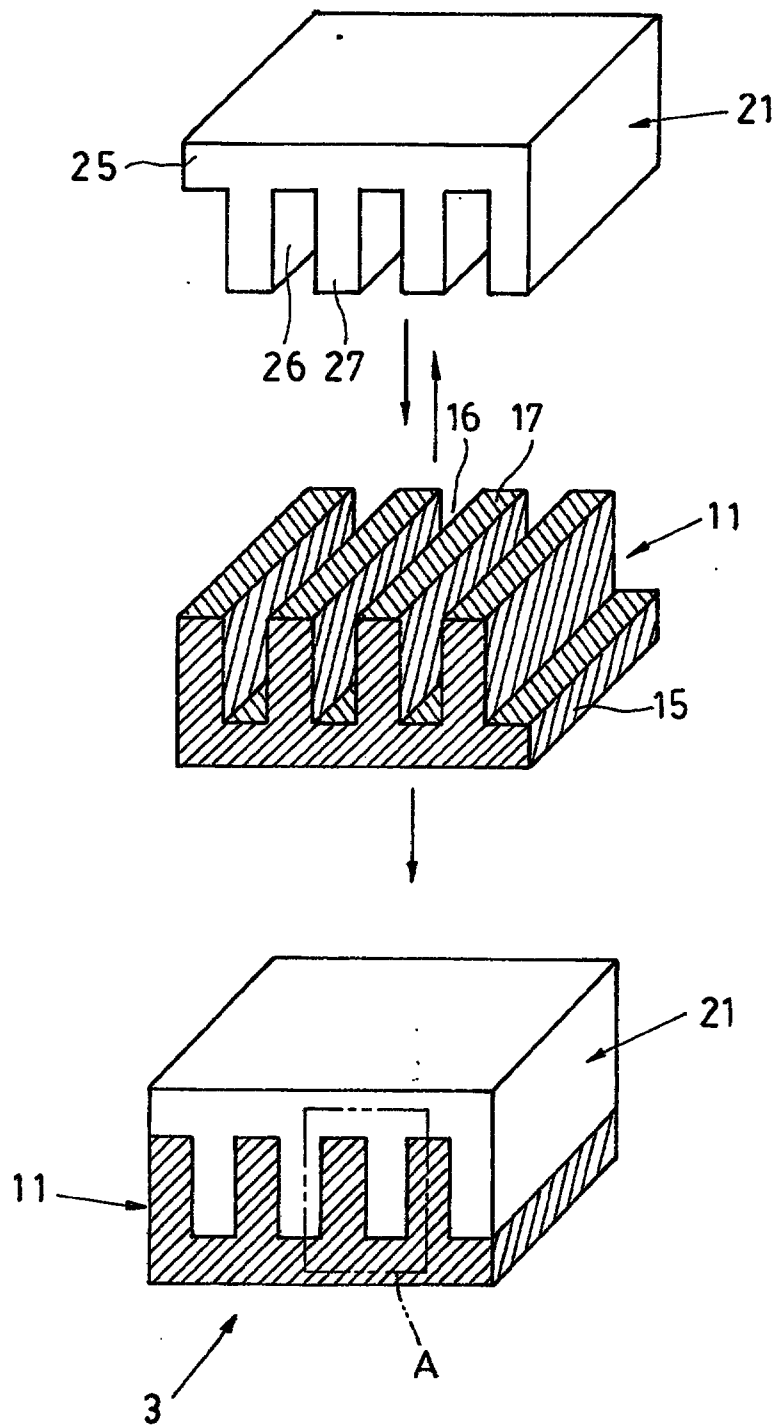


第2図



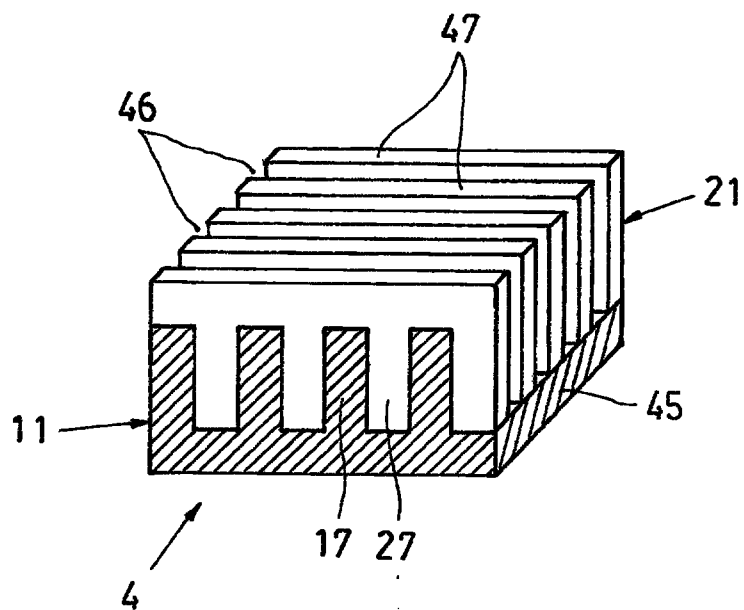
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第3図

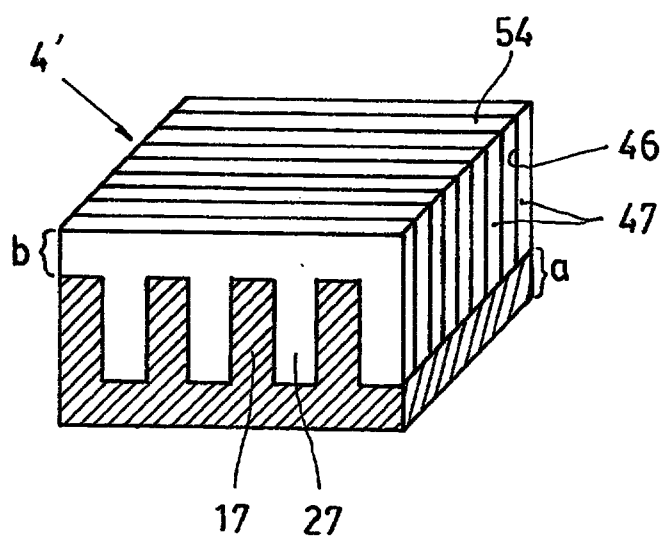


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第4図

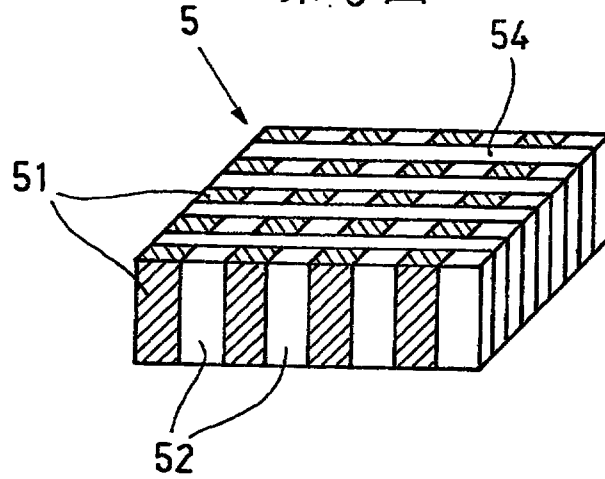


第5図

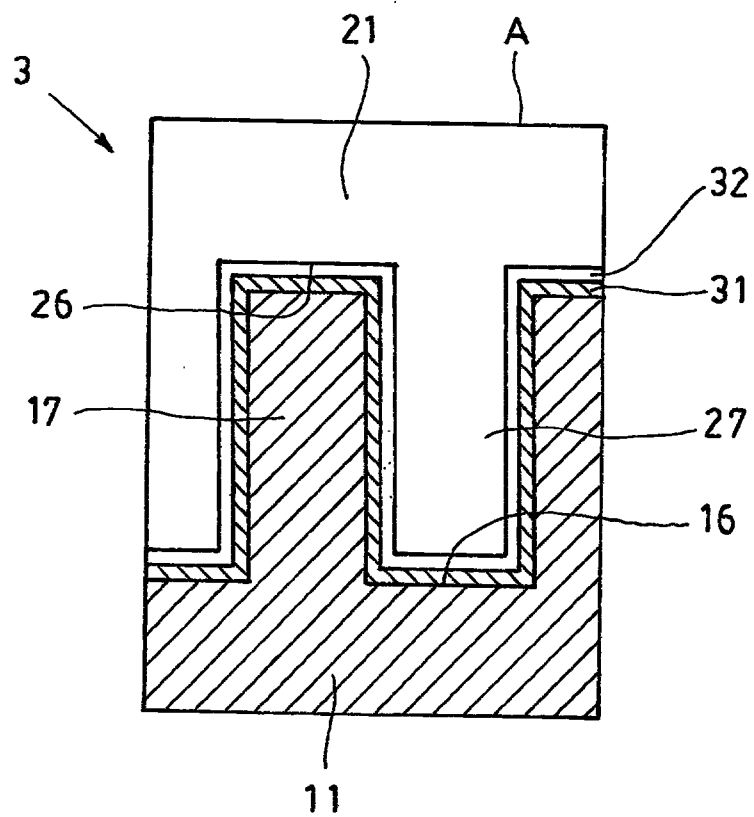


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第6図

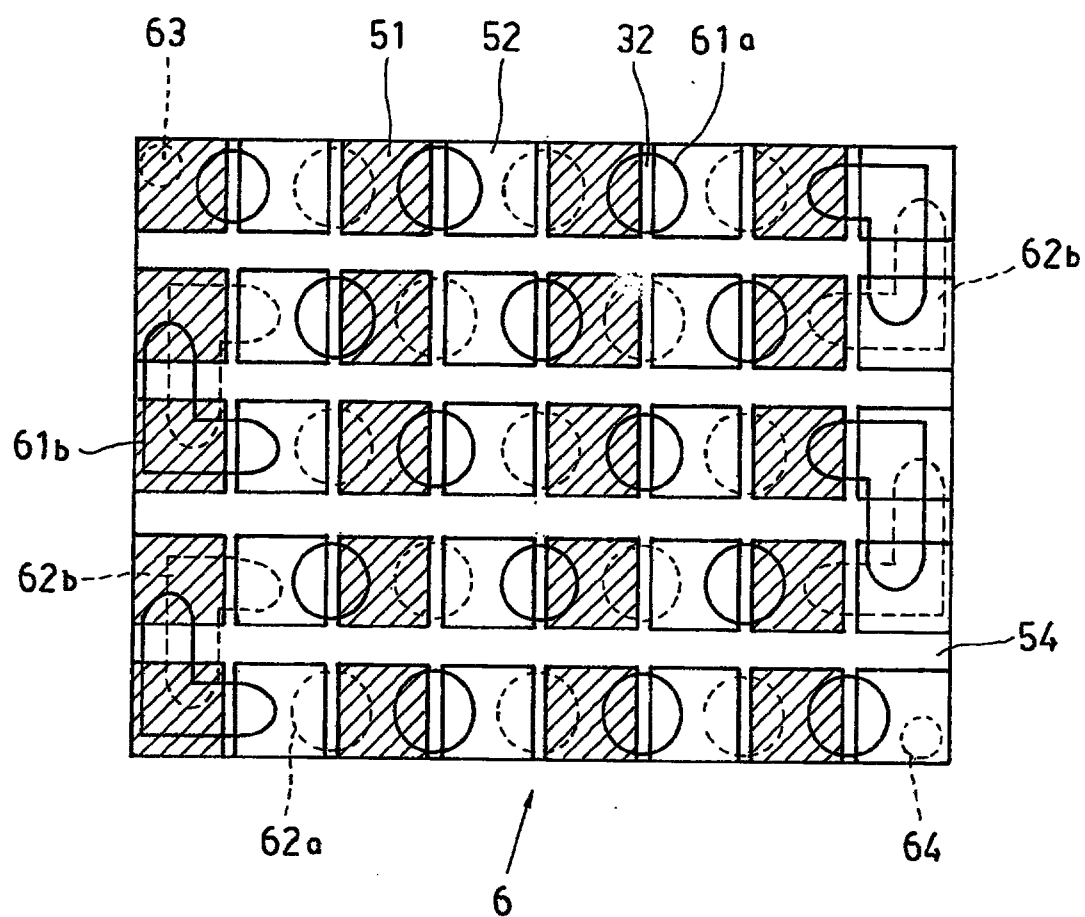


第7図



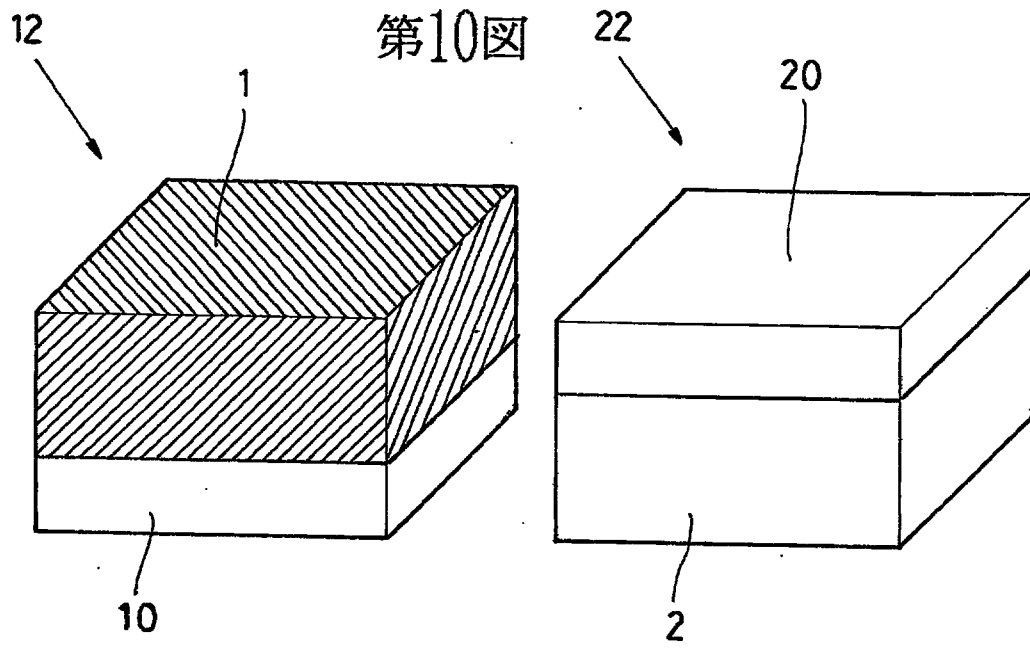
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第9図

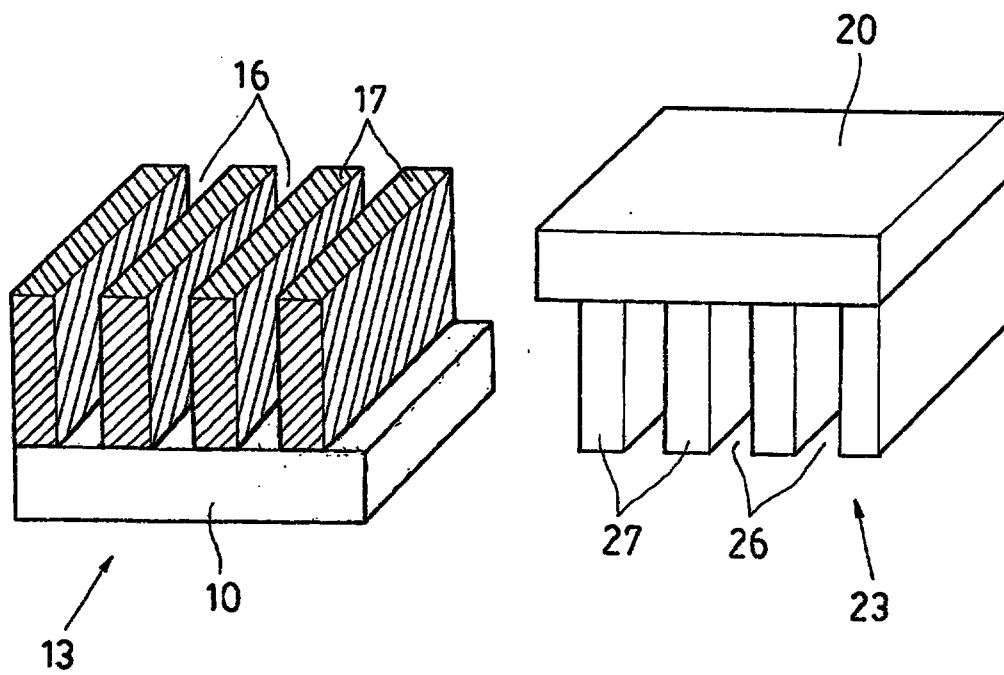


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第10図

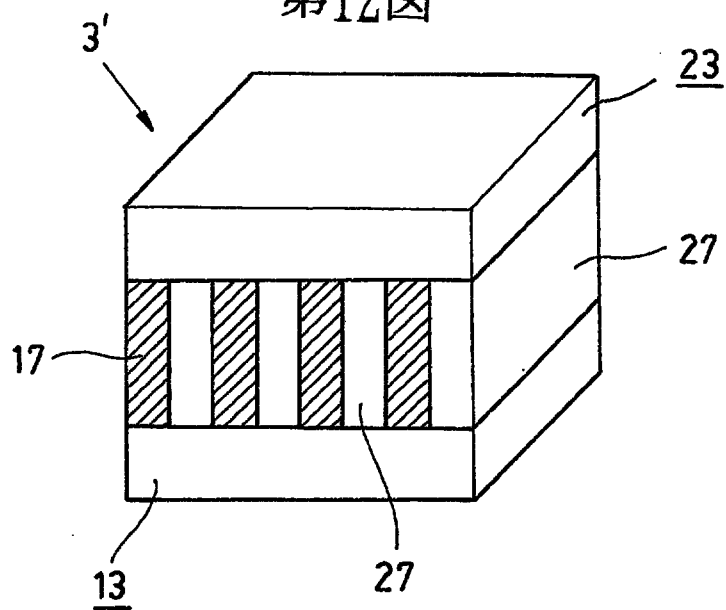


第11図

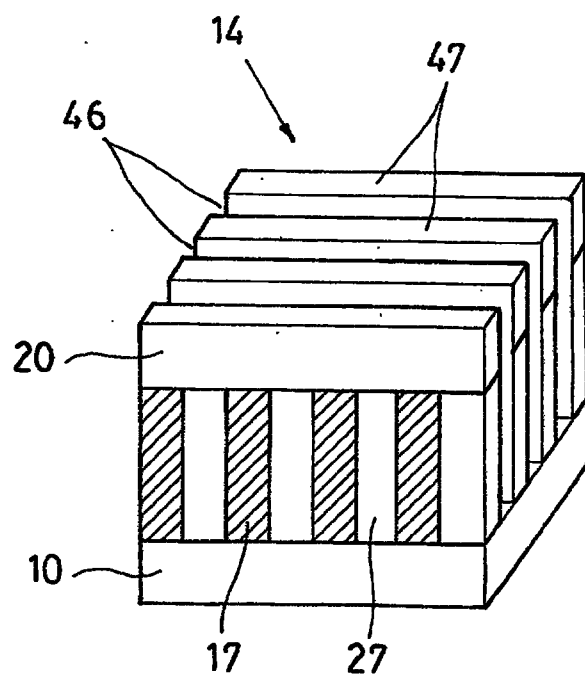


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第12図

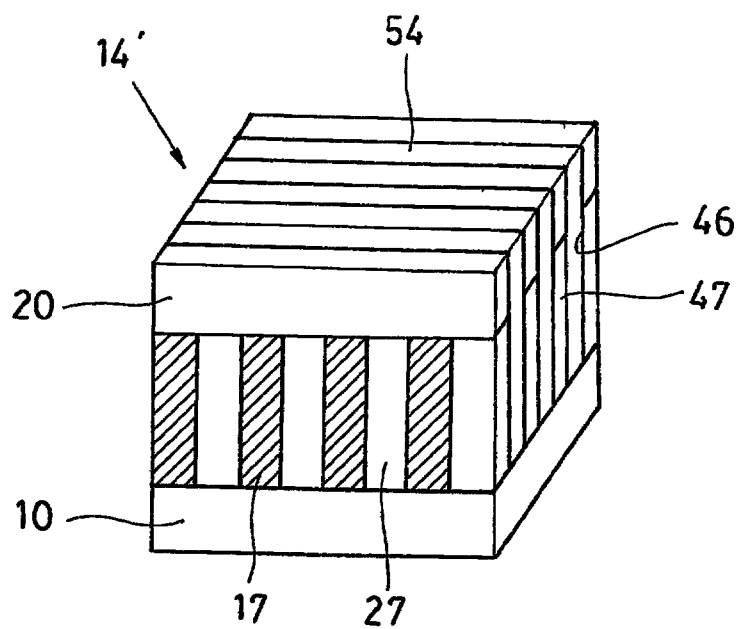


第13図

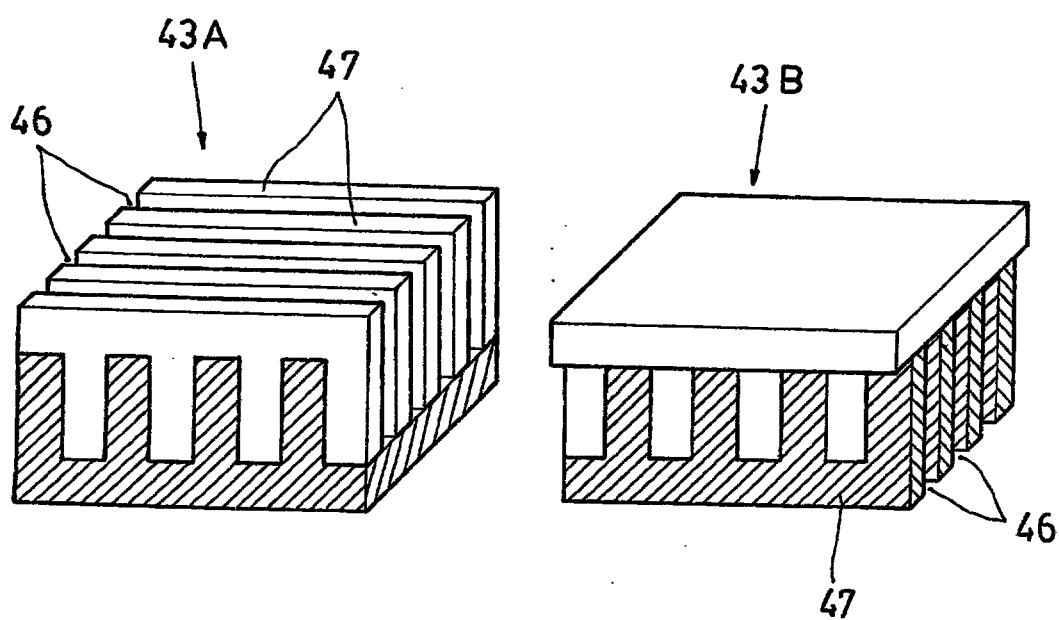


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第14図

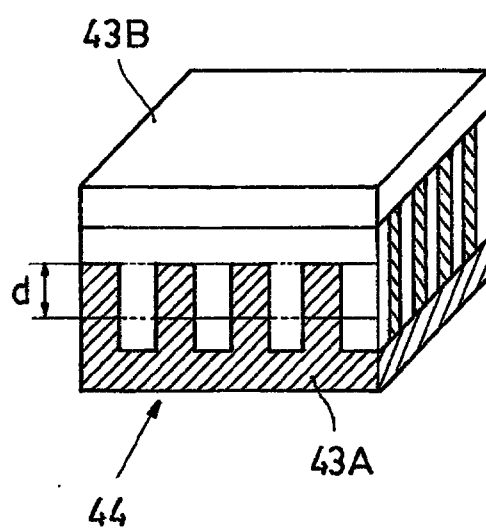


第15図

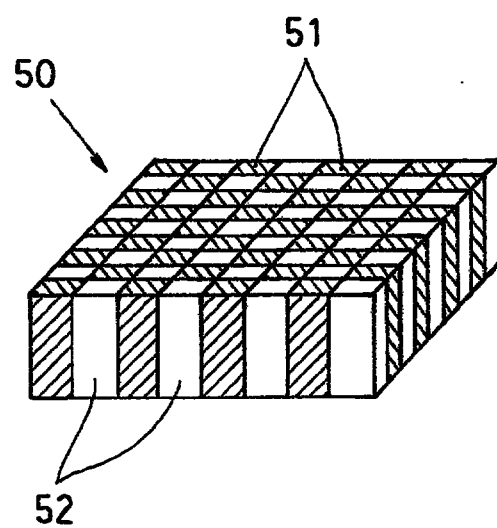


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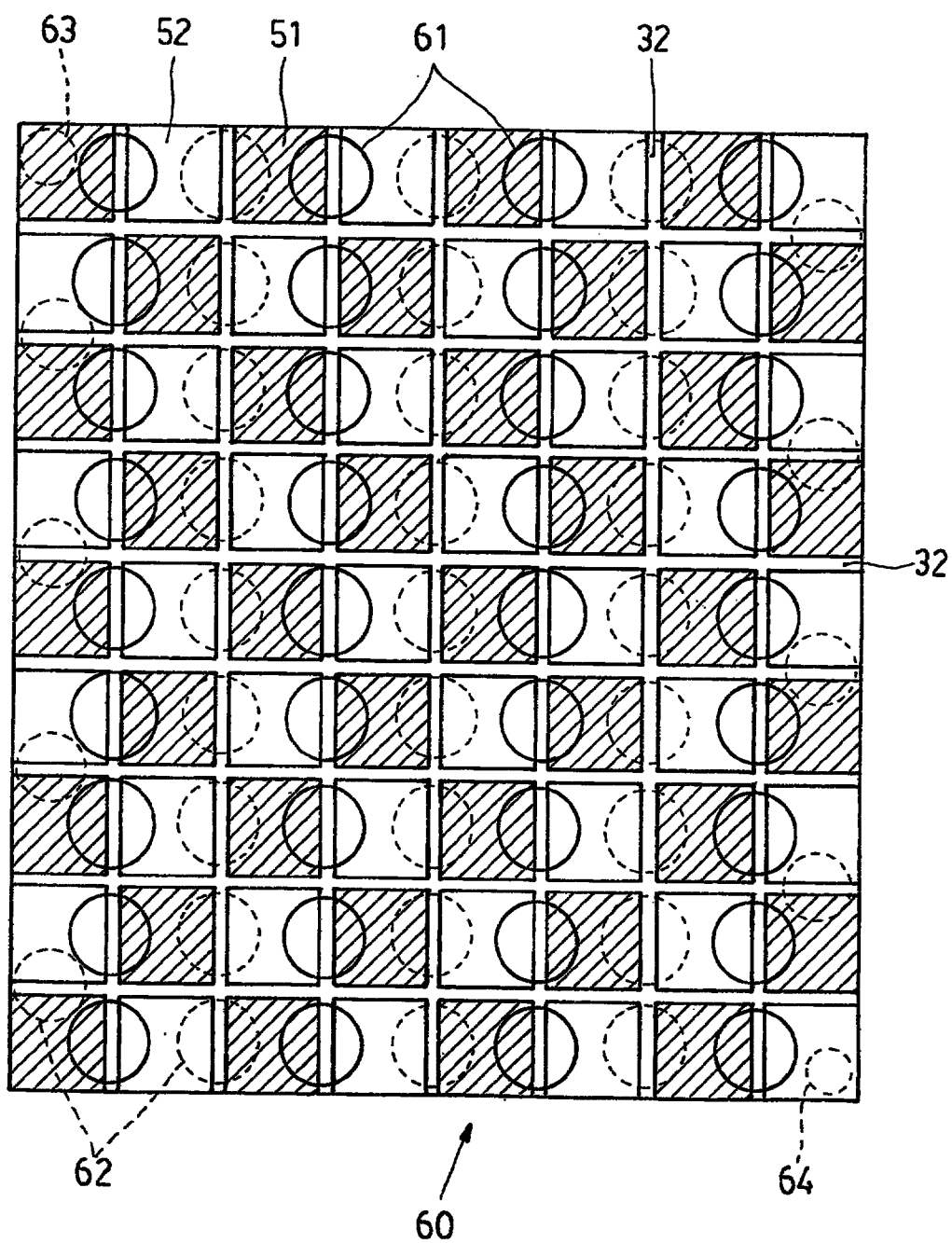
第16図



第17図

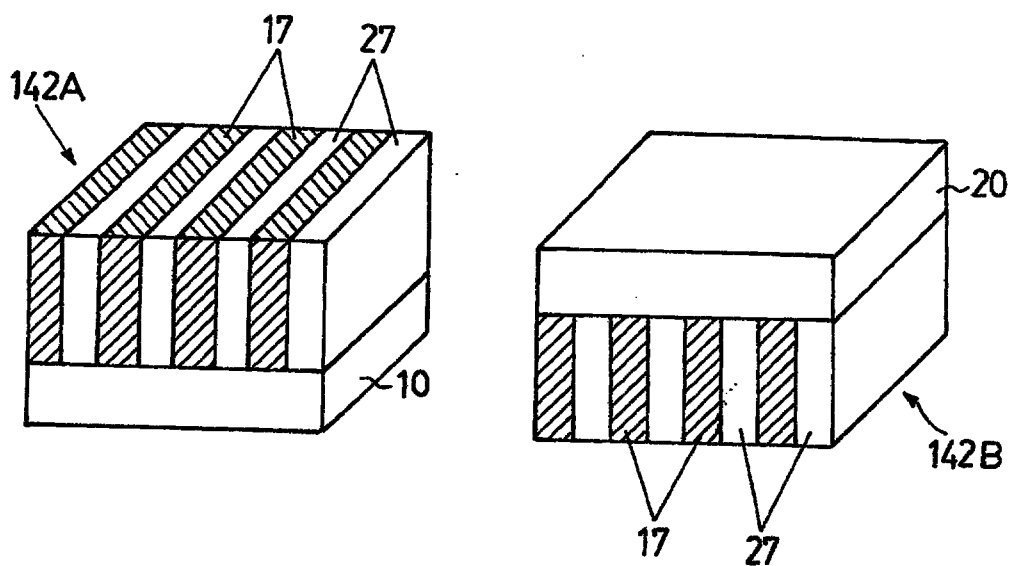


第18図

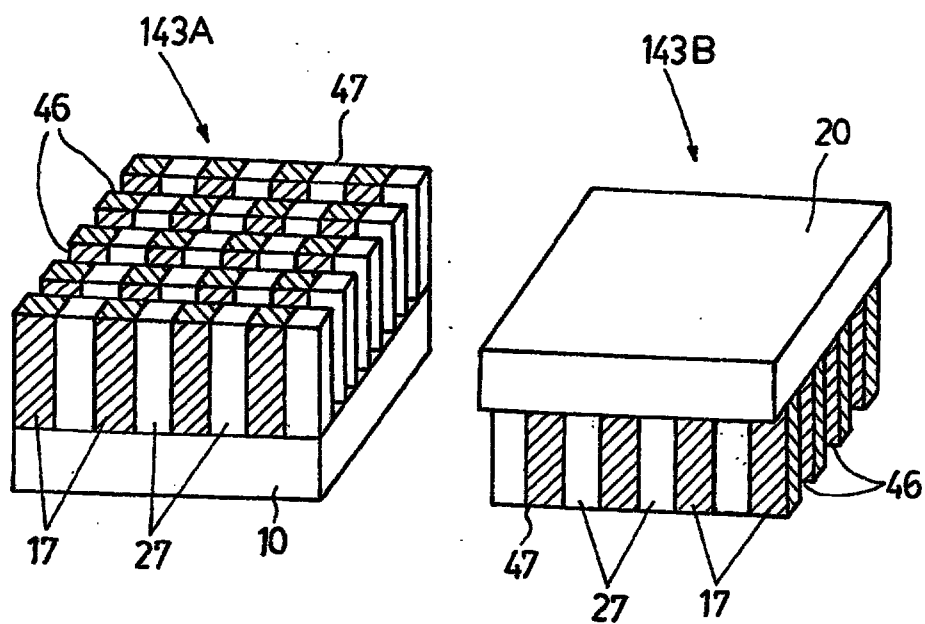


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第19図

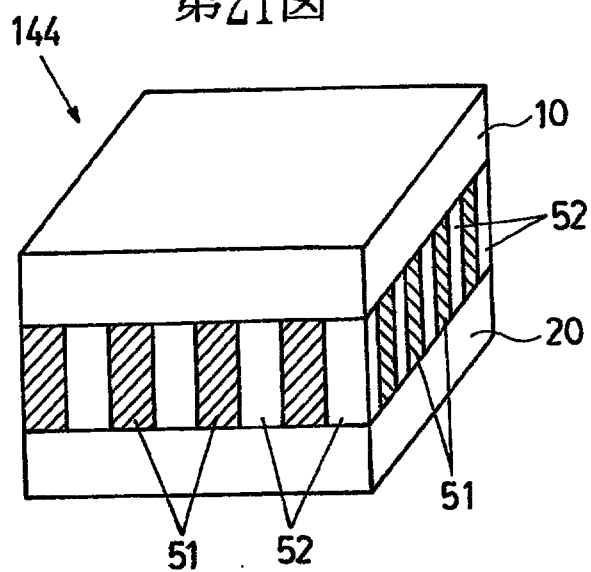


第20図

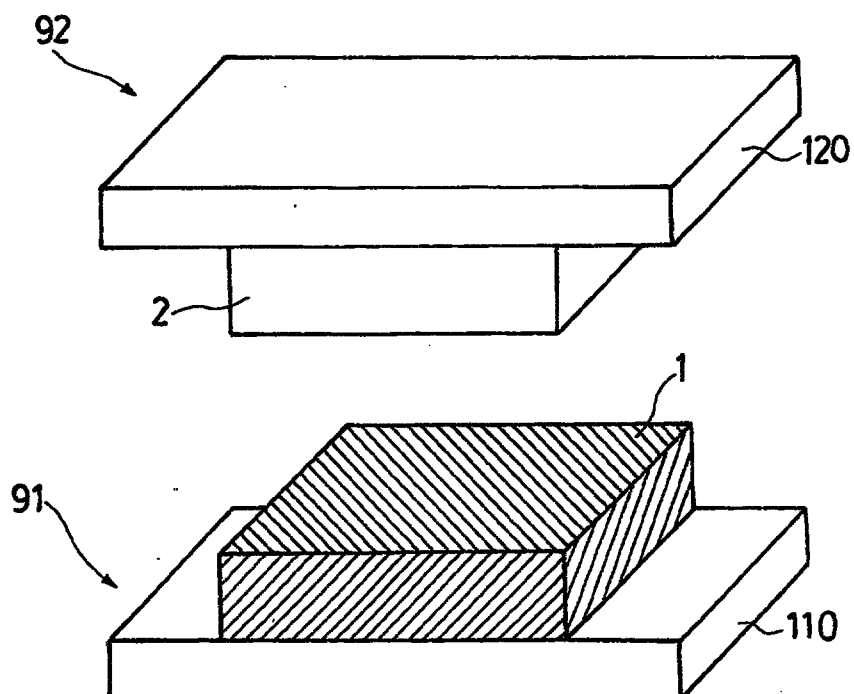


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第21図

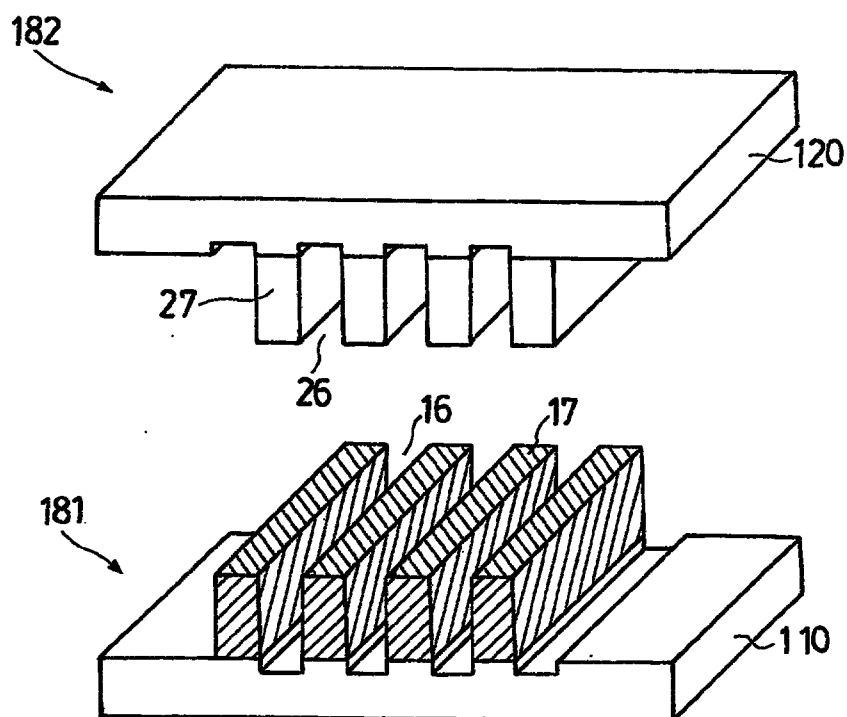


第22図

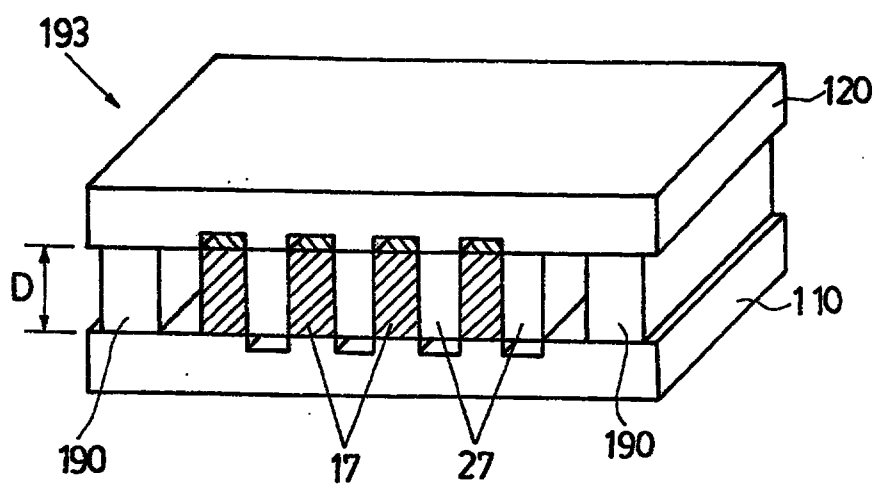


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第23図

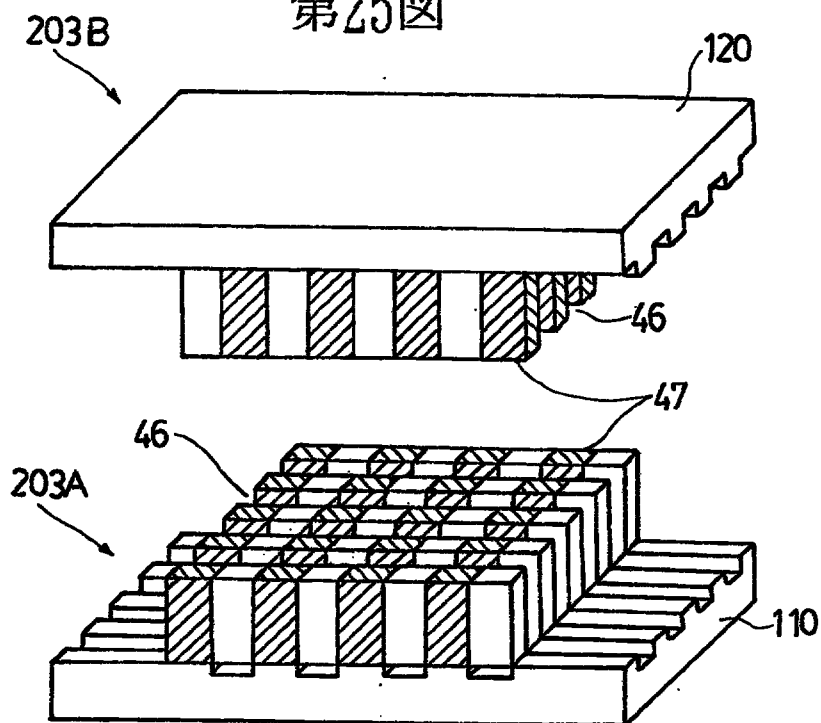


第24図

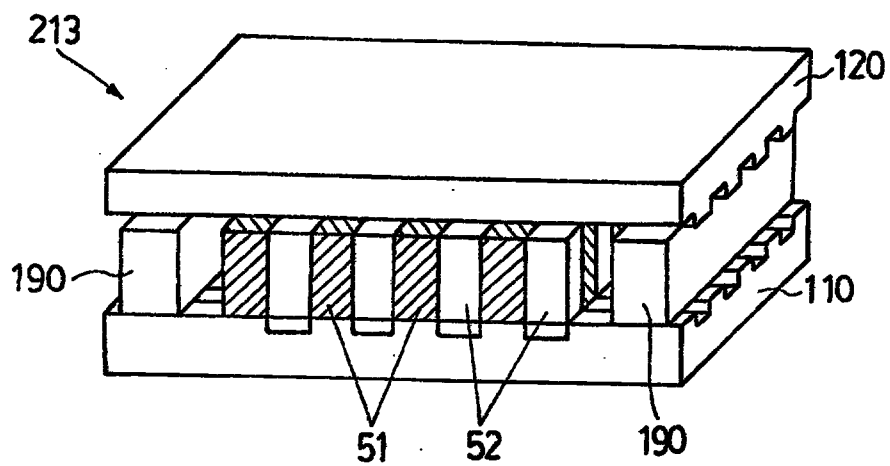


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第25図

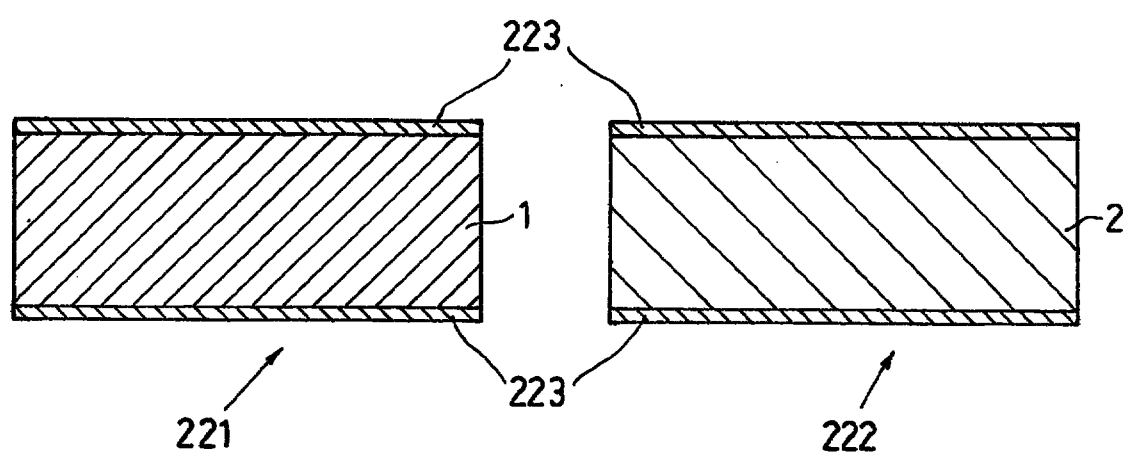


第26図

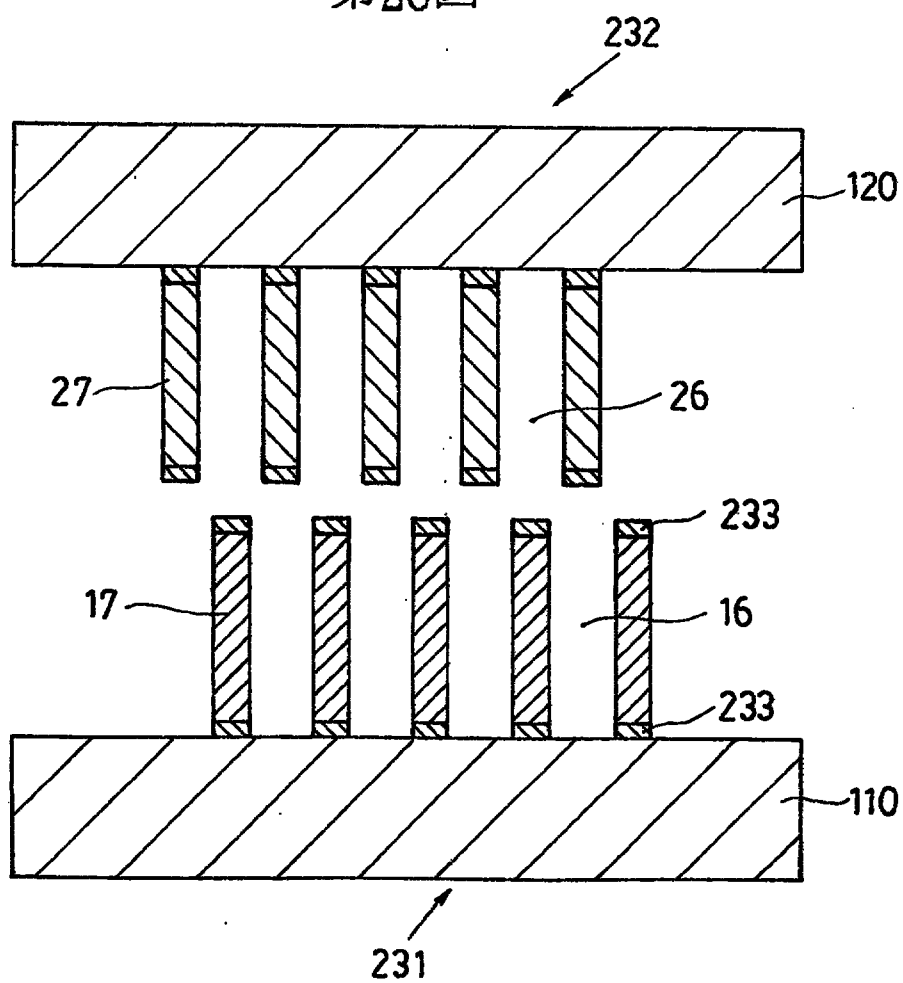


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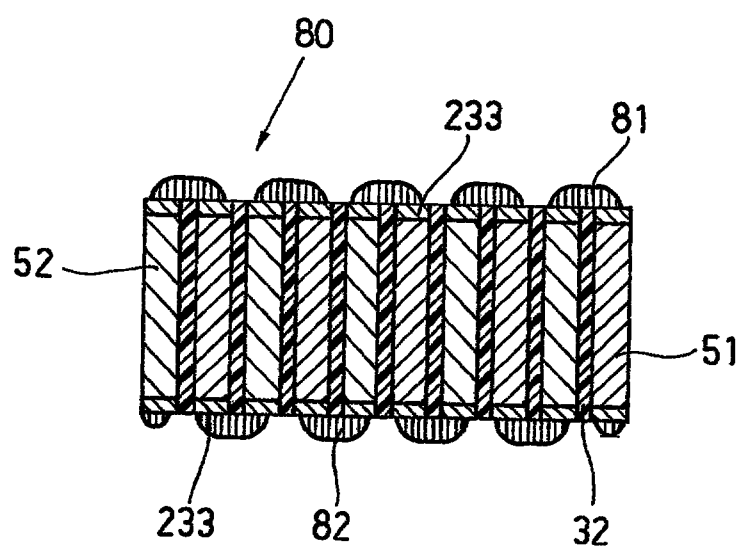
第27図



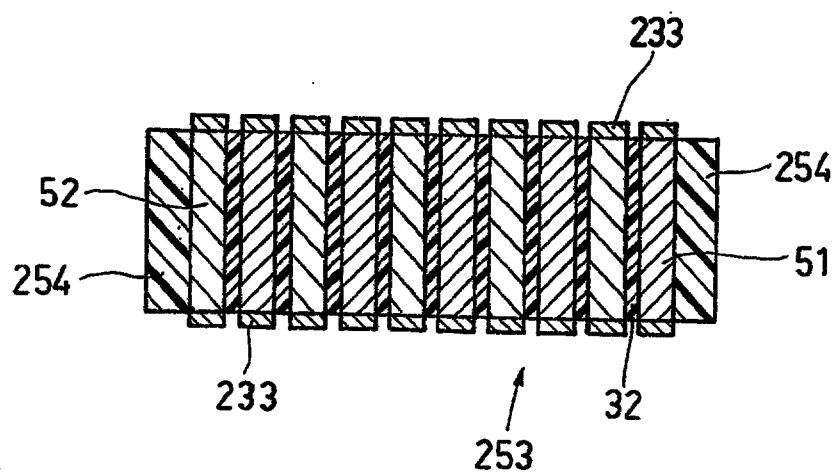
第28図



第29図

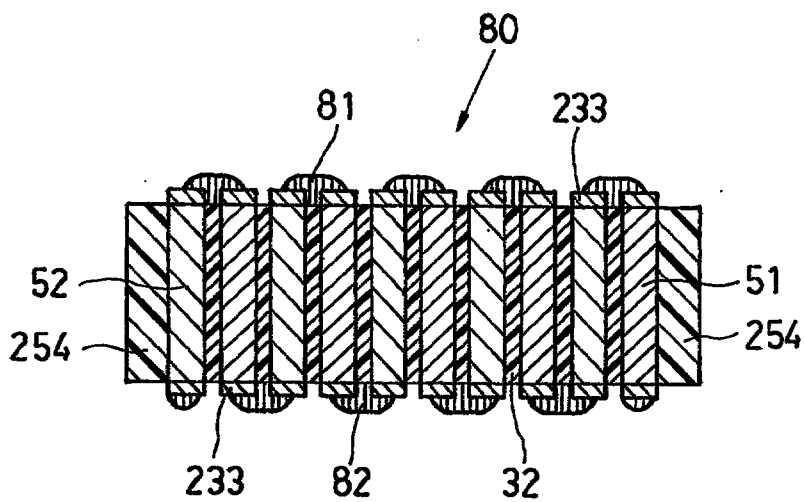


第30図

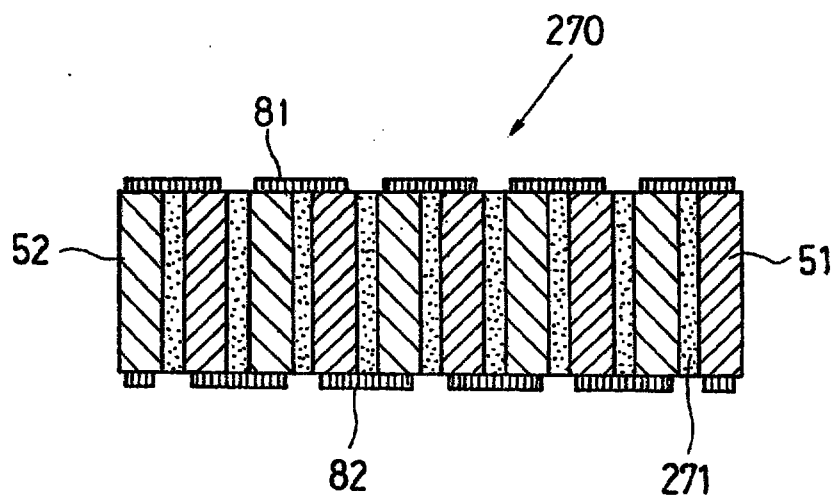


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第31図

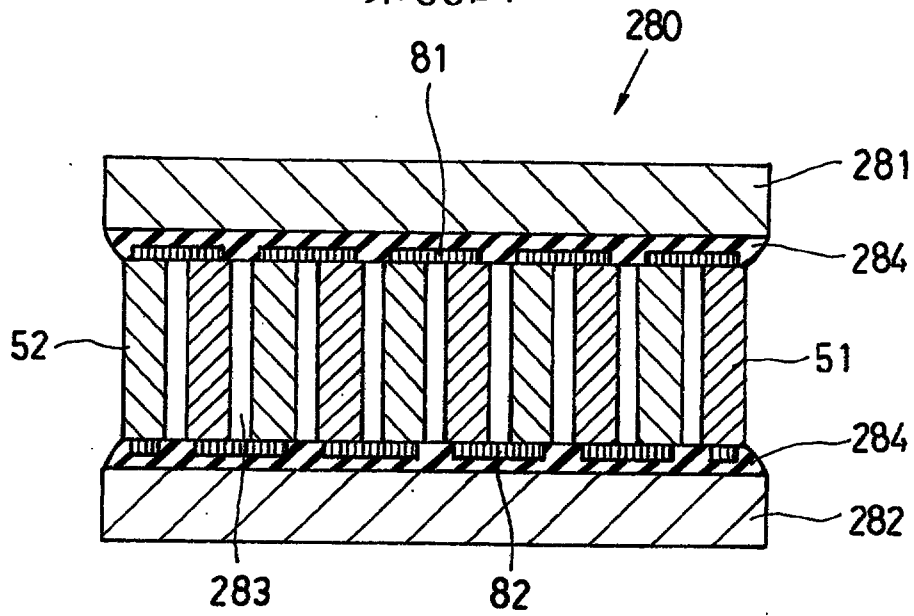


第32図

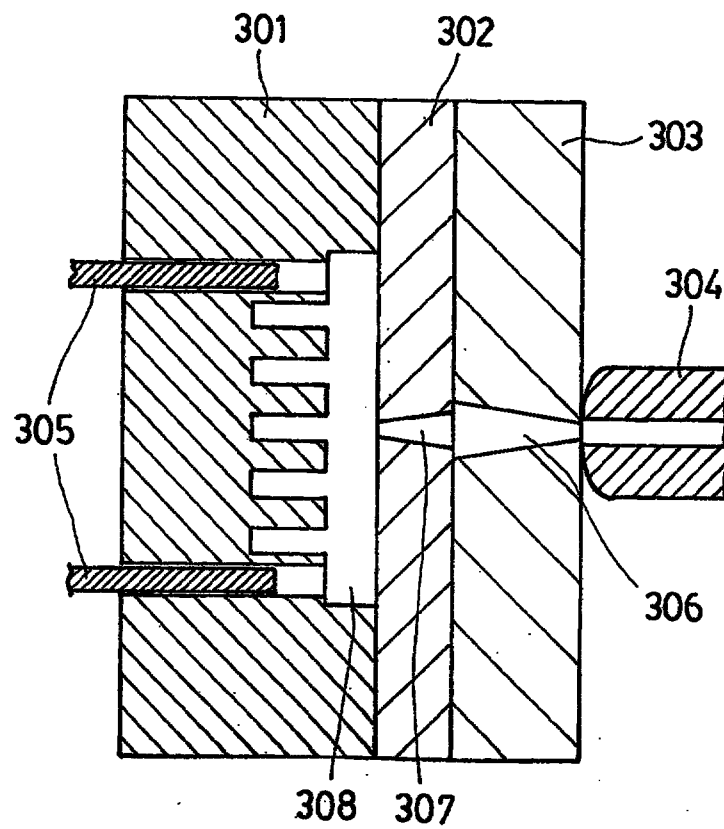


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第33図



第34図



SPECIFICATION

METHOD OF FABRICATING THERMOELECTRIC DEVICE

5 TECHNICAL FIELD

The present invention relates to a method of fabricating a thermoelectric device for use in a thermoelectric power generator taking advantage of the Seebeck effect, or a cooler taking advantage of the Peltier effect, and more particularly, to a method of fabricating a small
10 sized thermoelectric device incorporating a plurality of thermocouples.

BACKGROUND TECHNOLOGY

In each of the thermocouples making up a thermoelectric device, a voltage is developed by providing a difference in temperature between
15 the opposite ends thereof. This is due to the effect of the Seebeck effect, and a device designed to extract the voltage as electric energy is a thermoelectric power generator. The thermoelectric power generator wherein heat energy can be converted directly into electric energy has attracted much attention as effective means of utilizing heat energy, as
20 represented by the case of waste heat utilization.

Meanwhile, the flow of a current caused to occur through a thermocouple results in generation of heat at one end thereof, and absorption of heat at the other end thereof. This is due to the Peltier effect, and a cooler can be manufactured by taking advantage of such
25 phenomenon of heat absorption. This type of cooler which does not comprise mechanical components and can be reduced in size has an application as a portable refrigerator, or a localized cooler for lasers, integrated circuits, and the like.

Thus, the thermoelectric power generator or cooler made up of the thermoelectric device is simple in construction, and is in a more favorable condition for miniaturization as compared with other types of power generators or coolers, offering high usefulness. For example, with the thermoelectric device for use in the thermoelectric power generator, there will not arise a problem of leakage or depletion of electrolyte as with the case of a redox cell, and the thermoelectric device has therefore promising prospects for application to portable electronic devices such as an electronic wrist watch.

The general construction of a conventional thermoelectric device, and a conventional method of fabricating the same, have been disclosed in, for example, Japanese Patent Laid-open Publication No. 63 - 20880 or Japanese Patent Laid-open Publication No. 8 - 43555. Description disclosed therein is concerned with a thermoelectric device for use in generation of power. However, the basic construction thereof is the same as that of a thermoelectric device for use in cooling. Hence, the thermoelectric device for use only in generation of power is described hereinafter to avoid complexity in explanation.

In the conventional thermoelectric device disclosed in the publications described above, p-type and n-type thermoelectric semiconductors are alternately and regularly arranged so that a multitude of thermocouples are formed on a horizontal plane, and the thermocouples thus formed are electrically connected to each other in series.

The thermoelectric device is formed in a sheet-like shape by disposing the thermocouples on a plane, and the upper surface and under surface of the thermoelectric device become faces on which hot junctions and cold junctions of the thermocouples are located, respectively. Generation of electric power in the thermoelectric device is

caused to occur by a difference in temperature between the upper surface and the under surface of the device having a sheet-like shape.

Meanwhile, an output voltage of a thermocouple using a BiTe-based material, said to have the highest figure of merit of thermoelectric power generation at present, is about $400 \mu\text{V} / ^\circ\text{C}$ per couple.

When such thermocouples as described above are employed in a portable electronic device for use at around room temperature, for example, in an electronic watch, a satisfactory difference in temperature can not be expected to be developed inside the device. For example, in the case of a wrist watch, the temperature difference in a wrist watch developed between body temperature and the ambient temperature will be 2°C at most.

It follows that not less than about 2000 couples of BiTe-based thermocouples are required to obtain a voltage not lower than 1.5V, necessary for driving an electronic watch.

Furthermore, in the case of an electronic wrist watch, wherein mechanical components and electric circuit components need to be encased therein in spite of a small internal volume thereof in the first place, it is required that a thermoelectric device for power generation, very small in size, be used.

The conventional method of fabricating a thermoelectric device small in size and composed of a multitude of thermocouples has been disclosed in Japanese Patent Laid-open Publication No. 63 - 20880.

In the method disclosed, a multi-layered body is formed by stacking p-type and n-type thermoelectric semiconductors, in a thin sheet-like shape, on top of each other in layers while interposing a heat insulating material between respective layers, and then by bonding them together. Subsequently, grooves are formed at a given spacing in the multi-layered body, whereupon the grooves are filled up with a heat

insulating material, and connecting portions of individual thermoelectric semiconductors are removed, thereby forming n-type and p-type thermocouples, surrounded by the heat insulating material and isolated from each other. By electrically connecting the thermocouples
5 with each other in series, a thermoelectric device is completed.

Then, in the method disclosed in Japanese Patent Laid-open Publication No. 8 - 43555, p-type and n-type thermoelectric semiconductors, each having a plate-like shape, are first bonded to separate substrates, and thereafter, a grooving process of forming a
10 multitude of grooves at very small spacings in the longitudinal and transverse directions is applied to respective thermoelectric semiconductors.

As a result of the grooving process described above, a multitude of thermoelectric semiconductors, each columnar in shape, and
15 upstanding regularly on top of the respective substrates, resembling a kenzan (a needle-point flower holder for flower arrangement), are formed. The kenzan-like bodies composed of the n-type and p-type thermoelectric semiconductors, respectively, are thus prepared, and joined together such that the respective thermoelectric semiconductors,
20 columnar in shape, are mated with each other. Thereafter, an insulating material is filled between the respective thermoelectric semiconductors.

In the final step of processing, the substrates are removed, and a thermoelectric device is completed by electrically connecting
25 thermocouples with each other in series.

However, with the methods of fabricating the thermoelectric device as described in the foregoing, there will arise a problem that the material used for the thermoelectric semiconductors is prone to breakage during the process of forming the thermoelectric

semiconductors into a sheet-like shape, during the grooving process of forming the kenzan-like bodies, and the like, because of the fragile nature of the material itself for the thermoelectric semiconductors.

In particular, for forming as many as not less than 2000 couples of thermocouples in an ultra-small sized thermoelectric device which can be encased in a wrist watch, it is required that the thickness of the respective sheet-like thermoelectric semiconductors or the diameter of the respective columnar thermoelectric semiconductors be set to on the order of 100 μm or less, and consequently, the problem of fragility described above will become quite serious.

Hence, the present invention has been developed in order to solve such problems as encountered with the conventional methods of fabricating the thermoelectric device, and an object of the invention is therefore to provide a method of fabricating with ease and efficiently a thermoelectric device small in size, but incorporating a multitude of thermocouples so as to be able to output a high voltage.

DISCLOSURE OF THE INVENTION

To this end, a method of fabricating a thermoelectric device according to the invention comprises:

a grooved block fabrication process of forming grooved blocks composed of an n-type thermoelectric semiconductor and p-type thermoelectric semiconductor, respectively, each provided with a plurality of grooves formed at a same pitch and parallel with each other, leaving a depthwise portion of respective grooved blocks intact;

a fitting process of fitting the grooved blocks composed of the n-type thermoelectric semiconductor and p-type thermoelectric semiconductor formed, respectively, by said grooved block fabrication

process to each other such that surfaces of the respective grooved blocks, with the grooves formed thereon, face each other;

an adhesion process of forming an integrated block by adhering the grooved block composed of the n-type thermoelectric semiconductor and the grooved block composed of p-type thermoelectric semiconductor, fitted to each other by said fitting process, to each other after filling up gaps in fitting parts between the respective grooved blocks with an adhesive insulation member; and

a thermoelectric semiconductor pieces exposure process of exposing n-type and p-type thermoelectric semiconductor pieces by removing all portions of the integrated block formed by said adhesion process, other than the fitting parts where the grooved block composed of the n-type thermoelectric semiconductor and the grooved block composed of p-type thermoelectric semiconductor are fitted to each other.

When fabricating the thermoelectric device by the method comprising the process described above, thermoelectric semiconductor material having a problem of fragility is always handled in the form of a unit (block). Hence, delicate processing can be applied to the thermoelectric semiconductor material without causing breakage thereof, enabling the thermoelectric device made up of a plurality of thermocouples composed of a plurality of thermoelectric semiconductor pieces very small in size to be efficiently fabricated with ease.

Further, it is preferable that the method according to the invention further comprises a second grooving process of forming a plurality of grooves in the integrated block formed by the adhesion process, in the direction crossing the direction of the grooves formed by said grooved block fabrication process, leaving a depthwise portion of the integrated block intact; a solidification process of filling the grooves

formed by the second grooving process with adhesive insulation members and solidifying the same; and, a thermoelectric semiconductor pieces exposure process, to be applied thereafter, of exposing n-type and p-type thermoelectric semiconductor pieces by
5 removing all portions of the integrated block wherein the adhesive insulation members filling up the grooves are solidified in the solidification process, other than the fitting parts where the grooved blocks composed of the n-type thermoelectric semiconductor and p-type thermoelectric semiconductor, respectively, are fitted to each other.

10 This will result in a considerable increase in the number of thermocouples making up a thermoelectric device of a same size, and the output voltage of the thermoelectric device when used for generation of power can be raised.

It is yet further preferable that the method according to the
15 invention further comprises a grooving process of forming two grooved integrated blocks by forming a plurality of grooves at a same pitch and in the direction crossing the direction of the grooves formed by the grooved block fabrication process, leaving a depthwise portion of respective integrated blocks intact, in each of the two integrated blocks fabricated by
20 means of the grooved block fabrication process, fitting process, and adhesion process described in the foregoing; a second fitting process of fitting the two grooved integrated blocks to each other such that surfaces thereof with the grooves formed thereon face each other; a second adhesion process of forming a second integrated block by filling up gaps
25 in fitting parts between the two grooved integrated blocks fitted to each other by the fitting process with adhesive insulation members, and solidifying the same; and a thermoelectric semiconductor pieces exposure process, to be applied thereafter, of exposing n-type and p-type

thermoelectric semiconductor pieces by removing all depthwise portions of the second integrated block, other than the fitting parts.

This will result in a further considerable increase in the number of thermocouples making up a thermoelectric device of a same size, and the output voltage of the thermoelectric device when used for generation of power can be additionally increased.

In the methods of fabricating the thermoelectric device described, the process of forming the grooved block of the n-type thermoelectric semiconductor and grooved block of the p-type thermoelectric semiconductor by applying a grooving process to an n-type thermoelectric semiconductor block and p-type thermoelectric semiconductor block, respectively, such that a plurality of grooves are formed at a same pitch and in parallel with each other, leaving a depthwise portion of the respective blocks intact may be adopted for the grooved block fabrication process described above.

Otherwise, a process of forming the grooved block of the n-type thermoelectric semiconductor and grooved block of the p-type thermoelectric semiconductor by molding n-type thermoelectric semiconductor material and p-type thermoelectric semiconductor material by use of a mold for the grooved block, respectively, and sintering the same, may be adopted for the grooved block fabrication process described above.

In the methods of fabricating the thermoelectric device described, the thermoelectric device can be completed by applying a process of forming electrodes for connecting the exposed n-type and p-type thermoelectric semiconductor pieces to each other alternately and in series after the thermoelectric semiconductor pieces exposure process.

The method of fabricating the thermoelectric device may also comprise a grooving process applied to an n-type thermoelectric

semiconductor composite block, prepared by bonding an n-type thermoelectric semiconductor block to a base, and a p-type thermoelectric semiconductor composite block, prepared by bonding a p-type thermoelectric semiconductor block to a base, for forming a plurality of grooves in the n-type thermoelectric semiconductor block and the p-type thermoelectric semiconductor block, respectively, at a same pitch, and to a depth close to the interface between the respective thermoelectric semiconductor blocks and the base thereof; forming an n-type thermoelectric semiconductor composite block and p-type thermoelectric semiconductor composite block, with the grooves formed therein, respectively; and, the fitting process, adhesion process, second grooving process, solidification process, and the like, applied to a pair of thermoelectric semiconductor composite blocks, with the grooves formed therein, forming an integrated block. Or by means of these processes, two integrated blocks may be formed, and fitted to each other after the second grooving process is applied thereto, forming a second integrated block. Thereafter, the thermoelectric semiconductor pieces exposure process of exposing the n-type and p-type thermoelectric semiconductor pieces by removing the respective bases may be applied.

By adopting the processes described above, the thermoelectric semiconductor material can be fully utilized without wastage.

It may be preferable to use bases having a surface area larger than an area of the bonded surface of the respective thermoelectric semiconductor blocks and to interpose spacers between portions of the bases of the n-type thermoelectric semiconductor composite block and the p-type thermoelectric semiconductor composite block, respectively, where the respective thermoelectric semiconductor blocks do not exist, and in the fitting process, controlling a spacing between the bases to be

substantially equivalent to the thicknesses of the respective thermoelectric semiconductor blocks.

BRIEF DESCRIPTION OF THE DRAWINGS

5 Figs. 1 to 6 are perspective views of respective processes illustrating a first embodiment of a method of fabricating a thermoelectric device according to the invention;

Figs. 7 and 8 are expanded views of the portion A of an integrated block 3, shown by the imaginary lines in Fig. 3, illustrating variations of
10 the adhesion process;

Fig. 9 is a plan view of a completed thermoelectric device according to the first embodiment for explaining the construction of electrodes;

Figs. 10 to 14 are perspective views of respective processes
15 illustrating a second embodiment of a method of fabricating a thermoelectric device according to the invention;

Figs. 15 to 17 are perspective views showing the latter parts of fabrication processes illustrating a third embodiment of a method of fabricating a thermoelectric device according to the invention;

20 Fig. 18 is plan view of a completed thermoelectric device according to the third embodiment for explaining the construction of electrodes;

Figs. 19 to 21 are perspective views showing parts of fabrication processes illustrating a fourth embodiment of a method of fabricating a
25 thermoelectric device according to the invention;

Figs. 22 to 24 are perspective views showing the first half of fabrication processes illustrating a fifth embodiment of a method of fabricating a thermoelectric device according to the invention;

Figs. 25 to 26 are perspective views showing parts of fabrication processes illustrating a sixth embodiment of a method of fabricating a thermoelectric device according to the invention;

5 Figs. 27 to 29 are sectional views showing parts of fabrication processes illustrating a seventh embodiment of a method of fabricating a thermoelectric device according to the invention;

Figs. 30 and 31 are sectional views showing parts of fabrication processes illustrating an eighth embodiment of a method of fabricating a thermoelectric device according to the invention;

10 Figs. 32 and 33 are sectional views showing parts of fabrication processes illustrating a ninth embodiment of a method of fabricating a thermoelectric device according to the invention; and

15 Fig. 34 is a sectional view showing an example of a mold used in forming a grooved block of thermoelectric semiconductor by means of injection molding.

BEST MODE FOR CARRYING OUT THE INVENTION

Embodiments of the method of fabricating a thermoelectric device in carrying out the invention in the best mode are described hereinafter.

20

First Embodiment: Figs. 1 to 9

Firstly, a first embodiment of the method of fabricating a thermoelectric device according to the invention is described with reference to Figs. 1 to 9.

25

In the first embodiment of the invention, as shown in Fig. 1, an n-type thermoelectric semiconductor block 1 and a p-type thermoelectric semiconductor block 2 are prepared. It is desirable that the both blocks 1 and 2 be identical in all dimensions including the thickness thereof. For ease in identification of the respective blocks, all the surfaces of the n-

type thermoelectric semiconductor block 1 are shown by the diagonally shaded areas. The same applies to all other figures shown hereinafter.

Subsequently, as shown in Fig. 2, a first grooving process of fabricating a grooved block is applied, whereby a plurality of longitudinal grooves 16 at a given pitch are formed parallel with each other in the n-type thermoelectric semiconductor block 1 to a depth such that a thicknesswise portion 15 thereof is left intact, completing an n-type grooved block 11 provided with longitudinal partition walls 17 formed thereon at a predetermined spacing. Similarly, a plurality of longitudinal grooves 26 at a given pitch are formed parallel with each other in the p-type thermoelectric semiconductor block 2 as well to a depth such that a thicknesswise portion 25 thereof is left intact, completing the p-type grooved block 21 provided with longitudinal partition walls 27 formed thereon at a predetermined spacing.

In this instance, the longitudinal partition walls 17 of the n-type grooved block 11 and the longitudinal partition walls 27 of the p-type grooved block 21 are formed in a shape resembling the teeth of a comb, respectively, to enable the grooved blocks 11, 21 to snugly fit to each other, and while the longitudinal grooves 16, 26 are formed at a same pitch, the width of the respective longitudinal grooves 16, 26 is rendered slightly wider than that of the respective longitudinal partition walls 17, 27, to provide room for adhesion. Further, it is desirable to equalize the depth of the respective longitudinal grooves 16 to that of the respective longitudinal grooves 26.

The first grooving process of forming the longitudinal grooves 16, 26 is applied to the n-type thermoelectric semiconductor block 1 and p-type thermoelectric semiconductor block 2, respectively, by, for example, polishing with the use of a wire saw, or by grinding with the use of a dicing saw.

In the first embodiment of the invention, a BiTeSe sintered body is used as the n-type thermoelectric semiconductor block 1 and a BiTeSb sintered body is used as the p-type thermoelectric semiconductor block 2, the dimensions of the both blocks being set at 12 mm × 12 mm × 4 mm.

5 The longitudinal grooves 16, 26, each 70 μm wide, are formed at a pitch of 120 μm in the grooved blocks 11 and 21, respectively, to a depth of 3 mm against 4 mm in the thickness of the respective grooved blocks. Accordingly, the width of the respective longitudinal partition walls 17, 27 becomes 50 μm .

10 The method of fabricating the grooved blocks 11 and 21, composed of thermoelectric semiconductors, is not limited to the method of fine grooving by machining as described above. The same may be fabricated by a molding method such as an injection molding method, or the like, an example of which will be described later.

15 Subsequently, as shown in Fig. 3, a fitting process and adhesion process are applied, whereby the n-type grooved block 11 and p-type grooved block 21 are fitted to each other such that the longitudinal partition walls 27, 17 of the respective blocks are inserted into the longitudinal grooves 16, 26 of the respective opposite blocks, and both
20 blocks are fitted to each other by filling up gaps in fitting parts therebetween with an adhesive insulating material, forming an integrated block 3.

In these processes of forming the integrated block 3, wherein the n-type grooved block 11 and p-type grooved block 21 are fitted to each
25 other, and adhered together with the insulating material, adhesive layers formed thereby need to have the function of ensuring electrical insulation between the n-type grooved block 11 and p-type grooved block 21 besides the function of bonding the two blocks together.

For example, in the case where the inner walls of the longitudinal grooves 16, 26 are finished to have very smooth surfaces by polishing with the use of a wire saw, such electrical insulation can be ensured by simply immersing portions of the integrated block 3 in an adhesive of high fluidity prior to the adhesion process such that gaps between the longitudinal grooves 16, 26 and the longitudinal partition walls 27, 17, respectively, are filled up with the adhesive due to the capillary effect.

On the other hand, in the case where the inner walls of the longitudinal grooves 16, 26 are finished up into somewhat rough surfaces, maintenance of electrical insulation is ensured by applying a method as illustrated in Fig. 7 or 8 showing an enlarged view of the part A of the integrated block 3, as indicated by the imaginary lines in Fig. 3.

In the method shown in Fig. 7, an insulation film 31 is formed on the surfaces of both the longitudinal partition walls 17 and the longitudinal grooves 16 of the n-type grooved block 11, and the p-type grooved block 21 is fitted onto the insulation film 31 so that gaps between the insulation film 31 and the longitudinal partition walls 27 as well as the longitudinal grooves 26 thereof are filled up with the adhesive taking advantage of the capillary effect as described in the foregoing, forming an adhesive layer 32 after the adhesive is cured. The integrated block 3 is thus completed.

For the insulation film 31, either an inorganic film composed of silicon oxide, aluminum oxide, silicon nitride or the like, or an organic film composed of polyimide or the like may be used.

The insulation film 31 may be alternatively formed on the surfaces of the longitudinal partition walls 27 as well as the longitudinal grooves 26 of the p-type grooved block 21. Further, electrical insulation is additionally ensured by forming the insulation film 31 on the surfaces of

both the n-type grooved block 11 and p-type grooved block 21, to be fitted with each other.

In the method shown in Fig. 8, the integrated block 3 is fabricated by use of an adhesive with insulating spacers 33 dispersed therein. For example, 5 wt% of glass beads spherical in shape, 8 μm in average grain size, are added as the insulating spacers 33 to an epoxy adhesive. This will cause the glass beads to be dispersed substantially evenly in the adhesive layer 32 such that the n-type grooved block 11 and p-type grooved block 21 are forced to be isolated spatially from each other by the insulating spacers 33 composed of the glass beads, ensuring electrical insulation therebetween.

As shown in Fig. 4, a second grooving process is applied to the integrated block 3 shown in Fig. 3, completed by applying the fitting process and adhesion process as described hereinbefore, thereby forming transverse grooves 46. The block shown in Fig. 4, completed by forming the transverse grooves 46 in the integrated block 3, is referred to as a grooved integrated block 4 hereinafter.

In the process of forming the transverse grooves 46, a plurality of the transverse grooves 46 are formed at a given pitch in the direction crossing the direction in which the longitudinal grooves have been formed in the first grooving process as described in Fig. 3, leaving a thicknesswise portion 45 of the grooved integrated block 4 intact so that transverse partition walls 47 are formed at a predetermined spacing. In this process, the transverse grooves 46 may be formed so as to cross the longitudinal grooves 16, 26 formed in the first grooving process at optional angles. However, they most preferably cross at right angles as shown in Fig. 4.

Further, in this embodiment, the transverse grooves 46 are formed in the integrated block 3 from the side of the p-type grooved block

21 as shown in Fig. 4. However, the same may be formed therein conversely from the side of the n-type grooved block 11. Otherwise, the same may be formed in the fitting parts from the front face side or from the rear face side of the integrated block 3 shown in Fig. 3.

5 The transverse grooves 46 are preferably formed in the integrated block 3 to a depth such that the fitting parts between the n-type grooved block 11 and the p-type grooved block 21 are severed thereby.

As opposed to the case of the longitudinal grooves 16, 26, it is preferable that the width of the respective transverse grooves 46 be rendered as narrow as possible. This is because it is the transverse partition walls 47 that contribute to the capacity of power generation of the thermoelectric device as is shown from subsequent steps of processing, and consequently, from the viewpoint of performance of the thermoelectric device, the regions for the transverse grooves 46 should be reduced in size as much as possible.

10
15

Accordingly, in the first embodiment of the invention, the transverse grooves 46, 40 μm in width and 4 mm in depth, are formed at a pitch of 120 μm . Incidentally, the width 40 μm of the respective transverse grooves 46 represents a substantial limit size for the width of a groove formed by processing with the use of a wire saw.

20

Subsequently to the foregoing step of processing, a solidification process as shown in Fig. 5 is applied. That is, the respective transverse grooves 46 of the grooved integrated block 4 shown in Fig. 4 are filled up with insulating resin (insulation member), forming insulating resin layers 54 after the insulation member is cured. A block solidified with the insulating resin layers 54 is referred to as a grooved integrated block 4' hereinafter.

25

Thereafter, a process of exposing thermoelectric semiconductor pieces is applied to the grooved integrated block 4' solidified with the

insulating resin layers 54, whereby portions (portions having thickness denoted by a, b, respectively, in Fig. 5) of the grooved integrated block 4' which have been left intact without the grooving process applied thereto during the first and second grooving processes described in the foregoing are removed by polishing, or grinding the upper and under surfaces of the grooved integrated block 4', and the remainder is finished up such that only the fitting parts shown in Fig. 3, wherein the longitudinal grooves 16, 26, composed of the n-type thermoelectric semiconductor, and p-type thermoelectric semiconductor, respectively, are fitted to the longitudinal partition walls 27, 17, composed of the p-type thermoelectric semiconductor, and n-type thermoelectric semiconductor, respectively, and a portion wherein the transverse grooves 46 are formed, is left intact. A thermoelectric device block 5 shown in Fig. 6 is thus obtained.

In the thermoelectric device block 5, a multitude of n-type thermoelectric semiconductor pieces 51, and p-type thermoelectric semiconductor pieces 52 are insulated from each other via the insulating resin layers 54, and integrally adhered to each other while the upper as well as under surfaces thereof are exposed.

In the final step of processing, a process of forming electrodes is applied to both the upper and under surfaces of the thermoelectric device block 5 shown in Fig. 6 such that the n-type thermoelectric semiconductor pieces 51 and p-type thermoelectric semiconductor pieces 52 are connected with each other, alternately and electrically in series, thereby obtaining a thermoelectric device 6 shown in Fig. 9.

Fig. 9 is a plan view of the thermoelectric device 6, as seen from directly above, illustrating various electrodes formed on the upper as well as under surfaces thereof.

In the figure, upper surface electrodes 61a circular in shape as indicated by the solid lines and under surface electrodes 62a circular in shape as indicated by the broken lines are electrodes for connecting together the n-type thermoelectric semiconductor pieces 51 and p-type thermoelectric semiconductor pieces 52 adjacent to each other, electrically in series, forming a multitude of thermocouples. Upper surface electrodes 61b and under surface electrodes 62b, resembling the letter L in shape, are electrodes required in the periphery region of the thermoelectric device 6 for connecting the n-type or p-type thermoelectric semiconductor pieces in parallel although it is deemed unusable. The respective thermoelectric semiconductor pieces 51, 52 are insulated from each other by means of the adhesive layers 32 and the insulating resin layers 54. Further, under surface electrodes 63, 64, in the shape of a small circle indicated by the broken lines are electrodes for outputting voltage externally.

Each of the electrodes described above is formed by depositing a gold (Au) film on both the upper and under surfaces of the thermoelectric device block 5 shown in Fig. 6 by means of the vacuum coating method, sputtering method, electroless plating method, or the like, and then, by patterning on the gold film by the photolithographic technique and etching technique.

In the case where the upper and under surfaces of the thermoelectric device block 5, on which the electrodes are to be formed, are likely to cause a problem of surface roughness when finished by only grinding as described hereinbefore, it is desirable to render the surfaces smoother by lapping, or the like as this will prevent occurrence of faults with the electrodes (such as breakage) thereof.

For the electrodes, use can be made of not only the gold film but also other metal film, for example, a Cu film, Al film, Ni film, Fe film,

or a multi-layer film (for example, Al / Ni film) composed of the
aforesaid films combined together. Further, in forming the electrodes,
use may be made of the printing method, masked vapor deposition
method, or a method whereby the electrodes are patterned beforehand on
5 an insulating sheet-like material made of glass or ceramic, and the
sheet-like material as a whole is pasted on the surfaces.

In the method according to the first embodiment of the invention,
the longitudinal partition walls 17, 27 and the transverse partition walls
47, composed of the thermoelectric semiconductor materials, and very
10 thin, are formed in the first and second grooving processes as shown in
Figs. 2 and 4. Although these partition walls, individually, are very thin
and fragile, the same together constitute an integrated block, and
processing operations can be performed on respective blocks as a whole
without need of performing delicate operations such as holding
15 individual partition walls for transfer and stacking the same, and the
like. Hence, in comparison with the conventional method disclosed in
Japanese Patent Laid-open Publication No. 63 - 20880, it is possible to
fabricate a thermoelectric device incorporating a multitude of small
sized thermocouples efficiently with ease, overcoming the problem of
20 fragility.

In the case of another conventional method disclosed in Japanese
Patent Laid-open Publication No. 8 - 43555, integrated blocks are used.
However, thermoelectric semiconductors are bonded to separate base
members, and processed so as to form a multitude of columnar shapes.
25 As a result, extreme difficulties are still encountered in fabrication of a
product due to the serious problem of fragility. As opposed to such a
method, the method according to the first embodiment of the invention is
a method of fabrication whereby thermoelectric semiconductors are
always processed when the same are in the form of an integrated block,

thus enabling fine structural processing and assembling of thermoelectric semiconductor material, which is a very fragile material, to be carried out with ease. Consequently, it is possible to efficiently fabricate with ease a thermoelectric device provided with a
5 multitude of thermocouples in order to enhance the output voltage thereof, although same is small in size.

However, the process of exposing thermoelectric semiconductor pieces may be applied straight to the integrated block 3 shown in Fig. 3 by omitting the second grooving process, and the solidification process
10 whereby grooved parts (the transverse grooves 47 in Fig. 4) are filled up with the insulation member, which is then solidified, forming the insulating resin layers 54 shown in Fig. 5, as applied in carrying out the first embodiment. Such omission, however, will result in a decrease in the number of thermocouples making up the thermoelectric device.

15 In this case, the grinding process, and the like are applied to the upper as well as under surfaces of the integrated block 3 fabricated by means of the fitting process and adhesion process as shown in Fig. 3, and by removing portions of the integrated block 3, other than parts where the longitudinal partition walls 17, 27 of the n-type grooved block
20 11 and p-type grooved block 21, respectively, are fitted to the longitudinal grooves 16, 26, the thermoelectric device block with the n-type and p-type thermoelectric semiconductor pieces exposed can be fabricated.

Thereafter, the process of forming the electrodes is applied thereto, whereby electrodes for connecting the exposed n-type and p-type
25 thermoelectric semiconductor pieces (that is, the longitudinal partition walls 17 of the n-type groove block 11 and the longitudinal partition walls 27 of the p-type groove block 21) alternately to each other and in series are formed on the upper as well as under surfaces of the thermoelectric device block, thus fabricating the thermoelectric device.

Second Embodiment: Figs 10 to 14

Next, a second embodiment of the method of fabricating a thermoelectric device according to the invention is described hereinafter with reference to Figs. 10 to 14. In these figures, parts corresponding to those previously described with reference to the first embodiment shown in Figs. 1 to 5 are denoted by the same reference numerals.

In the second embodiment, as shown in Fig. 10, an n-type thermoelectric semiconductor composite block 12 formed by bonding an n-type thermoelectric semiconductor block 1 to a base 10, and a p-type thermoelectric semiconductor composite block 22 formed by bonding a p-type thermoelectric semiconductor block 2 to a base 20 are first prepared. It is desirable that the n-type thermoelectric semiconductor block 1 and the p-type thermoelectric semiconductor block 2 be identical in all dimensions including the thickness thereof.

The thermoelectric semiconductor blocks 1, 2 are bonded to the bases 10, 20, respectively, with an adhesive or wax. Further, for the bases 10, 20, use can be made of various materials having a given hardness such as glass, ceramic, plastic, metal, and the like.

Subsequently, a grooving process, the same as applied in the first grooving process in the first embodiment is applied to the respective thermoelectric semiconductor blocks 1, 2 of the thermoelectric semiconductor composite blocks 12, 22, respectively, and as shown in Fig. 11, longitudinal grooves 16, 26 as well as longitudinal partition walls 17, 27, resembling the teeth of a comb in shape, are formed, fabricating an n-type grooved composite block 13 and a p-type grooved composite block 23. The pitch and width of the longitudinal grooves 16, 26 are the same as in the case of the first embodiment, however, the depth thereof is set to be substantially close to the interface between the

thermoelectric semiconductor block 1, or 2 and the base 10 or 20, respectively. More specifically, the depth is selected from among slightly short of the interface, down to just the interface, or below the interface, cutting slightly into the base 10 or 20, depending on the
5 circumstance.

Thereafter, a fitting process whereby the n-type grooved composite block 13 and p-type grooved composite block 23 are fitted to each other such that respective grooved surfaces face each other is applied, and then, an adhesion process whereby gaps in fitting parts between the n-
10 type grooved composite block 13 and p-type grooved composite block 23 which are fitted to each other are filled up with an adhesive insulation member so that the n-type grooved composite block 13 and p-type grooved composite block 23 are adhered to each other is applied, thereby fabricating an integrated block 3' shown in Fig. 12.

Subsequently, a grooving process, the same as applied in the
15 second grooving process in the first embodiment, as shown in Fig. 4, is applied to the integrated block 3' as shown in Fig. 13, whereby transverse grooves 46 and transverse partition walls 47 are formed, fabricating a grooved integrated block 14. In this instance, the
20 transverse grooves 46 are cut into one of the grooved composite blocks to a depth close to the interface thereof with the base 10 or 20 of the other grooved composite block and in such a direction as to cross (at right angles, in this embodiment) the longitudinal grooves 16, 26, and the longitudinal partition walls 17, 27, formed in the first grooving process.

Then, as shown in Fig. 14, a solidification process is applied
25 whereby grooved parts, that is, the transverse grooves 46, are filled up with insulating resin (insulation member), and the insulating resin is then solidified, forming insulating resin layers 54. A block solidified

with the insulating resin layers 54 is referred to hereafter as a grooved integrated block 14'.

Thereafter, a process of exposing thermoelectric semiconductor pieces is applied to the grooved integrated block 14' shown in Fig. 14, whereby the bases 10 and 20, that is, bottom and top portions of the grooved integrated block 14', are removed, obtaining a thermoelectric device block 5, the same as shown in Fig. 6 in the case of the first embodiment. The base on the side where the grooving process is applied (the base 20 in the example shown in Fig. 13) may be removed prior to forming the transverse grooves 46.

Further, by applying a process of forming electrodes for forming the electrodes on the upper and under surfaces of the thermoelectric device block 5 such that n-type thermoelectric semiconductor pieces 51 and p-type thermoelectric semiconductor pieces 52 are connected to each other alternately and electrically in series, a thermoelectric device 6, the same as shown in Fig. 9, can be fabricated.

In the method according to the second embodiment, the bases 10, 20 are employed to integrally support the longitudinal partition walls 17, 27, and the transverse partition walls 47 in place of portions left intact without the grooving process applied thereto (the portions 15, 25 shown in Fig. 2) of the thermoelectric semiconductor blocks 1 and 2, respectively, which will be eventually removed by grinding as in the aforesaid first embodiment. Consequently, effective use can be made of portions of the thermoelectric semiconductor material, in regions close to the upper and under surfaces thereof, reducing unusable portions thereof. Therefore, the method has an advantage of remarkably improving the utilization efficiency of the material.

Other merits of operation according to this embodiment are the same as for the first embodiment.

Third Embodiment: Figs. 15 to 18

Now, a third embodiment of the method of fabricating a thermoelectric device according to the invention is described hereinafter with reference to Figs. 15 to 18. The first half of a process applied in
5 carrying out the third embodiment is the same as for the first embodiment described with reference to Figs 1 to 3, and accordingly, will only be briefly described referring to these figures.

In the third embodiment, two each of the n-type thermoelectric semiconductor blocks 1 and p-type thermoelectric semiconductor blocks
10 2 as shown in Fig. 1 are prepared. Subsequently, a first grooving process as shown in Fig. 2 is applied to the respective thermoelectric semiconductor blocks, whereby a plurality of longitudinal grooves 16, 26, and longitudinal partition walls 17, 27 are formed at a same pitch, and parallel with each other such that the depth of the former is equal to the
15 height of the latter, fabricating two pairs of n-type grooved blocks 11, and p-type grooved blocks 21.

In this case as well, the two pairs of the n-type grooved blocks 11, and p-type grooved blocks 21 may be fabricated by a process of fabricating grooved blocks using a molding method, which will be described later.

Subsequently, by applying a fitting process as shown in Fig. 3,
20 whereby the respective n-type grooved blocks 11 and p-type grooved blocks 21 are fitted to each other, and a first adhesion process of forming integrated blocks, whereby the grooved blocks fitted are adhered to each other by filling up gaps in fitting parts thereof with an adhesive
25 insulating material, two integrated blocks 3 are fabricated.

Thereafter, a second grooving process is applied to one of the two integrated blocks 3 from the side of the p-type grooved block 21 shown in Fig. 3, and to the other from the side of the n-type grooved block 11, whereby a plurality of grooves parallel with each other are formed at a

same pitch in the direction crossing the direction in which the first grooving process has been applied, (at right angles, in this embodiment), fabricating a pair of grooved integrated blocks 43A, 43B, wherein a plurality of transverse grooves 46 and transverse partition
5 walls 47 are formed as shown in Fig. 15, the depth of the former being equal to the height of the latter.

In this case, the dimensions of the transverse grooves 46 and transverse partition walls 47 are rendered similar to those of the longitudinal grooves 16, 26, and longitudinal partition walls 17, 27,
10 described in the first embodiment with reference to Fig. 2, so that the transverse grooves 46 in one of the grooved integrated blocks, and the transverse partition walls 47 in the other of the grooved integrated blocks can be fitted to each other. That is, in the grooved integrated blocks 43A, 43B, shown in Fig. 15, the transverse grooves 46 are formed at a same
15 pitch, and the width of the respective transverse grooves 46 is rendered wider than that of the respective transverse partition walls 47.

Subsequently, as shown in Fig. 16, by applying a second fitting process whereby the pair of grooved integrated blocks 43A, 43B are combined with each other by fitting the respective transverse partition
20 walls 47 into the respective transverse grooves 46, and further, by applying a second adhesion process whereby the grooved integrated blocks fitted together are integrally adhered to each other by filling up gaps between fitting parts with an adhesive insulating material, the pair of the grooved integrated blocks are integrally joined together,
25 forming a doubly integrated block 44.

Further, for fitting and adhering together the grooved integrated blocks 43A with 43B, the methods previously described in the first embodiment with reference to Figs. 3, 7, and 8 are applied.

Thereafter, a process of exposing thermoelectric semiconductor pieces is applied to the doubly integrated block 44. That is, portions of the doubly integrated block 44, other than a depthwise portion denoted by d in Fig. 16, are removed by polishing or grinding the upper as well as
5 under surfaces thereof so that the remainder is finished up, leaving intact regions where the longitudinal grooves 16, 26, the transverse grooves 46, the longitudinal partition walls 27, 17, and the transverse partition walls 47, composed of either of the n-type thermoelectric semiconductor and p-type thermoelectric semiconductor, are all fitted to
10 each other. Thus, as shown in Fig. 17, a thermoelectric device block 50 wherein n-type thermoelectric semiconductor pieces 51 and p-type thermoelectric semiconductor pieces 52 are alternately arranged is fabricated.

In integrally joining the grooved integrated blocks 43A with 43B in
15 carrying out this embodiment, preferable fabrication conditions require that the n-type thermoelectric semiconductor pieces 51 and p-type thermoelectric semiconductor pieces 52 be arranged regularly like a checkerboard as shown in Fig. 17. Accordingly, respective positions thereof need to be aligned, which may be accomplished by providing a
20 benchmark face on the periphery of each of the grooved integrated blocks, and joining the same together based on the benchmark face using a jig.

Such alignment in positioning will facilitate wiring work in a process of electrode wiring described hereinafter because of
25 standardized and simplified shapes and layout of the electrodes as shown in Fig. 18. Furthermore, this will contribute to improvement in the utilization efficiency of the thermoelectric semiconductors because the thermoelectric semiconductor pieces located in the edge portions on

the opposite sides in Fig. 9, not contributing to electrical connection in series, can be eliminated in this way.

Then, a process of forming electrodes is applied to the upper as well as under surfaces of the thermoelectric device block 50 such that
5 the n-type thermoelectric semiconductor pieces 51 and p-type thermoelectric semiconductor pieces 52 are alternately and electrically connected with each other in series, thereby fabricating a thermoelectric device 60 shown in Fig. 18.

Fig. 18 is a plan view of the thermoelectric device 60, as seen
10 directly from above, and respective electrodes are formed on both the upper surface and the under surface thereof.

Upper surface electrodes 61 circular in shape as indicated by the solid lines, formed on the upper surface of the thermoelectric device block 50 and under surface electrodes 62 circular in shape as indicated
15 by the broken lines, formed on the under surface thereof are electrodes for connecting together the n-type thermoelectric semiconductor pieces 51 and p-type thermoelectric semiconductor pieces 52, adjacent to each other, in series, forming a plurality of thermocouples. Further, under surface electrodes 63, 64 are electrodes for outputting voltage externally.

Each of the electrodes denoted by 61 to 64 is formed by depositing a
20 gold (Au) film on both the upper and under surfaces of the thermoelectric device block 50 shown in Fig. 17 by means of the vacuum coating method, sputtering method, electroless plating method, or the like, and then, by patterning on the gold film by use of the
25 photolithographic technique and etching technique. Further, as a material for the electrodes, use can be made of not only gold film but also various other materials cited in the first embodiment described in the foregoing.

In the case where surface roughness of the upper and under surfaces of the thermoelectric device block 50, on which the electrodes 61 to 64 are formed, is likely to cause a problem as with the case of the first embodiment, it is desirable to render the surfaces smoother by lapping, or the like, as occurrence of faults with the electrodes (such as breakage) thereof is inhibited in this way.

Accordingly, the method according to the third embodiment of the invention has an advantage in that the upper surface electrodes 61b and under surface electrodes 62b formed in the shape resembling the letter L as shown in Fig. 9, which are required in the first and second embodiments, can be dispensed with, facilitating the wiring process and enabling effective use of the thermoelectric semiconductor material.

Further, with the thermoelectric device according to the third embodiment, the number of thermoelectric semiconductor pieces incorporated therein per unit volume thereof can be substantially doubled over that in the case of the first embodiment or the second embodiment so that a thermoelectric device smaller in size, but capable of outputting a higher voltage, will be obtained.

With the method according to the third embodiment, the side of the integrated block 3 shown in Fig. 3, on which the grooving process is applied, may be ground beforehand prior to forming the transverse grooves 46 as shown in Fig. 15 such that fitting parts between the longitudinal grooves 16, 26, and the longitudinal partition walls 17, 27, composed of the n-type thermoelectric semiconductor and p-type thermoelectric semiconductor, respectively, are exposed.

If the transverse grooves 46 are formed subsequently, all of the longitudinal grooves 16, 26, the transverse grooves 46, the longitudinal partition walls 17, 27, and the transverse partition walls 47, composed of the n-type thermoelectric semiconductor, and p-type thermoelectric

semiconductor, respectively, are fitted together in their entirety when the second fitting process shown in Fig. 16 is applied. As a result, in the process of exposing the thermoelectric semiconductor pieces, the thermoelectric semiconductor pieces can be formed by leaving intact a
5 portion of thermoelectric semiconductor material, corresponding to the full height of the longitudinal partition walls 17, 27 with the result that the utilization efficiency of the thermoelectric semiconductor material is enhanced.

10 Fourth Embodiment: Figs. 19 to 21

A fourth embodiment of a method of fabricating a thermoelectric device according to the invention is described hereinafter with reference to Figs. 19 to 21. The first half of a process applied in carrying out the fourth embodiment is the same as for the second embodiment described
15 with reference to Figs. 10 to 12, and accordingly, will only be briefly described referring to these figures.

In the fourth embodiment, two each of n-type thermoelectric semiconductor composite blocks 12 formed by bonding the n-type thermoelectric semiconductor block 1 to the base 10, shown in Fig. 10,
20 and p-type thermoelectric semiconductor composite blocks 22 formed by bonding the p-type thermoelectric semiconductor block 2 to the base 20, shown in Fig. 10, are prepared.

Then, a first grooving process is applied to the respective thermoelectric semiconductor composite blocks 12, 22, whereby a
25 plurality of grooves at a same pitch are formed in the n-type thermoelectric semiconductor block 1, and the p-type thermoelectric semiconductor block 2, respectively, to a depth close to the interface between the thermoelectric semiconductor block 1, or 2 and the base 10 or 20 as shown in Fig. 11 such that longitudinal grooves 16, 26 as well as

longitudinal partition walls 17, 27 are formed in a shape resembling the teeth of a comb. Thus, two pairs of n-type grooved composite blocks 13 and p-type grooved composite blocks 23 are fabricated. The positions of the respective longitudinal grooves 16 of the n-type grooved composite
5 block 13 are preferably deviated from those of the corresponding longitudinal grooves 26 of the p-type grooved composite block 23 by a half of the pitch.

Subsequently, a first fitting process is applied to the two pairs of the n-type thermoelectric semiconductor composite blocks 13 and p-type
10 thermoelectric semiconductor composite blocks 23, to which the grooving process described above has been applied, respectively, whereby respective grooved n-type thermoelectric semiconductor composite blocks 13 and respective grooved p-type thermoelectric semiconductor composite blocks 23 are fitted to each other such that grooved surfaces of
15 each pair face each other, and then a first adhesion process is applied to the two pairs of the grooved n-type thermoelectric semiconductor composite blocks 13 and grooved p-type thermoelectric semiconductor composite blocks 23, fitted to each other through the first fitting process, whereby both blocks in each pair are adhered to each other by filling up
20 gaps in fitting parts therebetween with an adhesive insulation member, thereby fabricating two integrated blocks 3' as shown in Fig. 12.

With one of the two integrated blocks 3', the base 20 on the side of the p-type thermoelectric semiconductor block is removed while with the other, the base 10 on the side of the n-type thermoelectric semiconductor
25 block is removed, obtaining a pair of integrated blocks 142A, 142B, with the longitudinal partition walls 17 of the n-type thermoelectric semiconductor and the longitudinal partition walls 27 of the p-type thermoelectric semiconductor, exposed on either the upper surface or under surface thereof, respectively, as shown in Fig. 19.

Subsequently, a process, the same as the second grooving process described in the second embodiment described hereinbefore with reference to Fig. 13, is applied to the pair of the integrated blocks 142A, 142B, from the side where the base 10 or the base 20 is removed, whereby
5 a plurality of grooves at a same pitch are formed in the direction crossing the direction in which the first grooving process has been applied (at right angles, in this embodiment) to a depth close to the interface between the respective thermoelectric semiconductor blocks and the base 20 or the base 10 which has not been removed, thereby
10 fabricating two grooved integrated blocks 143A, 143B, with a plurality of transverse grooves 46 and transverse partition walls 47 formed therein. In this connection, it is preferable that the transverse grooves 46 in one of the grooved integrated blocks, e.g. 143A, are formed such that the positions thereof are deviated by a half of the pitch from those of the
15 transverse grooves 46 formed in the other of the grooved integrated blocks, e.g. 143B.

Subsequently, by applying a second fitting process whereby the two grooved integrated blocks 143A, 143B are fitted to each other such that respective grooved surfaces face each other, and then a second adhesion
20 process, whereby the two grooved integrated blocks 143A, 143B, thus fitted to each other, are adhered together by filling up gaps in fitting parts therebetween with an adhesive insulation member, a doubly integrated block 144 shown in Fig. 21 is fabricated.

In this case, similarly to the case of the third embodiment, the
25 relative position of the n-type thermoelectric semiconductor pieces 51 and p-type thermoelectric semiconductor pieces 52 need to be controlled so as to be arranged like a checkerboard as shown in Fig. 17 when fitting the two grooved integrated blocks 143A, 143B to each other.

As described in the third embodiment, alignment of respective positions can be accomplished by providing a benchmark face on the periphery of each of the grooved integrated blocks. Further, in the fourth embodiment, precision alignment of the respective positions may
5 be attained through direct observation of the respective n-type thermoelectric semiconductor pieces 51 and respective p-type thermoelectric semiconductor pieces 52 by use of a microscope if a transparent member such as glass, or the like is used for the bases 10 and 20.

10 Then, by removing the bases 10 and 20 from the doubly integrated block 144, a thermoelectric device block, the same as the thermoelectric device block 50 shown in Fig. 17 with reference to the third embodiment, is obtained. Subsequently, by providing electrodes as same as the electrodes 61 to 64 illustrated in Fig. 18, a thermoelectric device, the
15 same as the thermoelectric device 60 shown in Fig. 18, is fabricated.

In this embodiment, before the second grooving process is applied to the two integrated blocks 3', the base 20 or 10 on the side where the process of forming the transverse grooves 46 are applied is removed from the respective integrated blocks 3' so that when the pair of the
20 grooved integrated blocks 143A and 143B, with the transverse grooves 46 formed therein, are fitted to each other, the thermoelectric semiconductors as a whole can be fitted to each other, enabling all thermoelectric semiconductors left intact to be put to use for the thermoelectric semiconductor pieces without any wastage thereof.

25 However, since such a step of processing is not essential, the base 10 or the base 20 may be removed after the second grooving process (formation of the transverse grooves) has been applied instead of first removing the base 10 or the base 20.

Fifth Embodiment: Figs. 22 to 24

A fifth embodiment of a method of fabricating a thermoelectric device according to the invention is described hereinafter with reference
5 to Figs. 22 to 24.

In the method according to the fifth embodiment, an n-type thermoelectric semiconductor block 1 and a p-type thermoelectric semiconductor block 2 are bonded, respectively, to each of two large bases 110, 120 (hereinafter referred to as large bases), similarly to the
10 case of the second embodiment, fabricating a pair of an n-type thermoelectric semiconductor composite block 91 and p-type thermoelectric semiconductor composite block 92.

More specifically, the large bases 110, 120 employed in carrying out this embodiment have a surface area larger than a bonded surface
15 area of the respective thermoelectric semiconductor blocks 1, 2.

Similarly to the case of the second embodiment, longitudinal grooves 16, 26, and longitudinal partition walls 17, 27 are formed in the thermoelectric semiconductor blocks 1 and 2, respectively, by applying a first grooving process thereto, fabricating an n-type grooved composite
20 block 181, and p-type grooved composite block 182 shown in Fig. 23. In this instance, the longitudinal grooves 16, 26 are preferably formed to a depth cutting into a portion of the large bases 110, 120, respectively. The reason for this is to make the most of the effect of spacers 190 in a fitting process described hereinafter with reference to Fig. 24 such that n-type
25 as well as p-type thermoelectric semiconductors can be put to use efficiently.

Then, as shown in Fig. 24, a first fitting process is applied, whereby the n-type grooved composite block 181 and p-type grooved composite block 182, shown in Fig. 23, are combined to be fitted to each

other. In this instance, by interposing the spacers 190 between the large bases 110 and 120, a spacing D between the two large bases 110 and 120 is controlled (restrained) accurately to match the height of the longitudinal partition walls 17, 27, composed of a thermoelectric semiconductor, corresponding to the thickness of the respective thermoelectric semiconductor blocks 1, 2.

For example, by equalizing the thickness of the n-type thermoelectric semiconductor block 1, p-type thermoelectric semiconductor block 2, and spacers 190, respectively, the spacing D between the two large bases 110 and 120 can be maintained at a given distance, enabling the longitudinal partition walls 17, 27, composed of the n-type and p-type thermoelectric semiconductors, respectively, to be arranged without unevenness in thickness.

That is, even in case there is no uniformity in the depth of the longitudinal grooves 16, 26, respectively, the n-type and p-type thermoelectric semiconductors can be arranged so as to have no unevenness in thickness with respect to each other by use of the spacers 190 with the result that wasteful polishing or grinding of the n-type and p-type thermoelectric semiconductors can be avoided, enabling improvement in utilization efficiency thereof.

After the first fitting process with the use of the spacers 190, the n-type grooved composite block 181 and p-type grooved composite block 182 are adhered to each other by filling up gaps in fitting parts therebetween with an adhesive insulation member, obtaining an integrated composite block 193 shown in Fig. 24.

Subsequently, a second grooving process is applied, fabricating a grooved integrated composite block with transverse grooves and transverse partition walls formed therein, similar to the grooved integrated block 14 shown in Fig. 13 with reference to the second

embodiment, and insulating resin layers, the same as the insulating resin layers 54 shown in Fig. 14, are formed by filling up the respective transverse grooves with insulating resin, and by curing the insulating resin. Thereafter, by removing the large bases 110, 120, a thermoelectric device block, the same as the thermoelectric device block shown in Fig. 6, is obtained. Further, as shown in Fig 9, by forming various electrodes on the upper as well as under surfaces of the thermoelectric device block, and connecting the respective thermoelectric semiconductor pieces with each other, alternately and in series, the thermoelectric device 6 can be fabricated.

Sixth Embodiment: Figs. 25 and 26

Next, a sixth embodiment of the method of fabricating a thermoelectric device according to the invention using the integrated composite blocks described in carrying out the fifth embodiment is described hereinafter with reference to Figs. 25 and 26.

In the method according to the sixth embodiment, two integrated composite blocks 193 are fabricated by means of processes, the same as the respective processes described in the fifth embodiment with reference to Figs. 22 to 24.

Subsequently, a second grooving process (formation of transverse grooves) is applied to the two integrated composite blocks 193, respectively, whereby a large base 110 or 120, on the side where the second grooving process is applied, is removed in a manner similar to the process as applied in the fourth embodiment described with reference to Fig. 19, fabricating a pair of grooved integrated composite blocks 203A, 203B as shown in Fig. 25, provided with a plurality of transverse grooves 46 as well as transverse partition walls 47 formed therein, respectively, so as to be fitted to each other.

Thereafter, the pair of grooved integrated composite blocks 203A and 203B are fitted to each other while maintaining a spacing between the large bases 110 and 120 at a given distance (a value equivalent to the height of the thermoelectric semiconductors left intact) with the use of
5 spacers 190, and gaps in fitting parts therebetween are filled up with an adhesive insulation member, fabricating a doubly integrated block 213, as shown in Fig. 26.

Then, n-type and p-type thermoelectric semiconductor pieces 51, and 52 are exposed by removing the large bases 110, and 120 of the doubly
10 integrated block 213, thereby obtaining a thermoelectric device block, the same as the thermoelectric device block shown in Fig. 17 with reference to the third embodiment.

Further, by forming electrodes 81 to 84 on the upper as well as under surfaces of the thermoelectric device block as shown in Fig 18,
15 and connecting respective thermoelectric semiconductor pieces 51, 52 with each other, alternately and in series, the thermoelectric device 60 can be fabricated.

Provided that the thermoelectric device 60 fabricated in the third, fourth, or sixth embodiment has dimensions of 10 mm × 10 mm × 2 mm
20 after removing the peripheral region of the thermoelectric device block, 12 mm square, about 3400 couples of thermocouples can be integrated therein.

When a temperature difference of 1.5° C was applied to the thermoelectric device 60, an output voltage at 2.0 V was obtained.

25 Thus, as the thermoelectric device 60 is small enough to be encased in a small portable electronic device such as a wrist watch and yet has an open circuit output voltage at a level high enough to drive a wrist watch, it is possible to drive various portable electronic devices with the thermoelectric device 60 in combination with a booster circuit.

Seventh Embodiment: Figs. 27 to 29

Next, a seventh embodiment of the method of fabricating a thermoelectric device according to the invention is described hereinafter with reference to Figs. 27 to 29.

In the method according to the seventh embodiment of the invention, an n-type thermoelectric semiconductor block 1 and a p-type thermoelectric semiconductor block 2 as shown in Fig. 1 with reference to the first embodiment are first prepared, and as shown in Fig. 27, a metal coated layer 223 is formed on the surfaces of the respective thermoelectric semiconductor blocks 1, 2, that is, at least the surface bonded to a base, and the surface on the opposite side thereof (the surface on which electrodes are formed in a process of forming electrodes applied later on) by means of plating, vapor deposition, sputtering, or the like. Thus, a coated n-type thermoelectric semiconductor block 221, and coated p-type thermoelectric semiconductor block 222 are obtained.

The metal coated layer 223 is either a single layer composed of nickel (Ni), copper (Cu), gold (Au), or the like, or a composite layer composed of single layers stacked up. The metal coated layer 223 is provided in order to improve electrical connection between various wiring electrodes described hereinafter and thermoelectric semiconductors. It is desirable therefore to ensure ohmic contact between the metal coated layer 223 and the n-type thermoelectric semiconductor block 1, as well as the p-type thermoelectric semiconductor block 2, by applying proper heat treatment to the metal coated layer 223 when or after being formed.

The thickness of the metal coated layers 223 may be in the range of about 0.1 to 50 μm . However, in view of the possibility that the height of the coated n-type thermoelectric semiconductor block 221, and coated p-

type thermoelectric semiconductor block 222, respectively, is made even by slightly removing portions of the surfaces of the metal coated layers 223 through a polishing process, or the like in a later step of processing, there will arise problems that if the metal coated layers 223 are
5 excessively thin, it becomes difficult to apply treatment thereto due to too little allowance for polishing while if the same are excessively thick, this is prone to cause a stress-related problem. Accordingly, the thickness of the metal coated layers 223 is preferably in the range of 2 to 10 μm , and an electrolytic or electroless plating method is most suitable for forming
10 a film in a thickness on this order.

In this embodiment, for the metal coated layer 223, a multi-layered film composed of the Ni layer and Au layer, 5 μm in total thickness, is formed by the electrolytic plating method.

For the process shown in Fig. 27 and ones thereafter, any selected
15 from the processes adopted in the second, fourth, fifth, and sixth embodiments can be applied. The seventh embodiment will be described on the assumption processes substantially similar to those applied in the fifth embodiment are adopted.

Accordingly, Fig. 28 corresponds to Fig. 23. That is, an n-type
20 thermoelectric semiconductor composite block formed by bonding the coated n-type thermoelectric semiconductor block 221 to a large base 110, and a p-type thermoelectric semiconductor composite block formed by bonding the coated p-type thermoelectric semiconductor block 222 to a large base 120 are prepared, and longitudinal grooves 16, 26, and
25 longitudinal partition walls 17, 27 are formed in the coated n-type and p-type thermoelectric semiconductor blocks, respectively, by means of the grinding process using a dicing saw, or the polishing process using a wire saw. As a result, a coated n-type grooved composite block 231, and coated p-type grooved composite block 232 are fabricated. In this

instance, portions of the respective metal coated layers 223, at the upper or lower ends of the longitudinal partition walls 17, 27, are left intact as metal layers 233.

5 The coated n-type thermoelectric semiconductor block 221 and coated p-type thermoelectric semiconductor block 222 are bonded to the large base 110 and large base 120, respectively, by use of an adhesive or wax. Further, for the large bases 110 and 120, any material having a hardness to a given degree such as glass, ceramic, plastics, metal, or the like, may be employed.

10 The pitch at which the longitudinal grooves 16, 26 are formed, and the width and depth of the longitudinal grooves 16, 26 are substantially as described with reference to Fig. 23, except that the depth thereof somewhat differs. In this embodiment, the longitudinal grooves 16, 26 are formed to a depth either of the interface between the coated n-type
15 thermoelectric semiconductor block 221 and the large base 110 or between the coated p-type thermoelectric semiconductor block 222 and the large base 120, or so as to be cut into the large base 110 or 120.

The reason for this is that in carrying out a process of combining the coated n-type grooved composite block 231 with the coated p-type
20 grooved composite block 232, the surfaces of the metal layers 233 of the respective coated grooved composite blocks are rendered to be flush with each other.

Subsequently, as described in the fifth embodiment with reference to Fig. 24, the coated n-type grooved composite block 231 and coated p-type
25 grooved composite block 232 are combined to be fitted to each other, and gaps in fitting parts therebetween are filled with adhesive insulation members, forming adhesion layers 32 shown in Fig. 29, so that an integrated composite block is fabricated through adhesion of the coated grooved composite blocks with each other.

Thereafter, a second grooving process is applied to the integrated composite block, whereby a grooved integrated composite block with transverse grooves as well as transverse partition walls formed therein is formed, and by filling up the respective transverse grooves with
5 insulating resin and curing the same, insulating resin layers, the same as the insulating resin layers 54 shown in Fig. 5, are formed.

After removing the large bases 110, 120, a thermoelectric device block 5 as shown in Fig. 6 is obtained. Further, by forming respective electrodes 81, 82, as shown in Fig. 29, on both the upper and under
10 surfaces of the thermoelectric device block, and connecting n-type thermoelectric semiconductor pieces 51 and p-type thermoelectric semiconductor pieces 52 to each other, alternately and in series, a thermoelectric device 80 can be fabricated.

Fig. 29 illustrates the sectional shape of the thermoelectric device
15 80 according to the seventh embodiment of the invention, corresponding to the plan view shown in Figs. 9 and 18, respectively. In this connection, for forming the upper surface electrode 81 and the under surface electrode 82, the vapor deposition film described hereinbefore is normally used. However, the method according to this embodiment may
20 be characterized by use of an electrically conductive paste such as silver paste.

Electrical connection between the electrically conductive paste and such semiconductor as used in the method of the invention is generally prone to create a problem due to high contact resistance. Therefore,
25 with the construction according to the invention, the electrically conductive paste is not suitable for use for wiring electrodes. However, by providing the metal layer 233 shown in the seventh embodiment, the contact resistance described can be reduced to a negligible level.

Consequently, the electrically conductive paste can be used for the upper surface electrode 81 and the under surface electrode 82.

The method according to this embodiment has an advantage in that productivity is remarkably improved because with the use of the electrically conductive paste, the electrodes can be formed through patterning by use of a screen printing method.

Eighth Embodiment: Figs. 30 and 31

Next, an eighth embodiment of the method of fabricating a thermoelectric device according to the invention is described hereinafter with reference to Figs. 30 and 31.

The method according to the eighth embodiment is described starting from the stage of a thermoelectric device block (for example, the same as the thermoelectric device block 5 shown in Fig. 6) prior to the wiring process described in the first to the fifth embodiments. That is, respective processes applied up to this stage in this embodiment are the same as those in the case of the respective embodiments described above.

After the formation of the thermoelectric device block described above, metal layers 233, the same as in the case of the seventh embodiment, are formed on at least the surfaces of n-type thermoelectric semiconductor pieces 51 and p-type thermoelectric semiconductor pieces 52, where wiring electrodes are to be formed.

As a result, a thermoelectric device block 253 shown in Fig. 30 illustrating the sectional view thereof is fabricated.

In this embodiment, the metal layers 233 are preferably deposited by a plating method whereby a single-layered film composed of Ni, Au, Cu, or the like, or a multi-layered film composed of the aforesaid films, is formed. In particular, an electroless plating is most suitable whereby selective plating can be applied to exposed surfaces of the thermoelectric

semiconductor pieces 51, 52, taking advantage of selectivity in the condensation coefficient of Pd (palladium) acting as a catalyst on the surfaces of the thermoelectric semiconductor pieces 51, 52, adhesive layers 32, and insulating resin layers 54.

5 Further, it is preferable not to form the metal layer 233 on the side faces of the thermoelectric semiconductor pieces on the periphery of the thermoelectric device block (for example, the thermoelectric device block 5 shown in Fig. 6) prior to the wiring process being applied thereto, which is the starting point of description of this embodiment. Hence, in
10 this embodiment, a coated layer 254 composed of the same material as is used for the adhesive layers 32, or the insulating resin layers 54, is formed on the peripheral face (the side face) of the thermoelectric device block.

Fig. 31 shows a thermoelectric device 80, completed by forming
15 upper surface electrodes 81 and under surface electrodes 82 on the thermoelectric device block 253 shown in Fig. 30 by use of the electrically conductive paste as described in the seventh embodiment.

The method according to this embodiment, whereby the metal layers 233 are formed at a later stage of processing, has still an
20 advantage in that productivity is remarkably improved because the electrically conductive paste can be used as in the case of the seventh embodiment, and the electrodes can be formed through patterning by use of the screen printing method.

25 Ninth Embodiment: Figs. 32 and 33

Next, a ninth embodiment of the method of fabricating a thermoelectric device according to the invention is described hereinafter with reference to Figs. 32 and 33.

Fig. 32 shows a provisional thermoelectric device 270 fabricated according to the ninth embodiment, which is substantially the same as the thermoelectric device 6, 60, or 80 described in the respective embodiments described in the foregoing and fabricated by substantially the same processes except that in place of the adhesive layers 32, and the insulating resin layers 54, provisional fixture layers 271 are provided therein.

As opposed to the embodiments described in the foregoing, wherein the adhesive layers 32 and the insulating resin layers 54 are among the components of the thermoelectric device in the final form, the insulating resin layers 54 are not included in the components of the thermoelectric device in the final form in the case of the method according to the ninth embodiment.

Accordingly, in place of the adhesive layers 32 and the insulating resin layers 54, the provisional fixture layers 271 are formed for provisionally securing the n-type thermoelectric semiconductor pieces 51 and p-type thermoelectric semiconductor pieces 52, and are removed later on. The provisional fixture layers 271 are formed by filling up gaps in the fitting parts after the fitting process is applied to the pair of the grooved blocks or by filling up the transverse grooves 47 after being formed as shown in Figs. 4, 13, and the like, with a provisional fixture material in the same way as for the formation of the adhesive layers 32, and the insulating resin layers 54. For the provisional fixture material, an adhesive material removable by heating or by use of a solvent such as wax is employed.

In the method of fabrication according to the ninth embodiment, an adhesive resin such as epoxy resin is applied as shown in Fig. 33 to the entire upper as well as under surfaces of the provisional thermoelectric device 270 shown in Fig. 32, thereby forming insulating

fixture layers 284. The provisional thermoelectric device 270 is then sandwiched between a heat radiation plate 281 and a heat absorption plate 282, and fixedly attached thereto via the insulating fixture layers 284 integrally formed.

5 For the heat radiation plate 281 and heat absorption plate 282, a material having high thermal conductivity, that is, a metal or ceramic, is used.

Particularly in the case of a metal being selected for this purpose, a treatment to form an insulating oxide film may preferably be applied to
10 the surface of the metal because of the risk of an accidental short circuit occurring between upper surface electrodes 81 and the heat radiation plate 281, or between under surface electrodes 82 and the heat absorption plate 282 if the insulating fixture layers 284 is rendered too thin.

Thereafter, as shown in Fig. 33, after securing the provisional
15 thermoelectric device 270 onto the heat radiation plate 281 and heat absorption plate 282, the provisional fixture layers 271 are removed by use of heat or a solvent, thereby fabricating a thermoelectric device 280 provided with voids 283 created in regions vacated as above.

With the construction of the thermoelectric device 280 according to
20 this embodiment, heat conduction by materials other than the thermoelectric semiconductors between the heat radiation plate 281 and the heat absorption plate 282 is largely inhibited because of the very low thermal conductivity of the air in the voids 283, enhancing the performance of the thermoelectric device.

25 In the aforesaid embodiment, in place of both the adhesive layers 32 provided in the fitting parts between the n-type and p-type thermoelectric semiconductor grooved blocks and the insulating resin layers 54 provided in the transverse grooves formed after the pair of the grooved blocks are integrated, the provisional fixture layers 271 are

provided. However, only either of the adhesive layers or the insulating resin layers may be substituted by the provisional fixture layers 271, and after sandwiching the provisional thermoelectric device 270 between the heat radiation plate 281 and heat absorption plate 282 so as to be
5 integrally secured by the insulating fixture layers 284, the provisional fixture layers 271 may be removed so that either the adhesive layers 32 or the insulating resin layers 54 are left intact.

This will enable the thermoelectric device to maintain sufficient strength while enhancing the performance thereof.

10 With the thermoelectric device 280 shown in Fig. 33, when used for generation of power, the heat absorption plate 282 is positioned on the lower temperature side.

15 Another Embodiment of a Process of Fabricating a Thermoelectric Semiconductor Grooved Block: Fig. 34

Now, another embodiment of a process of fabricating a thermoelectric semiconductor grooved block according to the invention is described hereinafter with reference to Fig. 34.

With the first embodiment or the third embodiment described
20 hereinbefore, in the process of fabricating the n-type and p-type thermoelectric semiconductor grooved blocks, the plurality of grooves parallel with each other are formed in the n-type and p-type thermoelectric semiconductor blocks 1 and 2, respectively, by machining using the wire saw or the like, thereby fabricating the n-type
25 thermoelectric semiconductor grooved block 11 and p-type thermoelectric semiconductor grooved block 21.

However, the n-type thermoelectric semiconductor grooved block 11 and p-type thermoelectric semiconductor grooved block 21 can also be fabricated by molding n-type thermoelectric semiconductor material and

p-type thermoelectric semiconductor material separately into a mold (metal mold) for the grooved block, and then sintering the molded materials.

5 In such a process of fabricating the grooved blocks as described above, a compound used for injection molding is produced by adding a mixture as an organic binder, consisting of, for example, ethylene-vinyl-acetate - polybutylmethacrylate - polystyrene copolymer, atactic polypropylene, paraffin wax, and dibutyl phthalate to pulverized
10 powders of a thermoelectric semiconductor material (for example, in the case of the p-type thermoelectric semiconductor material, pulverized powders of BiTeSb crystals as in the case of the first embodiment) on the order of 1 μ m in average grain size, and kneading the same with the use of a pressurized kneader. A suitable mixing ratio of the pulverized
15 powders to the organic binder is 5 to 15 wt parts of the organic binder against 100 wt parts of the pulverized powders.

The compound for injection molding thus produced is molded by use of an injection molding machine, and Fig. 34 is a sectional view of a metal mold with which molding is performed.

20 In this case, the compound for injection molding is pressurized and filled from a nozzle 304 into a molding cavity 308 formed in the shape of the grooved block inside a movable mold 301 via a sprue 306 of a fixed mold 303 and a gate 307 of an intermediate mold 302.

A molded body formed in the molding cavity 308 as described above is pushed out by ejector pins 305, and taken out after the movable block
25 301 is shifted and separated from the intermediate mold 302. The molding cavity 308 is designed to have dimensions about 20% larger than those of the grooved block to allow for shrinkage occurring to the molded body during the sintering thereof.

The molded bodies are then placed side by side on a flat plate made of alumina in a vacuum furnace at 400° C for a retention time of 1 hour, obtaining provisional sintered bodies with organic binders substantially removed. In the final step, the provisional sintered bodies are again
5 placed side by side on the flat plate made of alumina, and subjected to a sintering process at 470° C for a duration of 3 hours in an electric furnace in a hydrogen-flow atmosphere, obtaining sintered bodies composed of the n-type or p-type thermoelectric semiconductors, respectively. The sintered bodies are the n-type grooved block 11, and p-
10 type grooved block 21, respectively.

Supplementary Explanation

Various embodiments of the method of fabricating the thermoelectric device according to the invention have been described in
15 the foregoing, and every one of the embodiments is based on the construction wherein the thermoelectric semiconductor pieces 51, 52 are all arranged in a matrix fashion. That is, all the embodiments have made a point of applying the process of forming the transverse grooves after the process of forming the longitudinal grooves, then the process of
20 exposing the thermoelectric semiconductor pieces, and further, the process of forming the electrodes for wiring and the like, thus completing the fabrication of the thermoelectric device.

However, in the case where the thermocouples, even though small in number, can be effectively utilized, the thermoelectric device
25 may be completed in the respective embodiments described hereinbefore by applying the process of exposing the thermoelectric semiconductor pieces without applying the process of forming the transverse grooves, and then, by forming the electrodes for wiring and the like.

In the case of adopting such steps of processing, the finished product will be the thermoelectric device of a construction wherein thin layers composed of n-type and p-type thermoelectric semiconductors, respectively, are alternately arranged and connected to each other in series.

It is obvious that the method of fabricating the thermoelectric device according to the invention is sufficiently effective for fabrication of the thermoelectric device having the construction described above.

As described in each of the aforesaid embodiments, the longitudinal grooves as well as the transverse grooves are formed by use of the wire saw or the dicing saw, and in the case that the grooving process is applied by a grinding method using the wire saw, the bottom surfaces of the longitudinal grooves as well as the transverse grooves become a circular arc in actual shape.

Although the longitudinal grooves have arc-shaped bottom surfaces while the longitudinal partition walls have rectangular top ends, there will arise no particular problem when the n-type grooved block is combined with the p-type grooved block to be fitted to each other because gaps formed are filled up with the adhesive.

Further, when the transverse grooves are formed by use of the wire saw after the integrated block has been formed, the bottom surfaces of the transverse grooves become a circular arc in shape. However, there will arise no problem in this case either, because the transverse grooves are filled up with the insulating resin.

As is evident from the foregoing description, in the method of fabricating the thermoelectric device according to the invention, the grooved blocks composed of the n-type and p-type thermoelectric semiconductors, respectively, are fabricated by applying a precision machining process to thermoelectric semiconductor members, or by

applying a precision molding process to thermoelectric semiconductor material, and then, by applying an integration process of combining the grooved blocks so as to be fitted to each other, the thermoelectric semiconductor members can always be handled in the form of a unit
5 (block). Hence, the thermoelectric device incorporating the thermocouples composed of a multitude of thermoelectric semiconductor pieces can be fabricated without applying processes such as a process of forming thermoelectric semiconductors into a thin sheet-like shape, a process of forming thermoelectric semiconductors into a
10 kenzan-like shape by applying a fine grooving process, and the like wherein the thermoelectric semiconductor materials are susceptible to undergo breakage.

Accordingly, an ultra small thermoelectric device capable of outputting a high voltage can be fabricated easily and efficiently, making
15 it possible to utilize power generated by temperature differences occurring in a portable electronic device such as a wrist watch.

INDUSTRIAL APPLICABILITY

With the method of fabricating a thermoelectric device according
20 to the invention, a thermoelectric device small in size, incorporating a multitude of thermocouples formed therein, and capable of outputting a high voltage can be fabricated easily and efficiently. As a high output voltage can be produced by putting the thermoelectric device to use as a small thermoelectric generator, the thermoelectric device installed in a
25 portable miniature electronic device such as a wrist watch and the like can be used as a power supply for electric power generated by temperature differences.

The thermoelectric device can also be used in fabrication of a high performance cooling system of small size, which is quite useful as a

portable refrigerator, or a localized cooler for lasers, integrated circuits, and the like.



CLAIMS

1. A method of fabricating a thermoelectric device comprising:

a grooved block fabrication process of forming grooved blocks composed of an n-type thermoelectric semiconductor and p-type thermoelectric semiconductor, respectively, each provided with a plurality of grooves formed at a same pitch and parallel with each other, leaving a depthwise portion of respective grooved blocks intact;

a fitting process of fitting the grooved blocks composed of the n-type thermoelectric semiconductor and p-type thermoelectric semiconductor formed, respectively, by said grooved block fabrication process to each other such that surfaces of the respective grooved blocks, with the grooves formed thereon, face each other;

an adhesion process of forming an integrated block by adhering the grooved block composed of the n-type thermoelectric semiconductor and the grooved block composed of the p-type thermoelectric semiconductor, fitted to each other by said fitting process, to each other after filling up gaps in fitting parts between the respective grooved blocks with an adhesive insulation member; and

a thermoelectric semiconductor pieces exposure process of exposing n-type and p-type thermoelectric semiconductor pieces by removing all portions of the integrated block formed by said adhesion process, other than the fitting parts where the grooved block composed of the n-type thermoelectric semiconductor and the grooved block composed of the p-type thermoelectric semiconductor are fitted to each other.

2. A method of fabricating a thermoelectric device comprising:

a grooved block fabrication process of forming grooved blocks composed of an n-type thermoelectric semiconductor and p-type thermoelectric semiconductor, respectively, each provided with a





plurality of grooves formed at a same pitch and parallel with each other, leaving a depthwise portion of respective grooved blocks intact;

a fitting process of fitting the grooved blocks composed of the n-type thermoelectric semiconductor and p-type thermoelectric semiconductor formed, respectively, by said grooved block fabrication process to each other such that surfaces of the respective grooved blocks, with the grooves formed thereon, face each other;

an adhesion process of forming an integrated block by adhering the grooved block composed of the n-type thermoelectric semiconductor and the grooved block composed of the p-type thermoelectric semiconductor, fitted to each other by said fitting process, to each other after filling up gaps in fitting parts between the respective grooved blocks with an adhesive insulation member;

a second grooving process of forming a plurality of grooves in the integrated block formed by said adhesion process, in the direction crossing the direction of the grooves formed by said grooved block fabrication process, leaving a depthwise portion of the integrated block intact;

a solidification process of filling up the grooves formed by said second grooving process with an adhesive insulation member and solidifying the same; and

a thermoelectric semiconductor pieces exposure process of exposing n-type and p-type thermoelectric semiconductor pieces by removing all portions of the integrated block wherein the adhesive insulation member filling up the grooves is solidified in said solidification process, other than the fitting parts where the grooved block composed of the n-type thermoelectric semiconductor and the grooved block composed of the p-type thermoelectric semiconductor are fitted to each other.





3. A method of fabricating a thermoelectric device comprising:

a grooved block fabrication process of forming two pairs of grooved blocks composed of an n-type thermoelectric semiconductor and p-type thermoelectric semiconductor, respectively, provided with a plurality of
5 grooves formed at a same pitch and parallel with each other, respectively, leaving a depthwise portion of respective grooved blocks intact;

a first fitting process of fitting each pair of the grooved blocks composed of the n-type thermoelectric semiconductor and the grooved
10 block of the p-type thermoelectric semiconductor, formed by said grooved block fabrication process, to each other such that surfaces with the grooves formed thereon face each other;

a first adhesion process of forming two integrated blocks by filling up gaps in fitting parts between each pair of the grooved blocks
15 composed of the n-type thermoelectric semiconductor and the p-type thermoelectric semiconductor, respectively, fitted to each other by said first fitting process, with adhesive insulation members; and solidifying the same;

a grooving process of forming two grooved integrated blocks by
20 forming in each of the two integrated blocks a plurality of grooves at a same pitch and in the direction crossing the direction of the grooves formed by said grooved block fabrication process, leaving a depthwise portion of respective integrated blocks intact;

a second fitting process of fitting the two grooved integrated blocks
25 to each other such that surfaces with the grooves thus formed thereon face each other;

a second adhesion process of forming a second integrated block by filling gaps in fitting parts between the two grooved integrated blocks

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fitted to each other by said fitting process with adhesive insulation members, and solidifying the same; and

a thermoelectric semiconductor pieces exposure process of exposing n-type and p-type thermoelectric semiconductor pieces by
5 removing all depthwise portions of the second integrated block, other than the fitting parts.

4. A method of fabricating a thermoelectric device according to one of Claims 1 to 3, wherein the grooved block fabrication process is a process of forming the grooved block of the n-type thermoelectric
10 semiconductor and grooved block of the p-type thermoelectric semiconductor by applying a grooving process to an n-type thermoelectric semiconductor block and p-type thermoelectric semiconductor block, respectively, such that a plurality of grooves are formed at a same pitch and parallel with each other, leaving a
15 depthwise portion of said respective blocks intact.

5. A method of fabricating a thermoelectric device according to one of Claims 1 to 3, wherein the grooved block fabrication process is a process of forming the grooved block of the n-type thermoelectric semiconductor and grooved block of the p-type thermoelectric
20 semiconductor by forming a molded n-type thermoelectric semiconductor material and molded p-type thermoelectric semiconductor material by use of a mold for the grooved block, respectively, and sintering the same.

6. A method of fabricating a thermoelectric device according to
25 one of Claims 1 to 5, further comprising an electrode forming process of forming electrodes for connecting the n-type and p-type thermoelectric semiconductor pieces exposed with each other alternately and in series after the thermoelectric semiconductor pieces exposure process.

7. A method of fabricating a thermoelectric device comprising:



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a first grooving process applied to an n-type thermoelectric semiconductor composite block prepared by bonding an n-type thermoelectric semiconductor block to a base and a p-type thermoelectric semiconductor composite block prepared by bonding a p-type thermoelectric semiconductor block to a base, for forming a plurality of grooves in the n-type thermoelectric semiconductor block and the p-type thermoelectric semiconductor block, respectively, at a same pitch, and to a depth close to the interface between the respective thermoelectric semiconductor blocks and the base thereof;

10 a fitting process of fitting the n-type thermoelectric semiconductor composite block and p-type thermoelectric semiconductor composite block, with the grooves formed by said first grooving process, respectively, to each other such that respective grooved surfaces face each other;

15 an adhesion process of forming an integrated block by filling gaps in fitting parts between the n-type thermoelectric semiconductor composite block and p-type thermoelectric semiconductor composite block, fitted to each other by said fitting process, with adhesive insulation members so as to adhere the n-type thermoelectric semiconductor composite block and p-type thermoelectric semiconductor composite block to each other;

25 a second grooving process of forming a plurality of grooves in the direction crossing the direction of the grooves formed by said first grooving process, and to a depth close to the interface between the respective thermoelectric semiconductor blocks and the base thereof in the integrated block formed by said adhesion process;

a solidification process of filling up the grooves formed by said second grooving process with insulation members, and solidifying the same; and



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a thermoelectric semiconductor pieces exposure process of exposing n-type and p-type thermoelectric semiconductor pieces by removing the respective bases of the integrated blocks wherein the grooves are filled with the insulation member and the insulation member is then solidified in said solidification process.

8. A method of fabricating a thermoelectric device according to Claim 7, characterized in that the bases of the n-type thermoelectric semiconductor composite block and the p-type thermoelectric semiconductor composite block, respectively, have a surface area larger than an area of a bonded portion of the surface of the respective thermoelectric semiconductor blocks, and in the fitting process, spacers are interposed between portions of the bases of the n-type thermoelectric semiconductor composite block and the p-type thermoelectric semiconductor composite block, respectively, where the respective thermoelectric semiconductor blocks do not exist, so that a spacing between the bases is controlled to be substantially equivalent to thicknesses of the respective thermoelectric semiconductor blocks.

9. A method of fabricating a thermoelectric device comprising:

a first grooving process applied to two n-type thermoelectric semiconductor composite blocks prepared by bonding an n-type thermoelectric semiconductor block to a base, respectively, and two p-type thermoelectric semiconductor composite blocks prepared by bonding a p-type thermoelectric semiconductor block to a base, respectively, for forming a plurality of grooves at a same pitch, and to a depth close to the interface between the respective thermoelectric semiconductor blocks and the base thereof, in the n-type thermoelectric semiconductor block and the p-type thermoelectric semiconductor block, respectively;



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a first fitting process of fitting the two pairs of the n-type thermoelectric semiconductor composite block and p-type thermoelectric semiconductor composite block, with the grooves formed therein, respectively, by said first grooving process to each other, respectively,
5 such that respective grooved surfaces face each other;

a first adhesion process of forming two integrated blocks by adhering the two pairs of the n-type thermoelectric semiconductor composite blocks and p-type thermoelectric semiconductor composite blocks to each other, respectively, by filling gaps in fitting parts between
10 the respective n-type thermoelectric semiconductor composite blocks and p-type thermoelectric semiconductor composite blocks, fitted to each other by said first fitting process, with adhesive insulation members;

a second grooving process of forming two grooved integrated blocks by forming a plurality of grooves at a same pitch in the two
15 integrated blocks formed, respectively, by said first adhesion process, in the direction crossing the direction of the grooves formed by said first grooving process, and to a depth close to an interface between the respective thermoelectric semiconductor blocks and the base thereof;

a second fitting process of fitting the two grooved integrated blocks
20 to each other such that respective grooved surfaces face each other;

a second adhesion process of forming a second integrated block by adhering the two grooved integrated blocks, fitted to each other by said second fitting process, to each other by filling gaps in fitting parts between the two grooved integrated blocks with adhesive insulation
25 members; and

a thermoelectric semiconductor pieces exposure process of exposing n-type and p-type thermoelectric semiconductor pieces by removing the respective bases of the second integrated block.





10. A method of fabricating a thermoelectric device according to Claim 9, characterized in that bases having a surface area larger than an area of a bonded portion of the surface of the respective thermoelectric semiconductor blocks are used for the base of the n-type thermoelectric semiconductor composite block and the p-type thermoelectric semiconductor composite block, respectively, and spacers are interposed between portions of the respective bases of the n-type thermoelectric semiconductor composite block and the p-type thermoelectric semiconductor composite block to be fitted to each other, where the respective thermoelectric semiconductor blocks do not exist, controlling a spacing between the bases to be substantially equivalent to thicknesses of the respective thermoelectric semiconductor blocks in the first fitting process, spacers being further interposed between portions of the respective bases of the two integrated grooved blocks to be fitted to each other, where the respective thermoelectric semiconductor blocks do not exist, controlling a spacing between the bases to be substantially equivalent to the thickness of the respective thermoelectric semiconductor blocks in the second fitting process.

11. A method of fabricating a thermoelectric device according to one of Claims 7 to 10, further comprising an electrode forming process of forming electrodes for connecting the exposed n-type and p-type thermoelectric semiconductor pieces to each other alternately and in series, applied after the thermoelectric semiconductor pieces exposure process.

12. A method of fabricating a thermoelectric device according to one of Claims 1, 2 or 7, characterized in that an insulation film is formed on at least one of plural fitting surfaces of a pair of thermoelectric semiconductor blocks to be fitted to each other in the fitting process.

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13. A method of fabricating a thermoelectric device according to one of Claims 1, 2 or 7, characterized in that the insulation member for filling up the gaps in the fitting parts in the adhesion process is an adhesive insulation member with insulating spacers dispersed therein.

5 14. A method of fabricating a thermoelectric device according to Claim 3 or 9, characterized in that an insulation film is formed on at least one of plural fitting surfaces of a pair of thermoelectric semiconductor blocks to be fitted to each other in at least either of the first fitting process or the second fitting process.

10 15. A method of fabricating a thermoelectric device according to Claim 3 or 9, characterized in that the insulation member for filling up the gaps in the fitting parts in at least either of the first adhesion process or the second adhesion process is an adhesive insulation member with insulating spacers dispersed therein.

15 16. A method of fabricating a thermoelectric device according to one of Claims 7 to 10, characterized in that before the n-type thermoelectric semiconductor block and the p-type thermoelectric semiconductor block are bonded to the bases, respectively, a metal coated layer is formed on the surface of the respective thermoelectric
20 semiconductor blocks, bonded to the respective bases, and on the surface thereof on the opposite side.

17. A method of fabricating a thermoelectric device according to Claim 16, further comprising an electrode formation process of forming electrodes for connecting the exposed n-type and p-type thermoelectric
25 semiconductor pieces to each other alternately and in series by use of an electrically conductive paste applied on the metal coated layer after the thermoelectric semiconductor pieces exposure process.

18. A method of fabricating a thermoelectric device according to one of Claims 1, 2, 3, 7, or 9, further comprising a metal layer formation





process of forming metal layers on respective surfaces of the exposed n-type and p-type thermoelectric semiconductor pieces, where the electrodes are formed, and an electrode formation process of forming the electrodes for connecting the exposed n-type and p-type thermoelectric semiconductor pieces to each other alternately and in series over the metal layers, said processes being applied after the thermoelectric semiconductor pieces exposure process.

19. A method of fabricating a thermoelectric device according to Claim 18, characterized in that the electrodes are formed by use of an electrically conductive paste in the electrode formation process.

20. A method of fabricating a thermoelectric device according to Claim 1, characterized in that provisional fixture layers as insulation members for filling up the gaps in the fitting parts are formed using a material removable by heating or by use of a solvent in the adhesion process;

said method further comprising an electrode formation process of forming electrodes for connecting the exposed n-type and p-type thermoelectric semiconductor pieces to each other alternately and in series after the thermoelectric semiconductor pieces exposure process, fabricating a provisional thermoelectric device, and thereafter performing a process of fixedly attaching a heat radiation plate to one of the surfaces of the provisional thermoelectric device, where the electrodes are formed, and a heat absorption plate to the other via an insulating fixture layers, respectively, and a process of removing the provisional fixture layers either by heating or by use of a solvent after said preceding process.

21. A method of fabricating a thermoelectric device according to Claim 2 or 7, characterized in that provisional fixture layers are formed using a material removable by heating or by use of a solvent as at least





either of the insulation members for filling up the gaps in the fitting parts in the adhesion process or the insulation members for filling up the grooves in the solidification process;

said method further comprising an electrode formation process of forming electrodes for connecting the exposed n-type and p-type thermoelectric semiconductor pieces to each other alternately and in series after the thermoelectric semiconductor pieces exposure process, fabricating a provisional thermoelectric device, and thereafter performing a process of fixedly attaching a heat radiation plate to one of the surfaces of the provisional thermoelectric device, where the electrodes are formed, and a heat absorption plate to the other via an insulating fixture layers, respectively, and a process of removing the provisional fixture layers either by heating or by use of a solvent after said preceding process.

22. A method of fabricating a thermoelectric device according to Claim 3 or 9, characterized in that provisional fixture layers as insulation members for filling up the gaps in the fitting parts are formed using a material removable by heating or by use of a solvent in the first adhesion process or the second adhesion process;

said method further comprising an electrode formation process of forming electrodes for connecting the exposed n-type and p-type thermoelectric semiconductor pieces to each other alternately and in series after the thermoelectric semiconductor pieces exposure process, fabricating a provisional thermoelectric device, and thereafter performing a process of fixedly attaching a heat radiation plate to one of the surfaces of the provisional thermoelectric device, where the electrodes are formed, and a heat absorption plate to the other via an insulating fixture layers, respectively, and a process of removing the



provisional fixture layers either by heating or by use of a solvent after said preceding process.

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FIG. 1

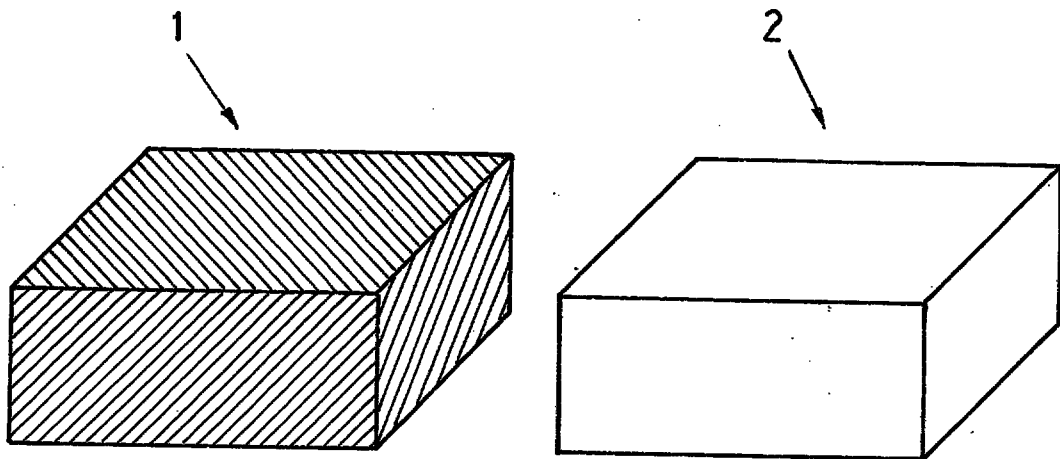


FIG. 2

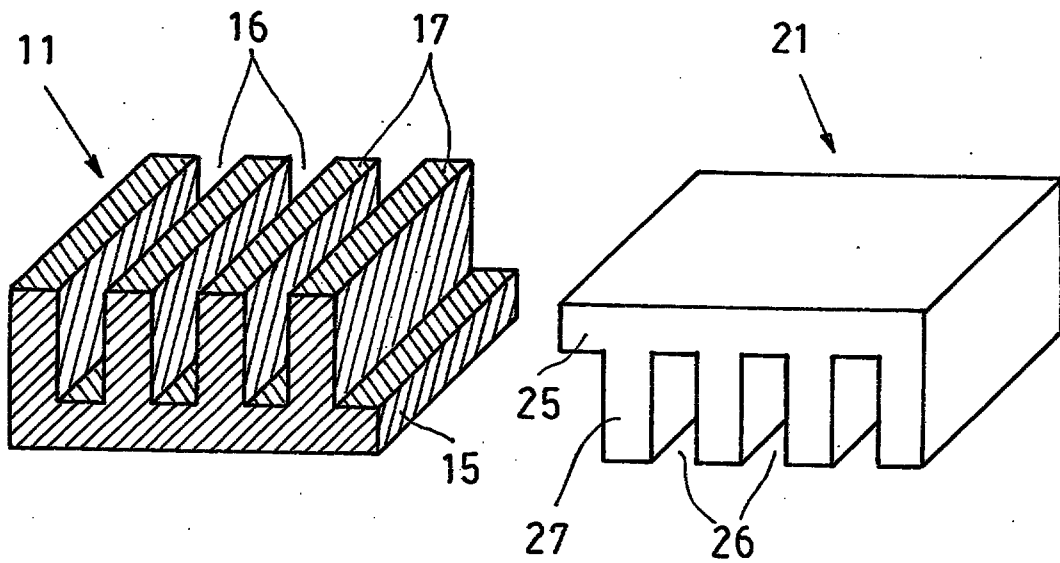


FIG. 3

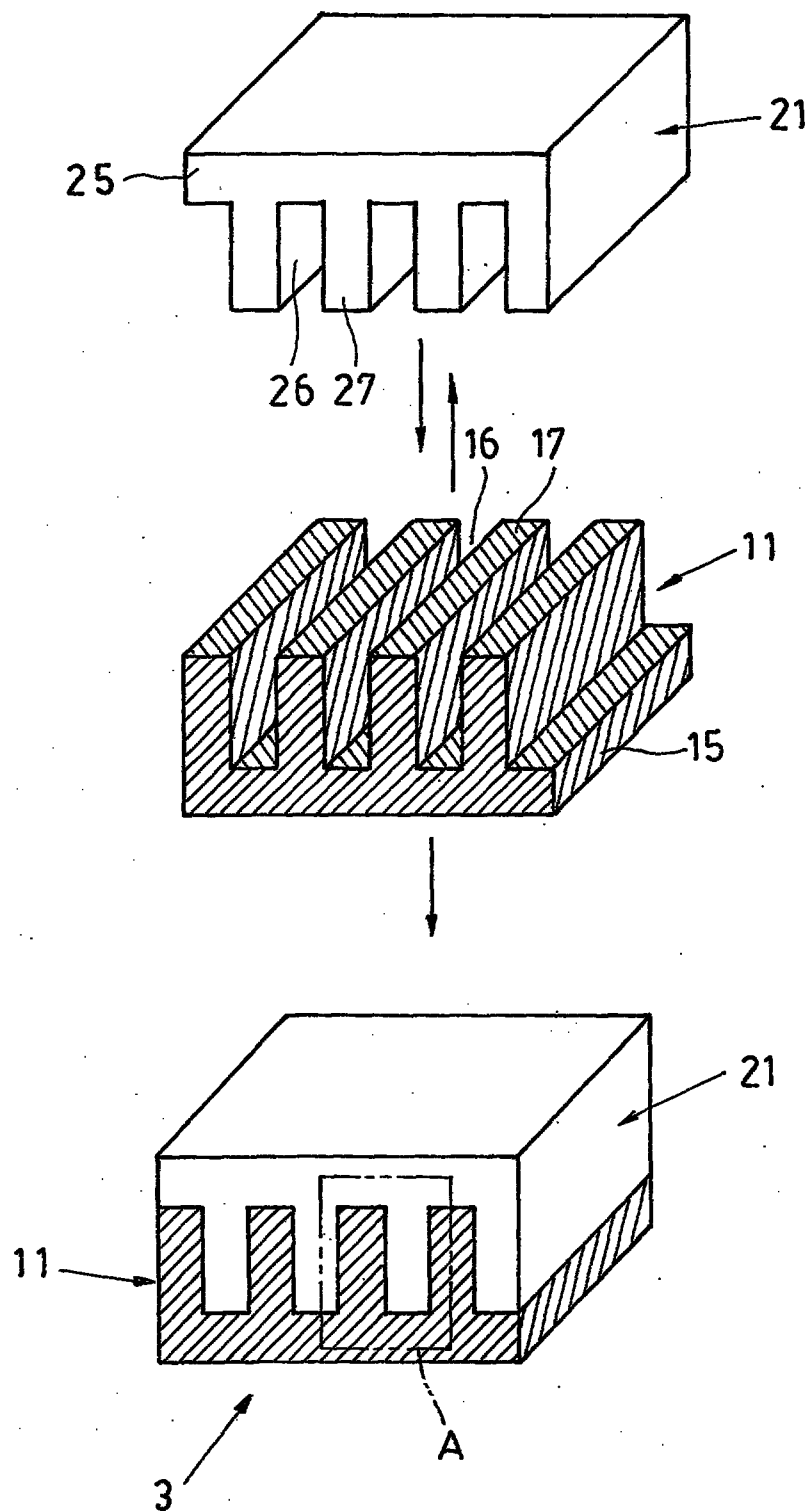


FIG. 4

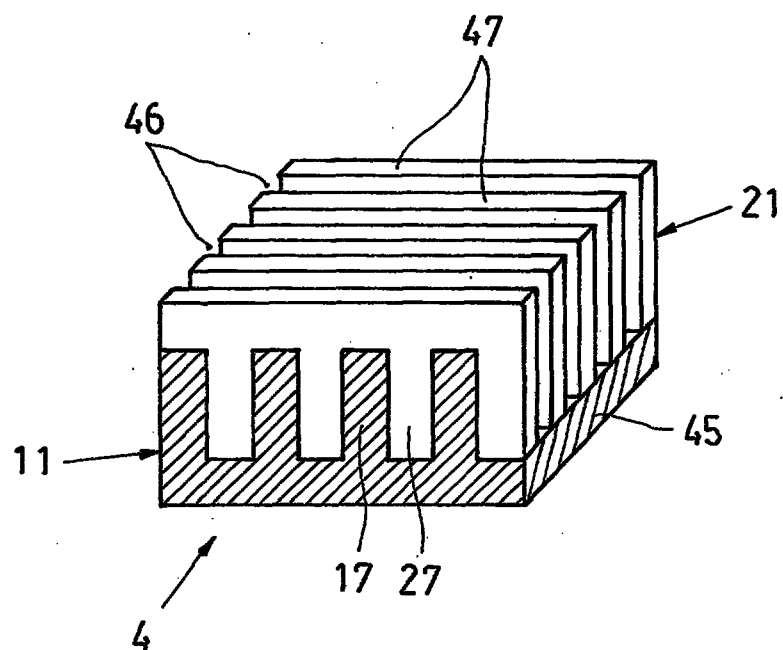


FIG. 5

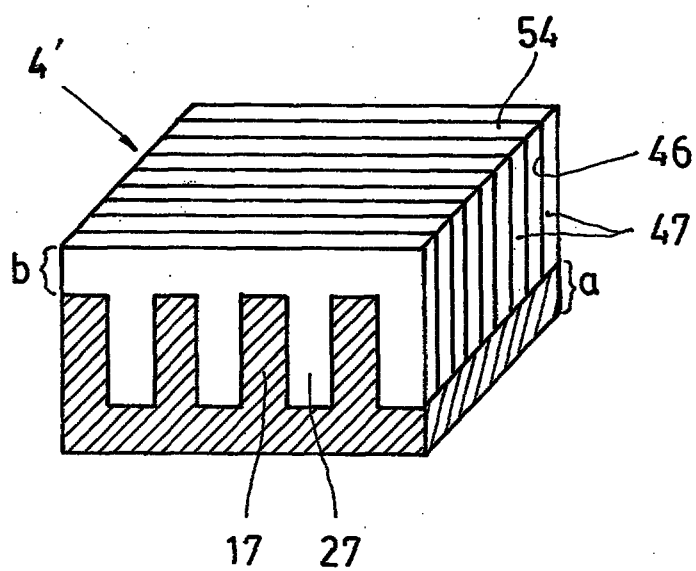


FIG. 6

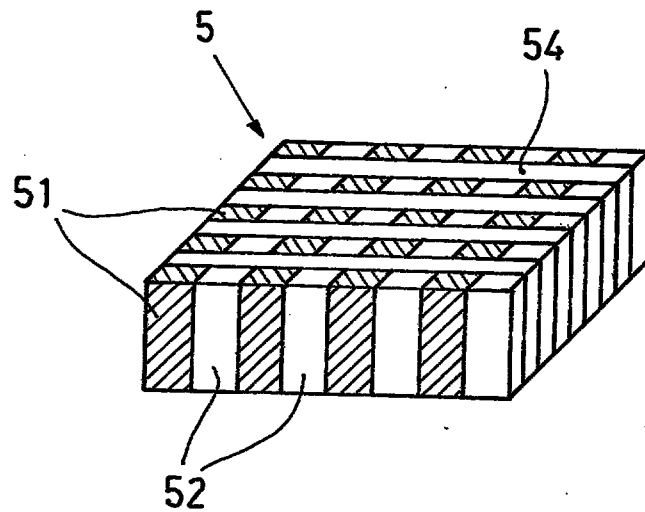


FIG. 7

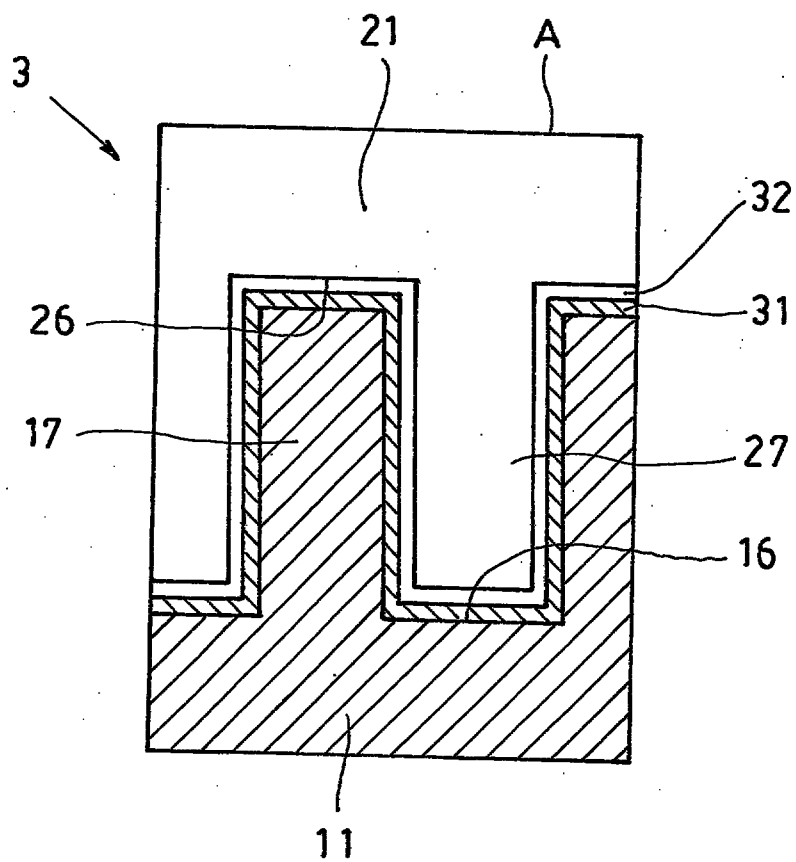


FIG. 8

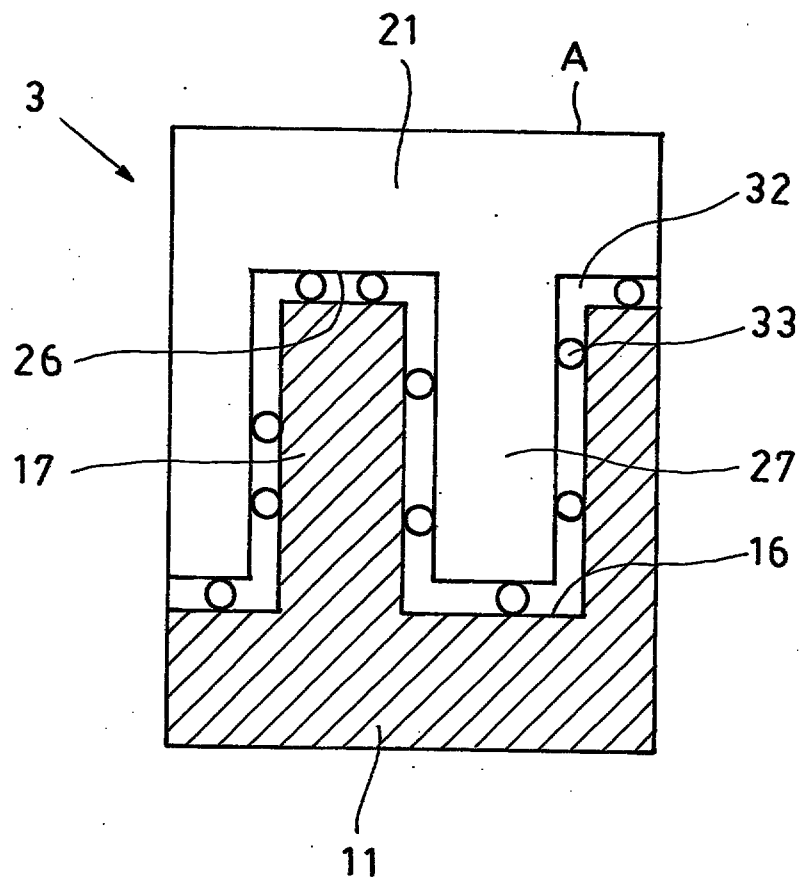


FIG. 9

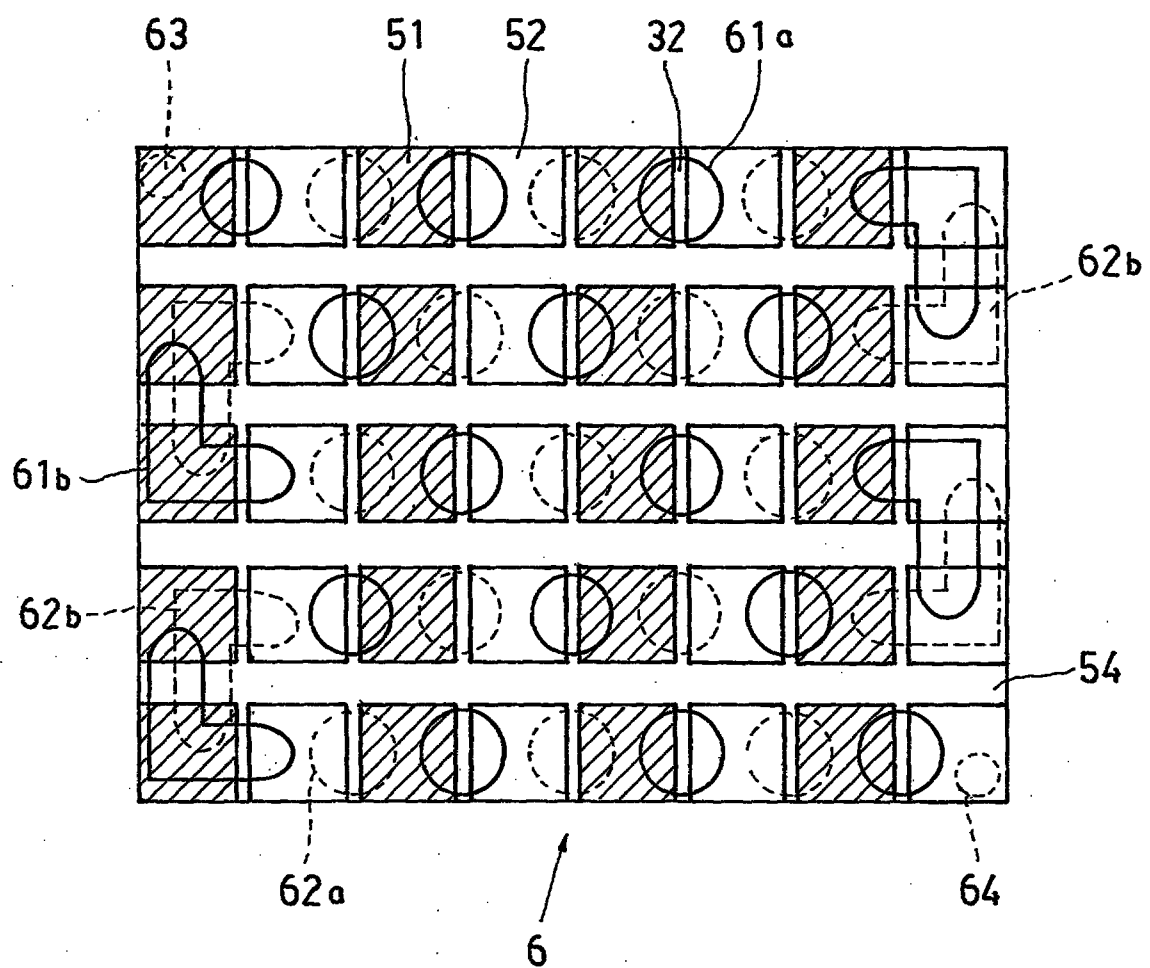


FIG. 10

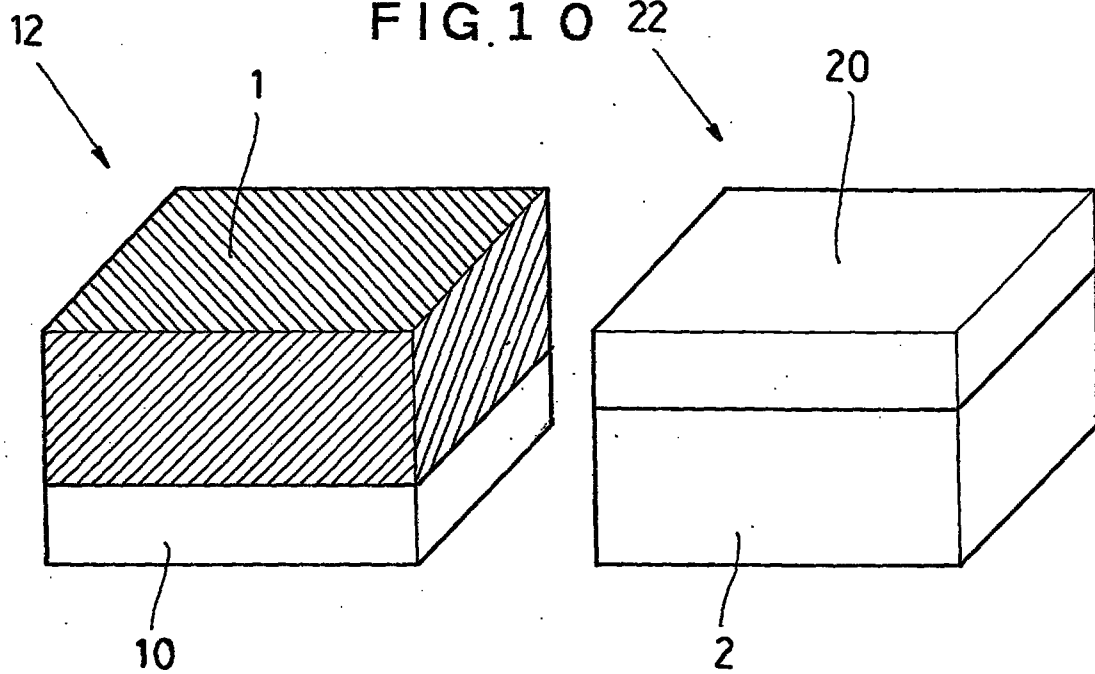


FIG. 11

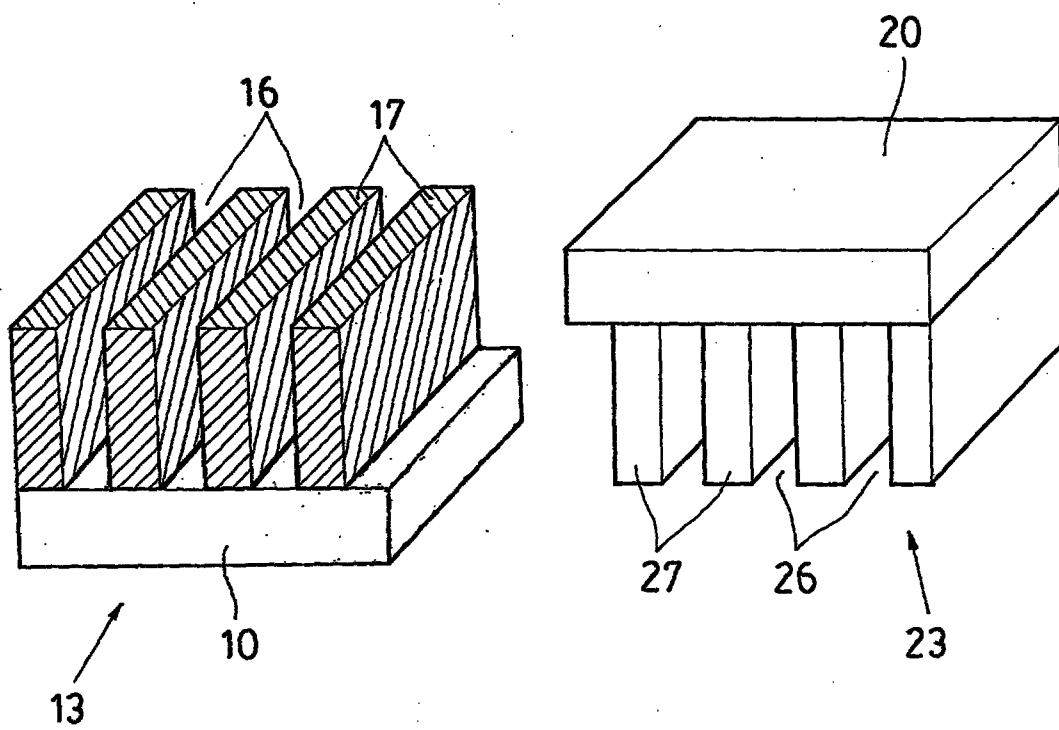


FIG. 1 2

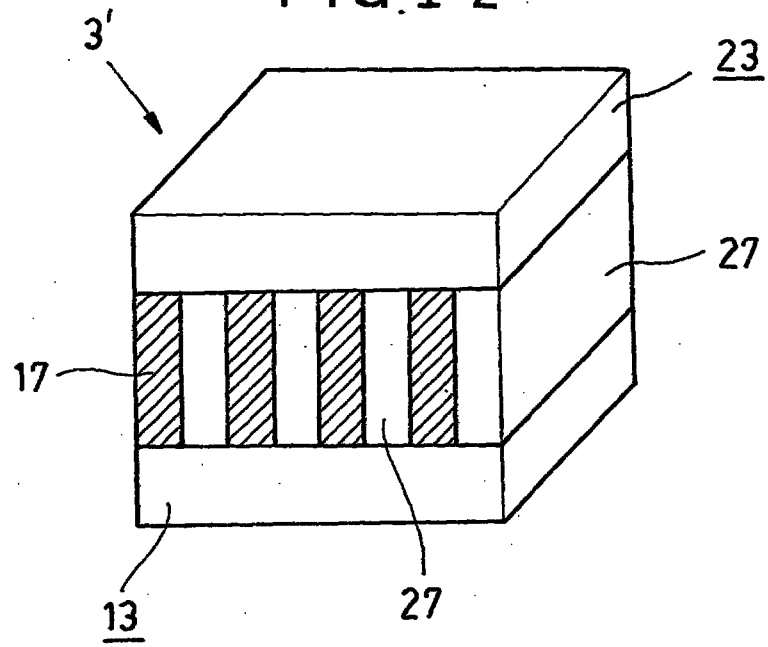


FIG. 1 3

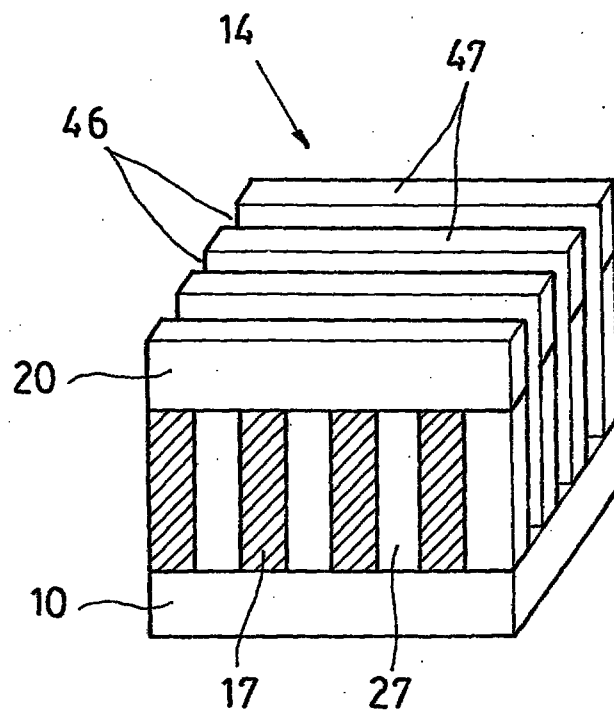


FIG. 14

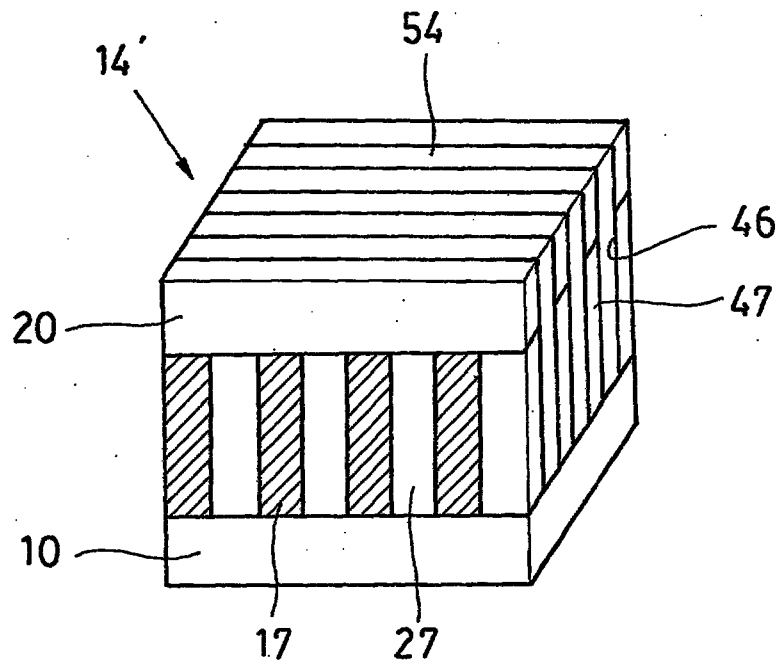
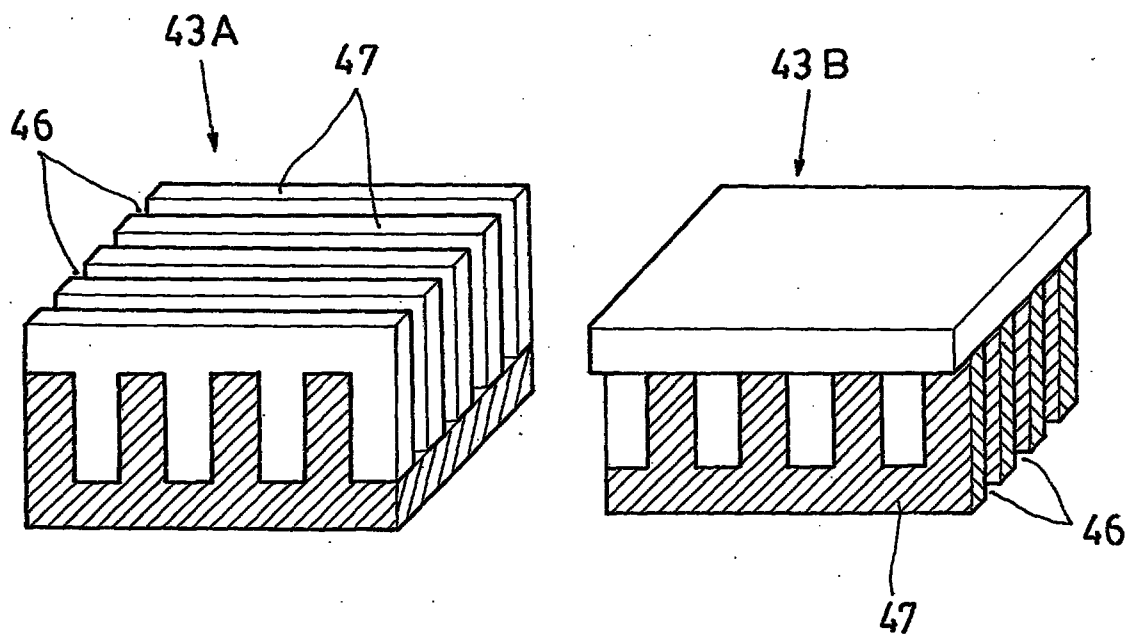


FIG. 15



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FIG. 16

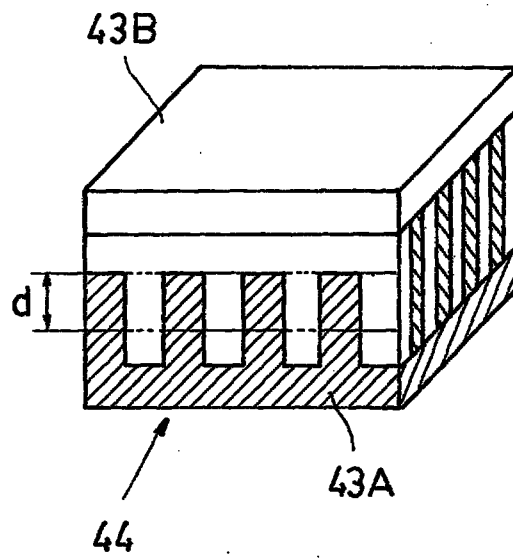


FIG. 17

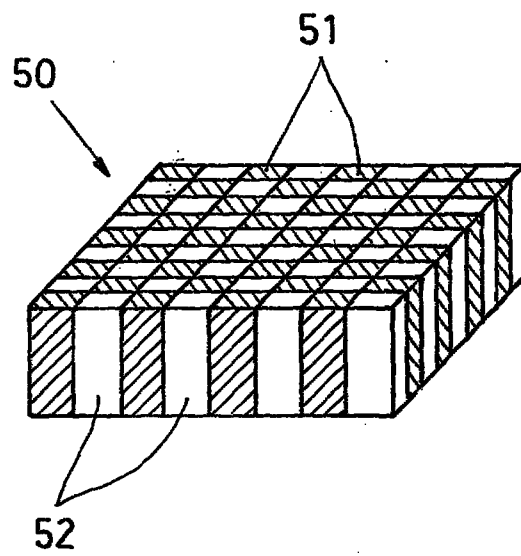


FIG. 18

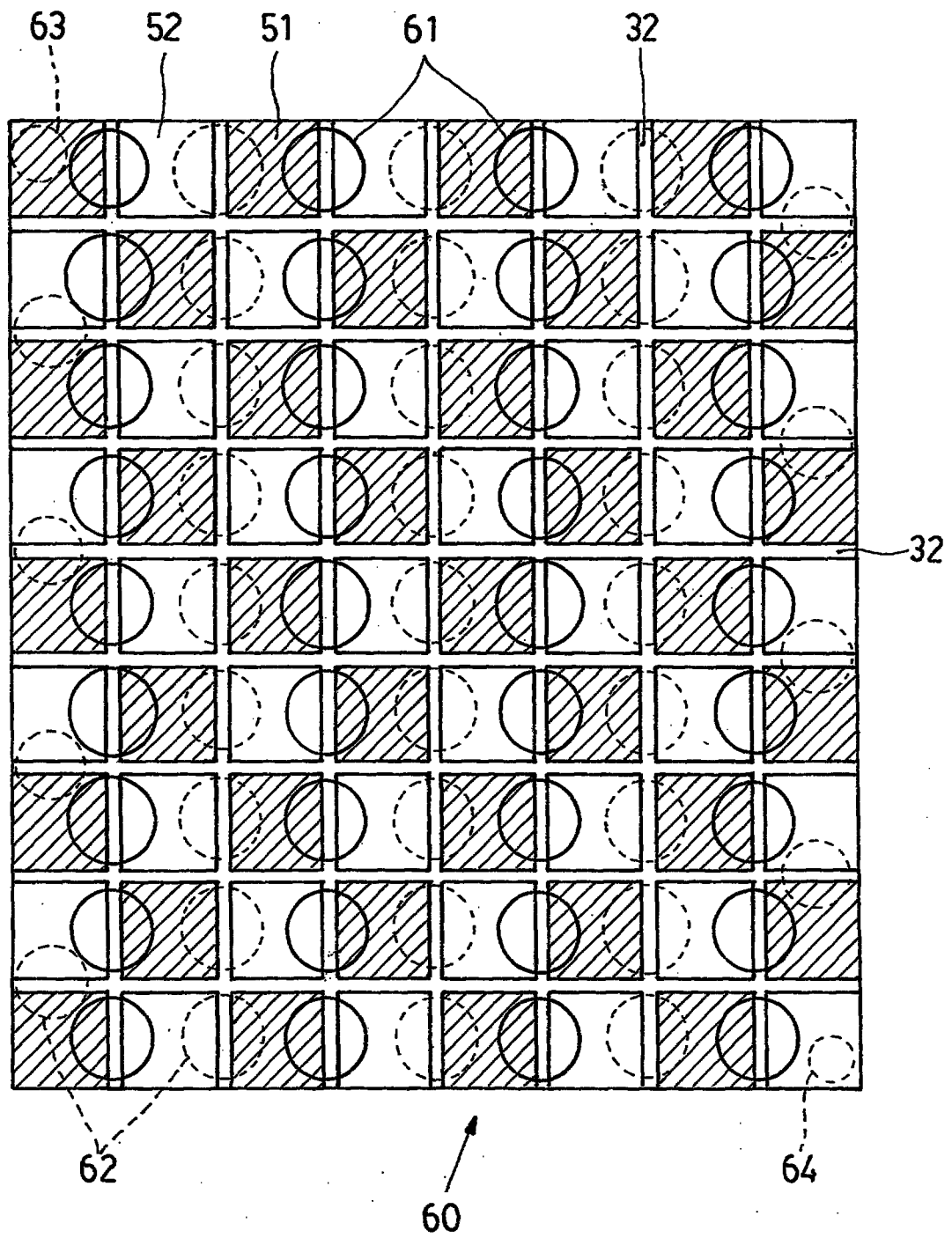


FIG. 19

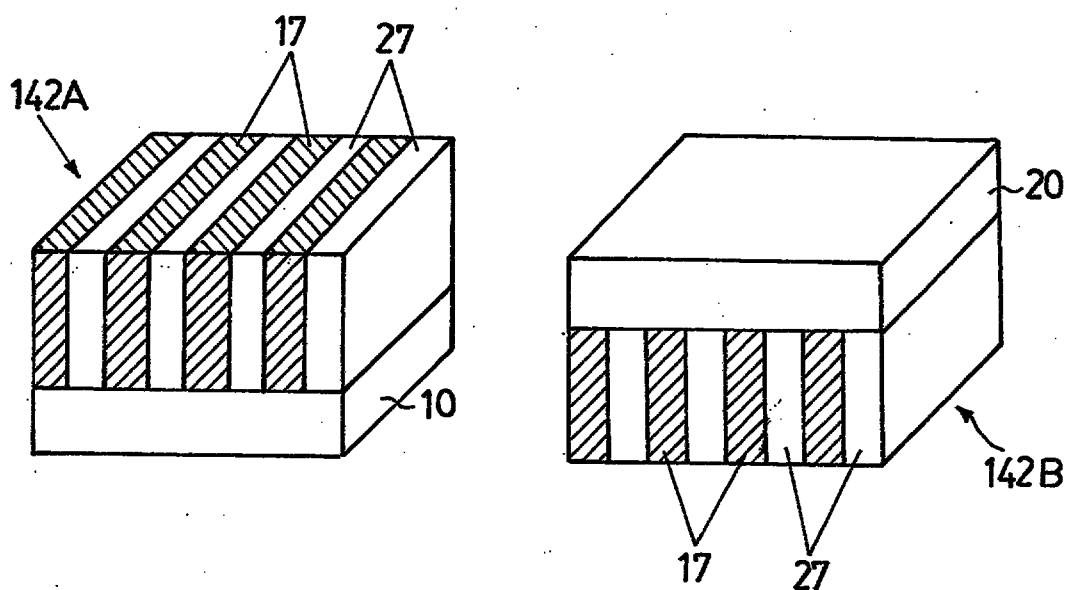


FIG. 20

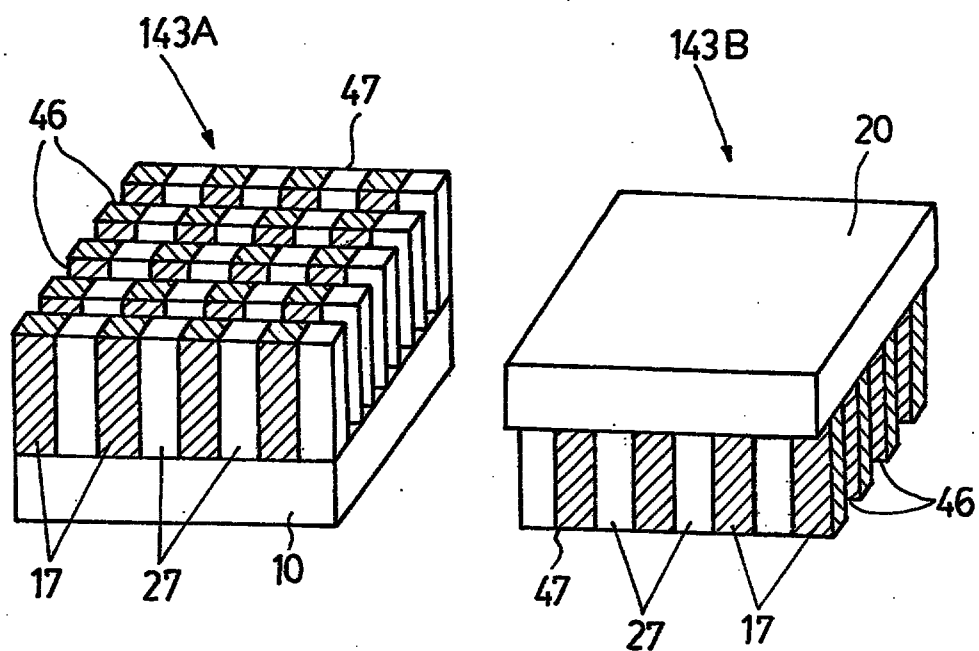


FIG. 2 1

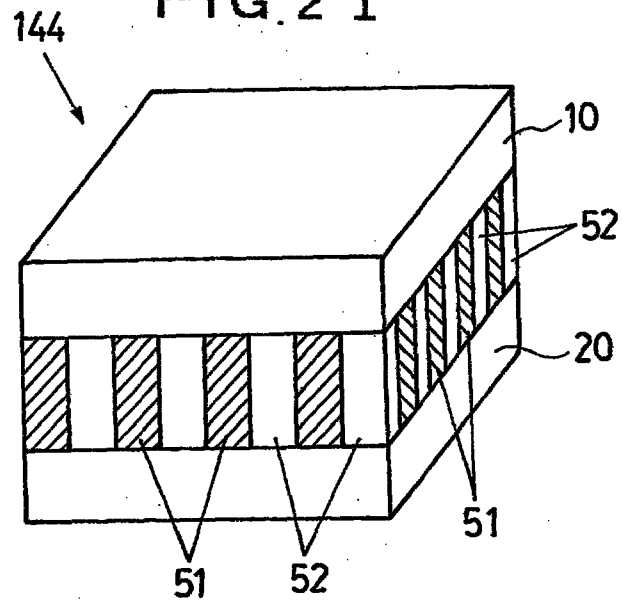


FIG. 2 2

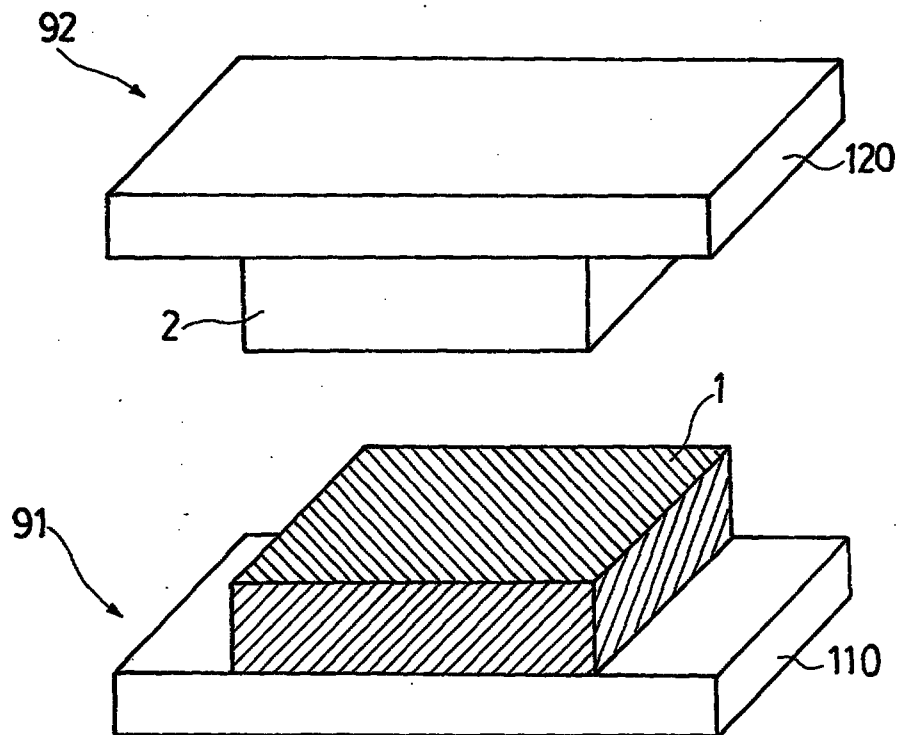


FIG. 2 3

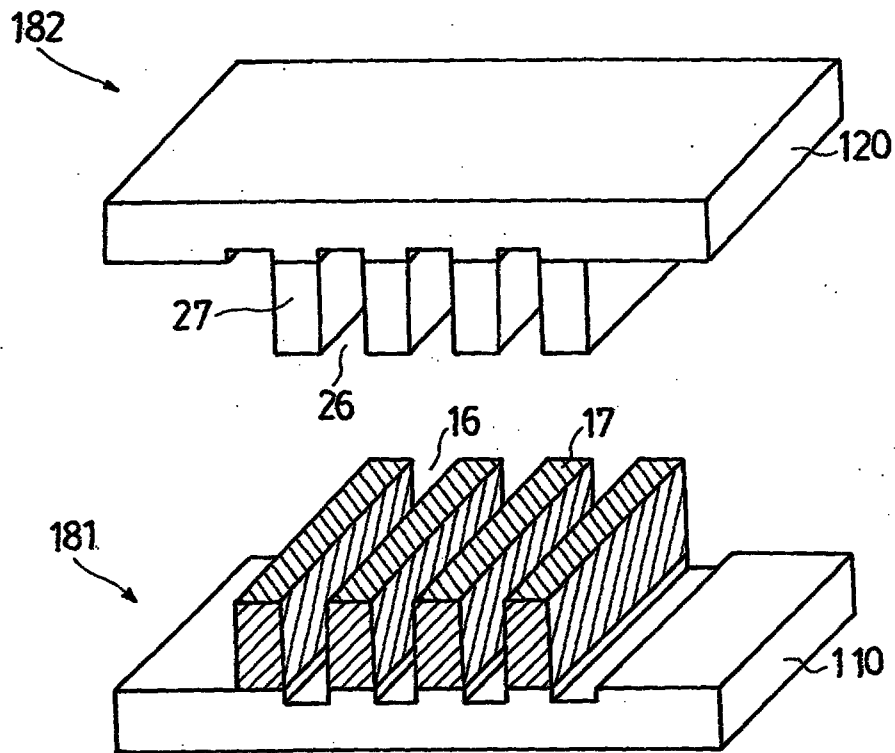


FIG. 2 4

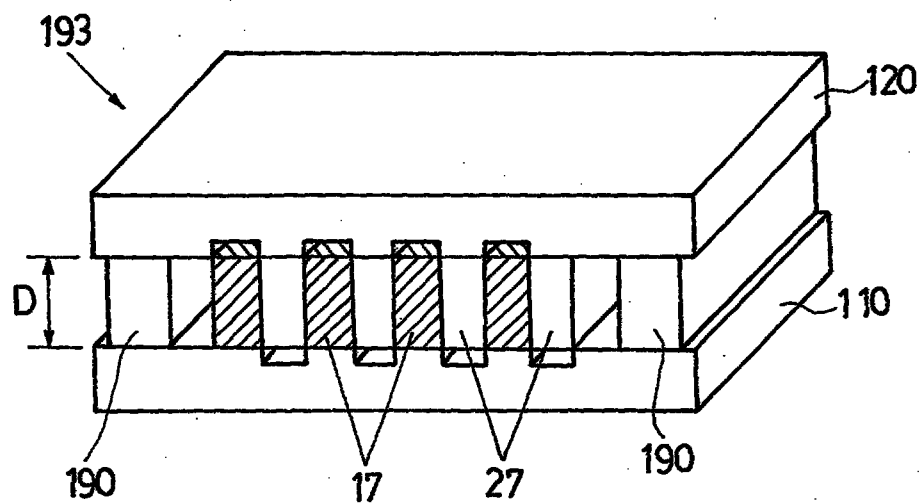


FIG. 2 5

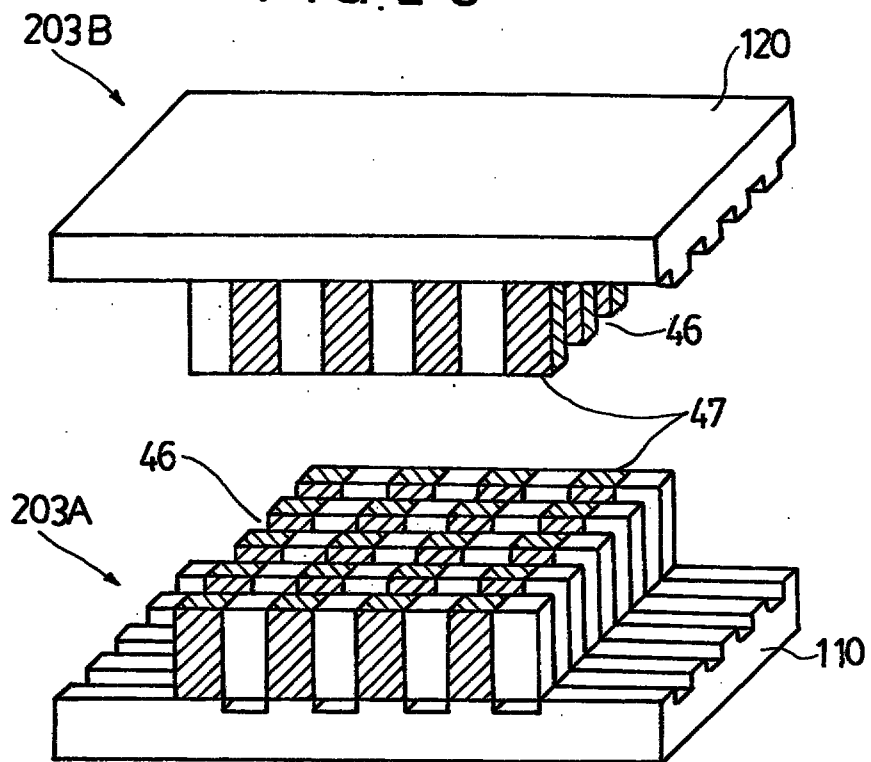


FIG. 2 6

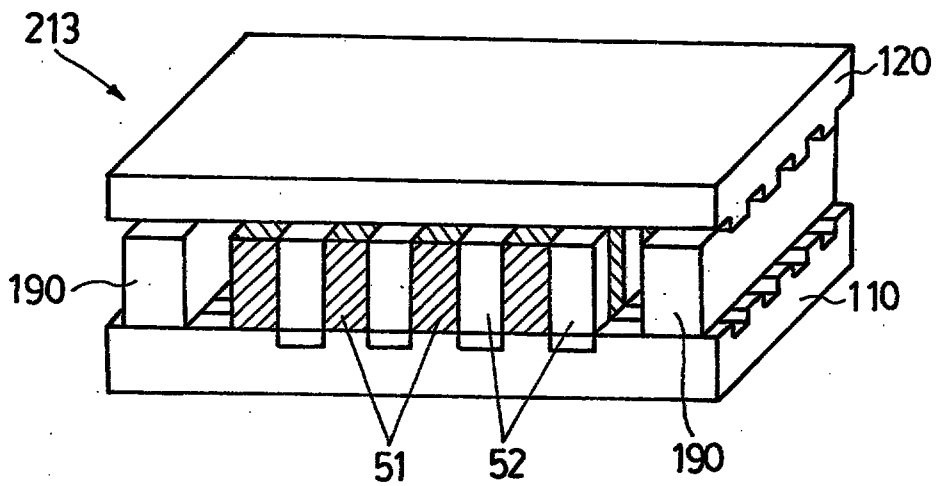


FIG. 2 7

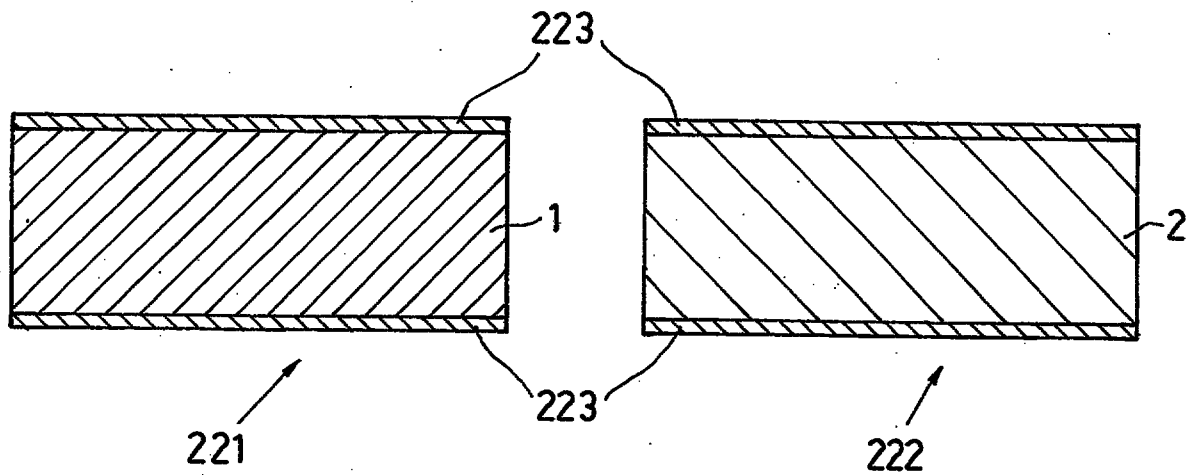


FIG. 2 8

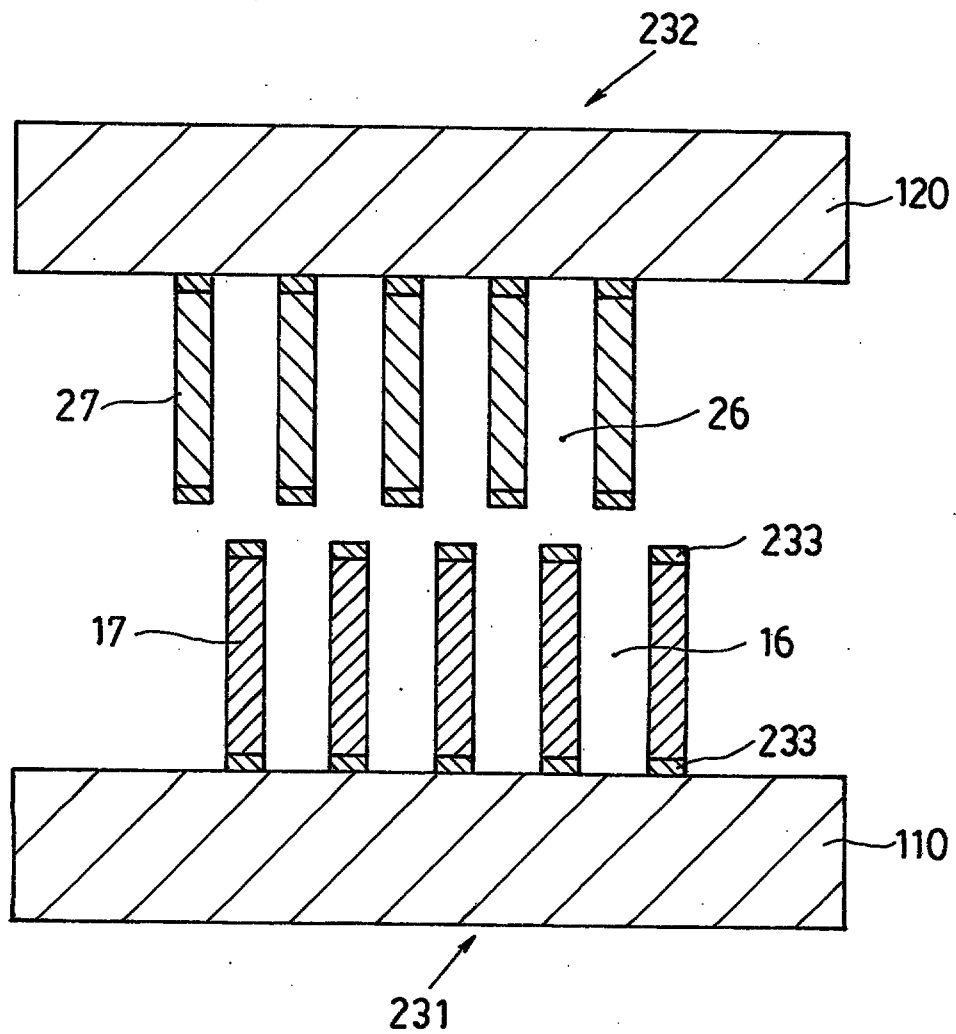


FIG. 29

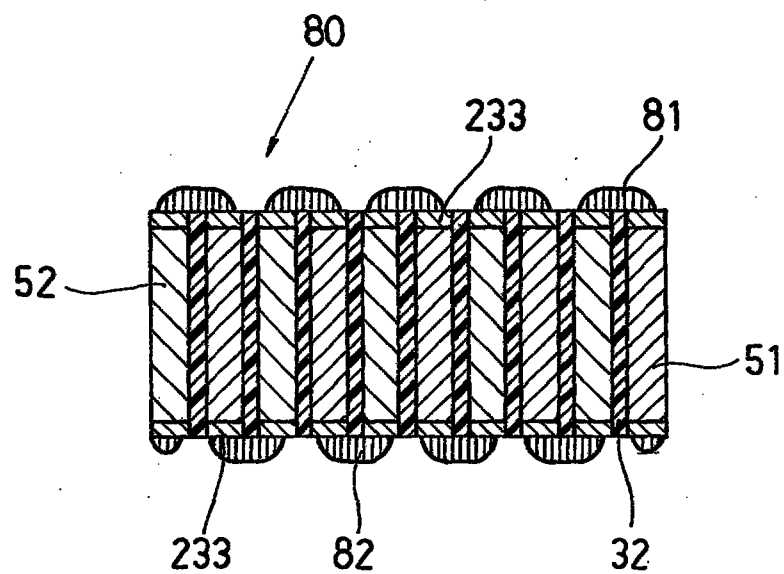


FIG. 30

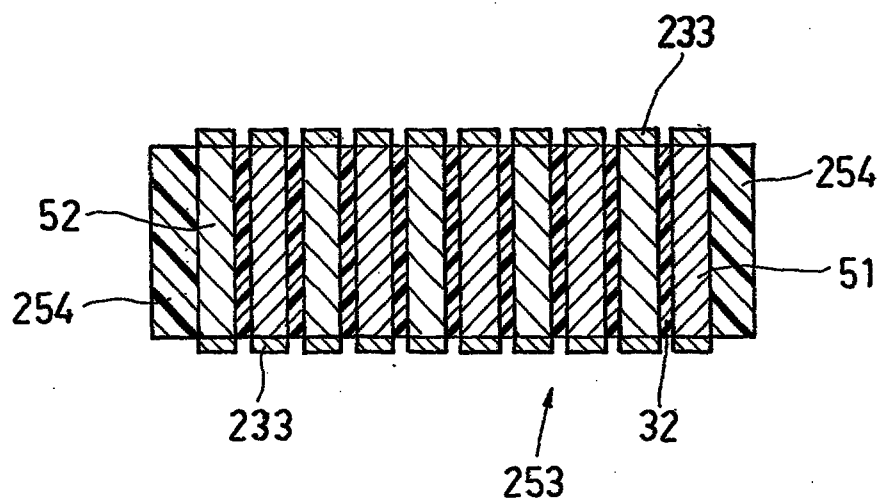


FIG. 3 1

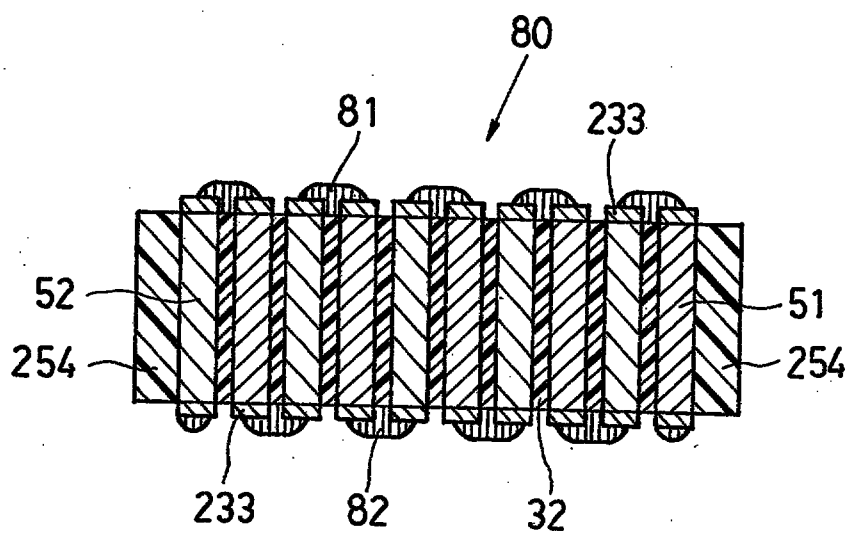


FIG. 3 2

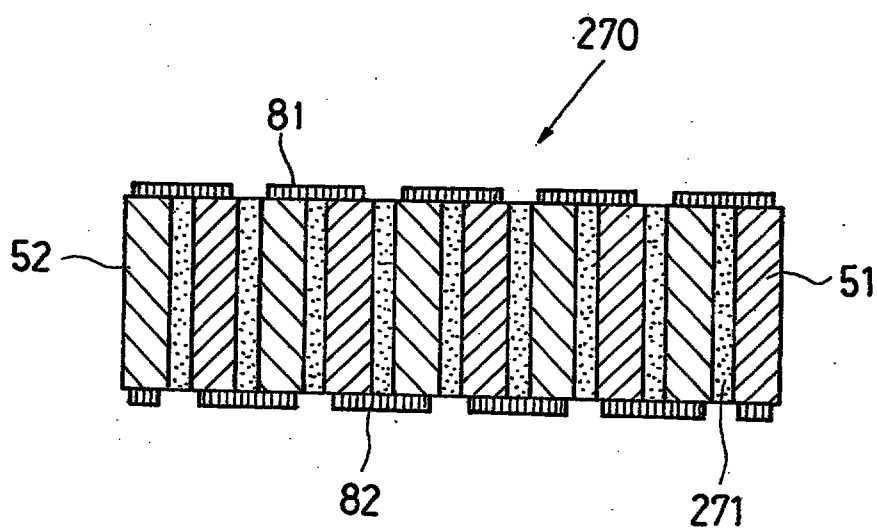


FIG. 3 3

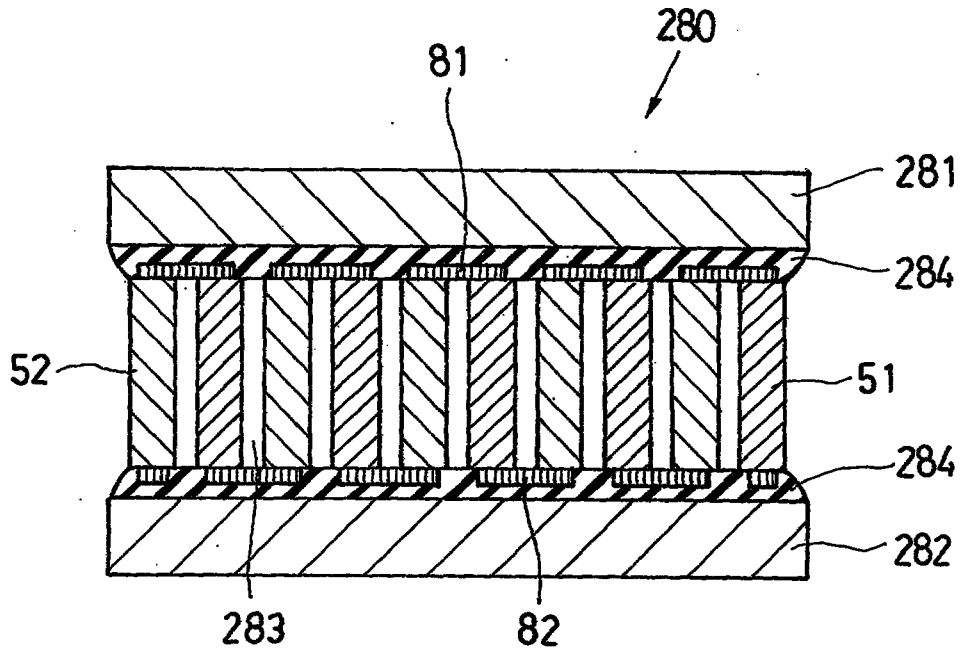
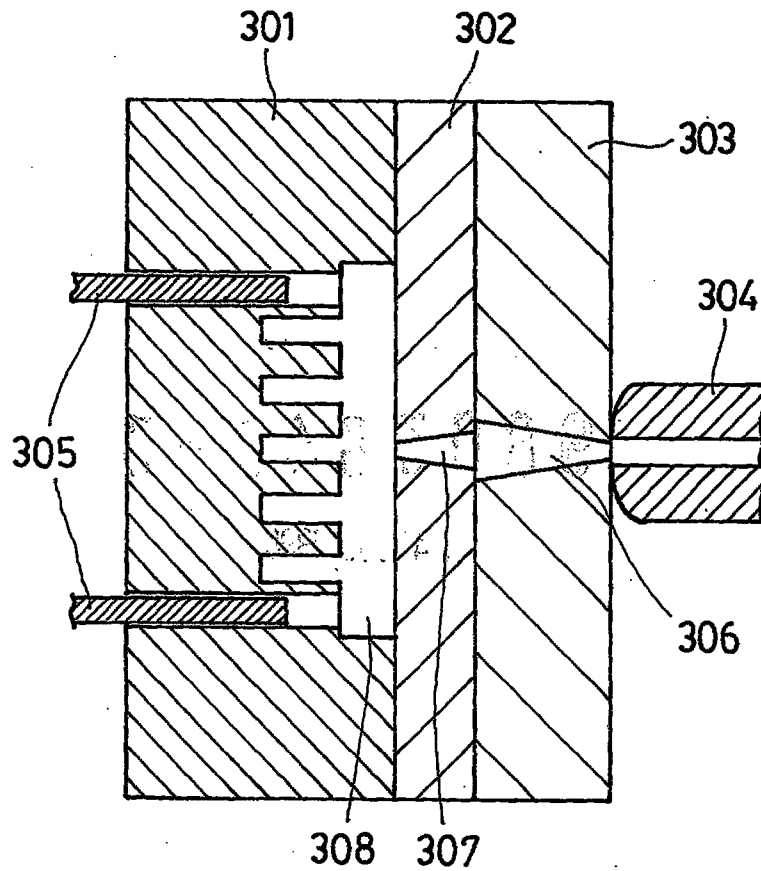
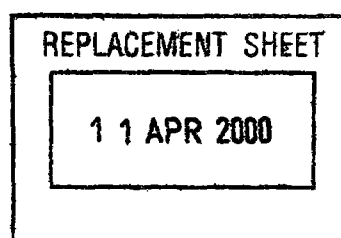


FIG. 3 4



ABSTRACT

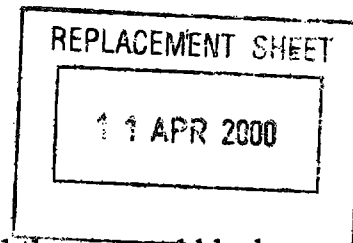
The invention provides a method of fabricating a thermoelectric device, whereby a grooved block (11) composed of n-type thermoelectric semiconductor and a grooved block (21) composed of p-type thermoelectric semiconductor, provided with a plurality of grooves (16, 26) formed therein, respectively, at a same pitch and parallel with each other, are formed such that a depthwise portion of respective grooved blocks is left intact, and then, an integrated block (3) is formed by fitting and adhering together the grooved blocks (11, 21) composed of the n-type and p-type thermoelectric semiconductors, respectively, filling up gaps in fitting parts with adhesive insulation members. After removing portions of the integrated block (3), other than the fitting parts where the n-type and p-type thermoelectric semiconductors are fitted to each other, n-type and p-type thermoelectric semiconductor pieces are exposed, and by forming electrodes for connecting the pieces to each other alternately and in series, the thermoelectric device is completed. Further, it is preferable to apply a process of exposing the thermoelectric semiconductor pieces and a process of forming the electrodes after applying a process of forming grooves to the integrated block (3) such that a plurality of grooves are formed in the direction crossing the direction in which the grooves (16, 26) have been formed, leaving a depthwise portion of the integrated block (3) intact, and insulation members filling up the grooves thus formed are solidified.



CLAIMS

1. A method of fabricating a thermoelectric device comprising:
 - a grooved block fabrication process of forming grooved blocks composed of an n-type thermoelectric semiconductor and p-type thermoelectric semiconductor, respectively, each provided with a plurality of grooves formed at a same pitch and parallel with each other, leaving a depthwise portion of respective grooved blocks intact;
 - a fitting process of fitting the grooved blocks composed of the n-type thermoelectric semiconductor and the grooved block composed of the p-type thermoelectric semiconductor formed, respectively, by said grooved block fabrication process to each other such that surfaces of the respective grooved blocks, with the grooves formed thereon, face each other;
 - an adhesion process of forming an integrated block by adhering the grooved block composed of the n-type thermoelectric semiconductor and the grooved block composed of the p-type thermoelectric semiconductor, fitted to each other by said fitting process, to each other after filling up gaps in fitting parts between the respective grooved blocks with an adhesive insulation member;
 - a second grooving process of forming a plurality of grooves in the integrated block formed by said adhesion process, in the direction crossing the direction of the grooves formed by said grooved block fabrication process, leaving a depthwise portion of the integrated block intact;
 - a solidification process of filling up the grooves formed by said second grooving process with an adhesive insulation member and solidifying the same; and
 - a thermoelectric semiconductor pieces exposure process of exposing n-type and p-type thermoelectric semiconductor pieces by removing all portions of the integrated block wherein the adhesive insulation member filling up the grooves is solidified in said solidification process, other than the fitting parts where the grooved block composed of





the n-type thermoelectric semiconductor and the grooved block composed of the p-type thermoelectric semiconductor are fitted to each other.

2. A method of fabricating a thermoelectric device comprising:

a grooved block fabrication process of forming two pairs of grooved blocks composed of an n-type thermoelectric semiconductor and p-type thermoelectric semiconductor, respectively, provided with a plurality of grooves formed at a same pitch and parallel with each other, respectively, leaving a depthwise portion of respective grooved blocks intact;

a first fitting process of fitting each pair of the grooved blocks composed of the n-type thermoelectric semiconductor and the grooved block of the p-type thermoelectric semiconductor, formed by said grooved block fabrication process, to each other such that surfaces with the grooves formed thereon face each other;

a first adhesion process of forming two integrated blocks by filling up gaps in fitting parts between each pair of the grooved blocks composed of the n-type thermoelectric semiconductor and the p-type thermoelectric semiconductor, respectively, fitted to each other by said first fitting process, with adhesive insulation members; and solidifying the same;

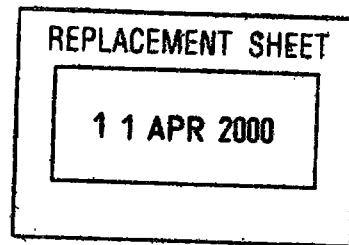
a grooving process of forming two grooved integrated blocks by forming in each of the two integrated blocks a plurality of grooves at a same pitch and in the direction crossing the direction of the grooves formed by said grooved block fabrication process, leaving a depthwise portion of respective integrated blocks intact;

a second fitting process of fitting the two grooved integrated blocks to each other such that surfaces with the grooves thus formed thereon face each other;

a second adhesion process of forming a second integrated block by filling gaps in fitting parts between the two grooved integrated blocks fitted to each other by said fitting process with adhesive insulation members, and solidifying the same; and

a thermoelectric semiconductor pieces exposure process of exposing n-type and p-type thermoelectric semiconductor pieces by

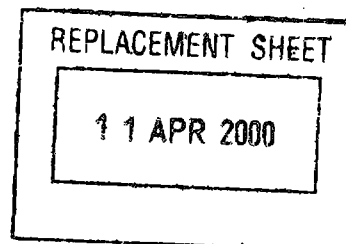




removing all depthwise portions of the second integrated block, other than the fitting parts.

3. A method of fabricating a thermoelectric device according to Claim 1 or 2, wherein the grooved block fabrication process is a process of forming the grooved block of the n-type thermoelectric semiconductor and grooved block of the p-type thermoelectric semiconductor by applying a grooving process to an n-type thermoelectric semiconductor block and p-type thermoelectric semiconductor block, respectively, such that a plurality of grooves are formed at a same pitch and parallel with each other, leaving a depthwise portion of said respective blocks intact.
4. A method of fabricating a thermoelectric device according to Claim 1 or 2, wherein the grooved block fabrication process is a process of forming the grooved block of the n-type thermoelectric semiconductor and grooved block of the p-type thermoelectric semiconductor by forming a molded n-type thermoelectric semiconductor material and molded p-type thermoelectric semiconductor material by use of a mold for the grooved block, respectively, and sintering the same.
5. A method of fabricating a thermoelectric device according to one of Claims 1 to 4, further comprising an electrode forming process of forming electrodes for connecting the n-type and p-type thermoelectric semiconductor pieces exposed with each other alternately and in series after the thermoelectric semiconductor pieces exposure process.
6. A method of fabricating a thermoelectric device comprising:
a first grooving process applied to an n-type thermoelectric semiconductor composite block prepared by bonding an n-type thermoelectric semiconductor block to a base and a p-type thermoelectric semiconductor composite block prepared by bonding a p-type thermoelectric semiconductor block to a base, for forming a plurality of grooves in the n-type thermoelectric semiconductor block and the p-type thermoelectric semiconductor block, respectively, at a same pitch, and to





a depth close to the interface between the respective thermoelectric semiconductor blocks and the base thereof;

a fitting process of fitting the n-type thermoelectric semiconductor composite block and p-type thermoelectric semiconductor composite block, with the grooves formed by said first grooving process, respectively, to each other such that respective grooved surfaces face each other;

an adhesion process of forming an integrated block by filling gaps in fitting parts between the n-type thermoelectric semiconductor composite block and p-type thermoelectric semiconductor composite block, fitted to each other by said fitting process, with adhesive insulation members so as to adhere the n-type thermoelectric semiconductor composite block and p-type thermoelectric semiconductor composite block to each other;

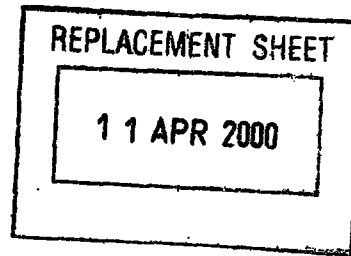
a second grooving process of forming a plurality of grooves in the direction crossing the direction of the grooves formed by said first grooving process, and to a depth close to the interface between the respective thermoelectric semiconductor blocks and the base thereof in the integrated block formed by said adhesion process;

a solidification process of filling up the grooves formed by said second grooving process with insulation members, and solidifying the same; and

a thermoelectric semiconductor pieces exposure process of exposing n-type and p-type thermoelectric semiconductor pieces by removing the respective bases of the integrated blocks wherein the grooves are filled with the insulation member and the insulation member is then solidified in said solidification process.

7. A method of fabricating a thermoelectric device according to Claim 6, characterized in that the bases of the n-type thermoelectric semiconductor composite block and the p-type thermoelectric semiconductor composite block, respectively, have a surface area larger than an area of a bonded portion of the surface of the respective thermoelectric semiconductor blocks, and in the fitting process, spacers are interposed between portions of the bases of the n-type thermoelectric





semiconductor composite block and the p-type thermoelectric semiconductor composite block, respectively, where the respective thermoelectric semiconductor blocks do not exist, so that a spacing between the bases is controlled to be substantially equivalent to the thicknesses of the respective thermoelectric semiconductor blocks.

8. A method of fabricating a thermoelectric device comprising:

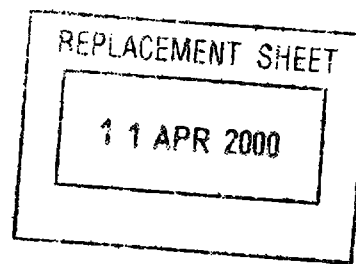
a first grooving process applied to two n-type thermoelectric semiconductor composite blocks prepared by bonding an n-type thermoelectric semiconductor block to a base, respectively, and two p-type thermoelectric semiconductor composite blocks prepared by bonding a p-type thermoelectric semiconductor block to a base, respectively, for forming a plurality of grooves at a same pitch, and to a depth close to the interface between the respective thermoelectric semiconductor blocks and the base thereof, in the n-type thermoelectric semiconductor block and the p-type thermoelectric semiconductor block, respectively;

a first fitting process of fitting the two pairs of the n-type thermoelectric semiconductor composite block and p-type thermoelectric semiconductor composite block, with the grooves formed therein, respectively, by said first grooving process to each other, respectively, such that respective grooved surfaces face each other;

a first adhesion process of forming two integrated blocks by adhering the two pairs of the n-type thermoelectric semiconductor composite blocks and p-type thermoelectric semiconductor composite blocks to each other, respectively, by filling gaps in fitting parts between the respective n-type thermoelectric semiconductor composite blocks and p-type thermoelectric semiconductor composite blocks, fitted to each other by said first fitting process, with adhesive insulation members;

a second grooving process of forming two grooved integrated blocks by forming a plurality of grooves at a same pitch in the two integrated blocks formed, respectively, by said first adhesion process, in the direction crossing the direction of the grooves formed by said first grooving process, and to a depth close to an interface between the respective thermoelectric semiconductor blocks and the base thereof;





a second fitting process of fitting the two grooved integrated blocks to each other such that respective grooved surfaces face each other;

a second adhesion process of forming a second integrated block by adhering the two grooved integrated blocks, fitted to each other by said second fitting process, to each other by filling gaps in fitting parts between the two grooved integrated blocks with adhesive insulation members; and

a thermoelectric semiconductor pieces exposure process of exposing n-type and p-type thermoelectric semiconductor pieces by removing the respective bases of the second integrated block.

9. A method of fabricating a thermoelectric device according to Claim 8, characterized in that bases having a surface area larger than an area of a bonded portion of the surface of the respective thermoelectric semiconductor blocks are used for the base of the n-type thermoelectric semiconductor composite block and the p-type thermoelectric semiconductor composite block, respectively, and spacers are interposed between portions of the respective bases of the n-type thermoelectric semiconductor composite block and the p-type thermoelectric semiconductor composite block to be fitted to each other, where the respective thermoelectric semiconductor blocks do not exist, controlling a spacing between the bases to be substantially equivalent to thicknesses of the respective thermoelectric semiconductor blocks in the first fitting process, spacers being further interposed between portions of the respective bases of the two integrated grooved blocks to be fitted to each other, where the respective thermoelectric semiconductor blocks do not exist, controlling a spacing between the bases to be substantially equivalent to the thickness of the respective thermoelectric semiconductor blocks in the second fitting process.
10. A method of fabricating a thermoelectric device according to one of Claims 6 to 9, further comprising an electrode forming process of forming electrodes for connecting the exposed n-type and p-type thermoelectric

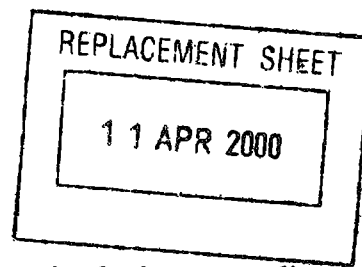


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semiconductor pieces to each other alternately and in series, applied after the thermoelectric semiconductor pieces exposure process.

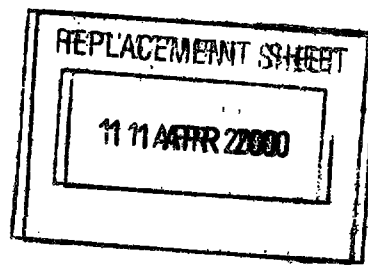
11. A method of fabricating a thermoelectric device according to Claim 1 or 6, characterized in that an insulation film is formed on at least one of plural fitting surfaces of a pair of thermoelectric semiconductor blocks to be fitted to each other in the fitting process.
12. A method of fabricating a thermoelectric device according to Claim 1 or 6, characterized in that the insulation member for filling up the gaps in the fitting parts in the adhesion process is an adhesive insulation member with insulating spacers dispersed therein.
13. A method of fabricating a thermoelectric device according to Claim 2 or 8, characterized in that an insulation film is formed on at least one of plural fitting surfaces of a pair of thermoelectric semiconductor blocks to be fitted to each other in at least either of the first fitting process or the second fitting process.
14. A method of fabricating a thermoelectric device according to Claim 2 or 8, characterized in that the insulation member for filling up the gaps in the fitting parts in at least either of the first adhesion process or the second adhesion process is an adhesive insulation member with insulating spacers dispersed therein.
15. A method of fabricating a thermoelectric device according to one of Claims 6 to 9, characterized in that before the n-type thermoelectric semiconductor block and the p-type thermoelectric semiconductor block are bonded to the bases, respectively, a metal coated layer is formed on the surface of the respective thermoelectric semiconductor blocks, bonded to the respective bases, and on the surface thereof on the opposite side.





16. A method of fabricating a thermoelectric device according to Claim 15, further comprising an electrode formation process of forming electrodes for connecting the exposed n-type and p-type thermoelectric semiconductor pieces to each other alternately and in series by use of an electrically conductive paste applied on the metal coated layer after the thermoelectric semiconductor pieces exposure process.
17. A method of fabricating a thermoelectric device according to one of Claims 1, 2, 6, or 8, further comprising a metal layer formation process of forming metal layers on respective surfaces of the exposed n-type and p-type thermoelectric semiconductor pieces, where the electrodes are formed, and an electrode formation process of forming the electrodes for connecting the exposed n-type and p-type thermoelectric semiconductor pieces to each other alternately and in series over the metal layers, said processes being applied after the thermoelectric semiconductor pieces exposure process.
18. A method of fabricating a thermoelectric device according to Claim 17, characterized in that the electrodes are formed by use of an electrically conductive paste in the electrode formation process.
19. A method of fabricating a thermoelectric device comprising
- a grooved block fabrication process of forming grooved blocks composed of an n-type thermoelectric semiconductor and p-type thermoelectric semiconductor, respectively, each provided with a plurality of grooves formed at a same pitch and parallel with each other, leaving a depthwise portion of respective grooved blocks intact;
 - a fitting process of fitting the grooved blocks composed of the n-type thermoelectric semiconductor and p-type thermoelectric semiconductor formed, respectively, by said grooved block fabrication process to each other such that surfaces of the respective grooved blocks, with the grooves formed thereon, face each other;
 - an adhesion process of forming an integrated block by adhering the grooved block composed of the n-type thermoelectric semiconductor





and the grooved block composed of the p-type thermoelectric semiconductor, fitted to each other by said fitting process, to each other after filling up gaps in fitting parts between the respective grooved blocks with an adhesive insulation member; and

a thermoelectric semiconductor pieces exposure process of exposing n-type and p-type thermoelectric semiconductor pieces by removing all portions of the integrated block formed by said adhesion process, other than the fitting parts where the grooved block composed of the n-type thermoelectric semiconductor and the grooved block composed of the p-type thermoelectric semiconductor are fitted to each other,

wherein provisional fixture layers as insulation members for filling up the gaps in the fitting parts are formed using a material removable by heating or by use of a solvent in the adhesion process;

said method further comprising an electrode formation process of forming electrodes for connecting the exposed n-type and p-type thermoelectric semiconductor pieces to each other alternately and in series after the thermoelectric semiconductor pieces exposure process, fabricating a provisional thermoelectric device, and thereafter performing a process of fixedly attaching a heat radiation plate to one of the surfaces of the provisional thermoelectric device, where the electrodes are formed, and a heat absorption plate to the other via an insulating fixture layers, respectively, and a process of removing the provisional fixture layers either by heating or by use of a solvent after said preceding process.

20. A method of fabricating a thermoelectric device according to Claim 1 or 6, characterized in that provisional fixture layers are formed using a material removable by heating or by use of a solvent as at least either of the insulation members for filling up the gaps in the fitting parts in the adhesion process or the insulation members for filling up the grooves in the solidification process;

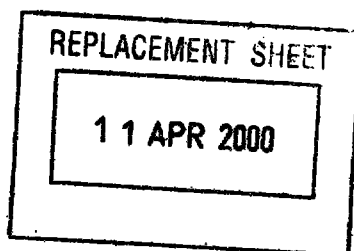
said method further comprising an electrode formation process of forming electrodes for connecting the exposed n-type and p-type thermoelectric semiconductor pieces to each other alternately and in series after the thermoelectric semiconductor pieces exposure process,



fabricating a provisional thermoelectric device, and thereafter performing a process of fixedly attaching a heat radiation plate to one of the surfaces of the provisional thermoelectric device, where the electrodes are formed, and a heat absorption plate to the other via an insulating fixture layers, respectively, and a process of removing the provisional fixture layers either by heating or by use of a solvent after said preceding process.

21. A method of fabricating a thermoelectric device according to Claim 2 or 8, characterized in that provisional fixture layers as insulation members for filling up the gaps in the fitting parts are formed using a material removable by heating or by use of a solvent in the first adhesion process or the second adhesion process;

said method further comprising an electrode formation process of forming electrodes for connecting the exposed n-type and p-type thermoelectric semiconductor pieces to each other alternately and in series after the thermoelectric semiconductor pieces exposure process, fabricating a provisional thermoelectric device, and thereafter performing a process of fixedly attaching a heat radiation plate to one of the surfaces of the provisional thermoelectric device, where the electrodes are formed, and a heat absorption plate to the other via an insulating fixture layers, respectively, and a process of removing the provisional fixture layers either by heating or by use of a solvent after said preceding process.



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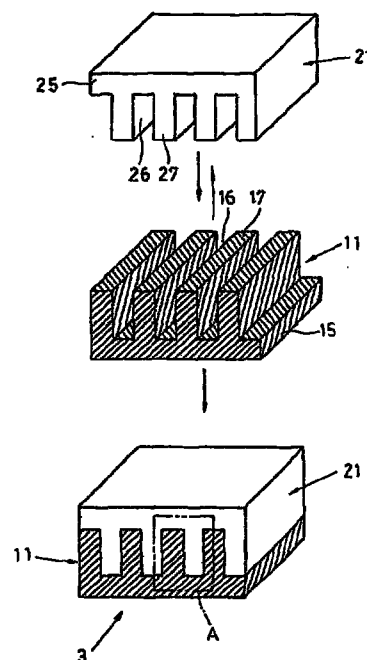
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(21) 国際出願番号 PCT/JP97/04115 (22) 国際出願日 1997年11月12日(12.11.97) (30) 優先権データ 特願平8/304846 1996年11月15日(15.11.96) JP (71) 出願人 (米国を除くすべての指定国について) シチズン時計株式会社(CITIZEN WATCH CO., LTD.)(JP/JP) 〒163-04 東京都新宿区西新宿2丁目1番1号 Tokyo, (JP) (72) 発明者 ; および (75) 発明者 / 出願人 (米国についてのみ) 平石久人(HIRAISHI, Hisato)(JP/JP) 渡辺 滋(WATANABE, Shigeru)(JP/JP) 〒359 埼玉県所沢市大字下富野840番地 シチズン時計株式会社 技術研究所内 Saitama, (JP) (74) 代理人 弁理士 大澤 敬, 外(OSAWA, Takashi et al.) 〒170 東京都豊島区東池袋1丁目20番2号 池袋ホワイトハウスビル818号 Tokyo, (JP)		(81) 指定国 AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, HU, IL, IS, JP, KE, KG, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO特許 (GH, KE, LS, MW, SD, SZ, UG, ZW), ユーラシア特許 (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), 欧州特許 (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI特許 (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG). 添付公開書類 国際調査報告書
(54)Title: METHOD OF MANUFACTURING THERMIONIC ELEMENT (54)発明の名称 熱電素子の製造方法 (57) Abstract A method of manufacturing a thermionic element, comprising preparing a grooved block (11) of an n-type thermoelectric semiconductor and a grooved block (21) of a p-type thermoelectric semiconductor, on each of which a plurality of grooves (16, 26) are formed at the same pitch with portions in a thicknesswise direction ungrooved, fitting the grooved block (11, 21) of the n-type thermoelectric semiconductor and of the p-type thermoelectric semiconductor to each other, and filling an adhesive insulating material in gaps between the fitted portions to form an integral block (3). The method further comprises removing portions except fitted portions in the integral block (3), where the n-type and p-type thermoelectric semiconductors are fitted to each other, to expose n-type and p-type thermoelectric semiconductors stock pieces, and forming electrodes for connecting the respective thermoelectric semiconductors stock pieces alternately in series. Further, it is desirable to form a plurality of grooves in a direction intersecting the direction of the grooves (16, 26), with portions of the stock pieces left, and perform the above steps of exposing the thermoelectric semiconductors stock pieces and forming the electrodes after filling an insulating material in the formed grooves and having the same solidifying.		



(57) 要約

この発明は、それぞれ厚さ方向の一部を残して同一ピッチで複数本の溝(16, 26)が平行に形成されたn型の熱電半導体の溝入りブロック(11)およびp型の熱電半導体の溝入りブロック(21)を作製し、そのn型とp型の熱電半導体の溝入りブロック(11, 21)を互いに嵌合させ、その嵌合部の空隙に接着性のある絶縁部材を充填して固着し、一体化ブロック(3)を形成する。その一体化ブロック(3)におけるn型とp型の熱電半導体が互いに嵌合している嵌合部以外の部分を除去して、n型およびp型の熱電半導体素片を露出させ、その各熱電半導体素片を交互に直列に接続する電極を形成して、熱電素子を製造する方法である。さらに、上記一体化ブロック(3)に、上記溝(16, 26)の方向と交差する方向に複数本の溝加工を厚さ方向の一部を残して施し、その溝加工部に絶縁部材を充填して固化させた後、上記熱電半導体素片を露出させる工程と電極を形成する工程を行なうようにするのが望ましい。

PCTに基づいて公開される国際出願のパンフレット第一頁に掲載されたPCT加盟国を同定するために使用されるコード(参考情報)

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ES	スペイン						