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VARIABLE FREQUENCY OSCILLATOR

This invention relates to variable frequency oscillators.

According to the present invention there is provided a variable frequency oscillator comprising: a first phase-locked loop including a first voltage controlled oscillator; a second phase-locked loop including a second voltage controlled oscillator having the same constants as the first voltage controlled oscillator; an oscillator means for generating a stable pulse train, the arrangement being such that, in operation, the first phase-locked loop is synchronised with a sequence of input data, the second phase-locked loop is synchronised with the pulse trains from the oscillator means, and the first voltage controlled oscillator in the first phase-locked loop is stabilised by a control voltage applied to the second voltage controlled oscillator in the second phase-locked loop; and a digital circuit for counting pulses generated at regular intervals and delaying the pulses by a predetermined period of time to delay the sequence of the input data before application to the first phase-locked loop.

The variable frequency oscillator may include a ring oscillator for controlling the frequency of oscillation of each voltage controlled oscillator by controlling the current flowing into the ring oscillator.

The variable frequency oscillator preferably comprises shifting means for shifting the phase of each output pulse from the first voltage controlled oscillator in the first phase-locked

loop by 90° , a flip-flop circuit arranged to be set by the input data and reset by the output from the shifting means, and a circuit arranged to be triggered on the trailing edge of the output from the flip-flop circuit for delivering a pulse having a predetermined pulse width.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a block diagram of one embodiment of a variable frequency oscillator according to the present invention;

10 Figure 2(a) is a block diagram of a counter circuit of the variable frequency oscillator of Figure 1;

Figure 2(b) is a circuit diagram of part of the variable frequency oscillator of Figure 1;

15 Figures 3(a) and 3(b) illustrate recording formats of a floppy disk;

Figure 4 is a block diagram of a conventional variable frequency oscillator;

Figure 5 is a timing chart for illustrating and comparing the operations of the conventional variable frequency oscillator of Figure 4 and the variable frequency oscillator of Figure 1; and

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Figure 6 is a detailed circuit diagram of the conventional variable frequency oscillator of Figure 4.

Before describing a conventional variable frequency oscillator (VFO) for floppy disks, formats for data writing for floppy disks and the functions for such a VFO will be described. Presently, IBM
5 format and similar formats are nearly exclusively used as formats for floppy disks and so these formats are described below.

Referring to Figures 3(a) and 3(b), there are shown a data pulse train read from a floppy disk 20 cm (8 inch) in diameter by means of a floppy disk drive (FDD). Figure 3(a) shows a single density (FM) recording on the disk. In this case, one clock pulse is admitted every 4 μ s of 1 bit cell of the fetched data pulse train. A VFO produces data window waveforms as shown from the data pulse train, and then the window waveforms are ANDed with the data pulse train to produce separate data pulses. Figure 3(b) shows a double density (MFM) recording, in which only when neighbouring bits are 0's is a clock pulse admitted. In this case, a VFO produces data window waveforms from the fetched data pulse train, and then the window waveforms are ANDed with the data pulse train for reproduction of data. When a floppy disk 12.7 cm (5 inch) in diameter, called a mini-floppy disk, is used the period of bit cells is twice that of a 20 cm (8 inch) floppy disk.

When the pulses of a data pulse train read from the floppy disk drive are located precisely in standard positions within bit cells as shown in Figures 3(a) and 3(b), data window waveforms can be produced by, for example, a one-shot multivibrator with relative ease. In reality, however, there arises a possibility that each pulse is shifted from its standard position by about ± 350 ns with a 20 cm (8 inch) standard floppy disk and ± 700 ns with a mini-floppy disk at worst. This phenomenon is known as peak shift and is caused by interference between neighbouring waveforms when data is read. A VFO acts to produce correct data window waveforms from a fetched

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data pulse train accompanied by such peak shift and to derive only data pulses.

An example of a conventional VFO is described in detail in "Interface", July, 1979. Figure 4 shows this conventional VFO in block diagram form, in which data read from a floppy disk drive is applied to a terminal 401 and admitted to a phase comparator 404 through a one-shot multivibrator 403. A voltage-controlled oscillator (VCO) 408 produces window waveforms which are supplied to the phase comparator 404 through a gate circuit 410 for phase comparison with the output from the multivibrator 403. The output from the comparator 404 is fed to a first low-pass filter 406 or a second low-pass filter 407 via a switching circuit 405 to remove the high frequency components, and then the signal is fed to the VCO 408, so that the frequency of oscillation of the VCO 408, that is, the frequency and phase of the window signal, is controlled by the phase difference between those signals. In particular, the phase comparator 404, the filter 406 or 407 and the VCO 408 form a phase-locked loop, and the circuit does not respond to rapid changes in data signals due to peak shift, the data signals being fetched for application to the terminal 411. Rather, it responds to slow changes and produces a signal which is synchronised with the input signal and the phase of which is always in step with that of the input signal. The system includes both the first low-pass filter 406 responding quickly to its input signal or having a high cut-off frequency and the second low-pass filter 407 responding slowing

to its input signal or having a low cut-off frequency. The two filters are alternatively used by the operation of the switching circuit 405 for the reason described hereinafter.

Any floppy disk has evenly spaced pulses, called sync fields,
5 written in the head portions of sectors for synchronisation. Therefore, no peak shift takes place in these fields. Thus, the first filter 406 responding quickly is used for the fields and a synchronisation with sync bits is effected rapidly. Thereafter, when fields of recorded data are to be treated, the filter 406 is
10 changed over to the filter 407, which responds slowly to its input signal, so that the system will not respond to changes in the interval of pulses attributed to peak shift. The signal for the changeover operation can be supplied from a processor or a floppy disk controller of the system using the floppy disk drive and is
15 applied to a terminal 402. Next, the operation of the one-shot multivibrator 403, a gate circuit 410 and an output waveform shaping circuit 409 having an output terminal 412 are described by referring to the time chart of Figure 5.

The multivibrator 403 is triggered into action on each rising
20 portion of data pulses (waveform (a) of Figure 5) read from the floppy disk drive and delivers pulses having a pulse width that is one-fourth the duration of one bit cell (waveform (b) of Figure 5). These pulses are applied to the phase comparator 404 at all times, and during sync fields they are compared in phase with window
25 waveforms (waveform (c)). The multivibrator 403 serves to adjust

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the timings of the associated signals such that each data pulse read by the floppy disk drive is brought to the centre of each window. During data fields, the pulse interval between fetched waveforms sometimes becomes twice or half of the period of windows and so direct comparison between the output from the multivibrator 403 and the window waveforms is impossible. The gate circuit 410 acts to select the signal applied to the comparator 404 based on the sync field signal fed to the terminal 402 and consists of a switch and a flip-flop which is set on the rising portion of each data pulse as shown in waveform (d) and reset on the transition points of each window waveform (waveform (c)), that is, the leading edge and the trailing edge of each pulse. The switch allows the output signal from the flip-flop to be applied to the comparator 404 during data field periods. In this way, during these periods the waveform (b) is compared in phase with each falling portion of the waveform (d) to prevent occurrence of comparison error due to missing pulses. The output waveform shaping circuit 409 brings each fetched pulse to the centre of each window, moves the pulses and shapes them, so that the circuit delivers waveforms as shown by waveform (3). The shaping circuit is made up of a delay circuit such as a one-shot multivibrator.

Figure 6 is a circuit diagram of the conventional VFO shown in Figure 4. The blocks surrounded by phantom lines are denoted by the same reference numerals as those of Figure 4 except for a low-pass filter 601 which does not possess entirely individual circuits

to have both rapid and slow responses, but rather a portion is used for the rapid and slow responses in common in this filter.

The conventional VFO has some disadvantages. First, it is difficult to fabricate the oscillator in the form of a semiconductor integrated circuit as can be seen from Figure 6. The circuitry shown in Figure 6 requires 19 resistors and 6 capacitors as discrete components. It is possible even with the prior art technique to fabricate these components on one chip by attaching the discrete components to the outside surface of the chip and fabricating the other components in semiconductor integrated circuit form. However, features inherent in semiconductor integrated circuitry cannot be fully derived from such a construction. Specifically, the space to mount components cannot be made small. A large number of junction points to not assure a good reliability. The number of steps for mounting components and the cost of fabricating the circuitry cannot be reduced. A considerable limitation is imposed on the design of such a chip for a semiconductor integrated circuit.

In particular, when connections are made to externally attached components from the inside of a semiconductor integrated circuit chip, a considerably larger chip area is needed than the case where no connections are required, because pads for connection and transistors in the outer buffer circuits are several tens of times as large as those of a device dispensing with external connection. Furthermore, the cost of packaging the integrated circuit is increased.

Another disadvantage of the conventional VFO is that adjustments

are necessary after assembly. This is caused by the fact that stable and precise VFOs are not available.

Referring now to Figure 1 there is shown one embodiment of a variable frequency oscillator (VFO) according to the present invention. The VFO includes a counter circuit 201, a crystal oscillator 202, a phase comparator 204, a switching circuit 205, low-pass filters 206, 207, an adder 208, a phase-shift circuit 210, a differentiating circuit 211, a frequency divider circuit 212, a second phase comparator circuit 214 and a second adder 216.

The counter circuit 201 is set by the leading edge of each data pulse, which is read from a floppy disk drive (not shown) and applied to a terminal 219, and counts the pulses generated by the crystal oscillator 202 until a certain count is reached, whereupon the counter 201 is reset and delivers a pulse. The switching circuit 205 selects one of the filters 206, 207 depending on whether a sync field data signal or a data field signal is applied to a terminal 220. The filters have different passbands, and when the sync field signal is to be passed, the filter 206 having a broader passband is selected. The adder 208 forms the sum of the output from either the first filter 206 or the second filter 207 and the output from a third low-pass filter 205 and applies it to the control terminal of a voltage controlled oscillator (VCO) 209 to control the frequency of oscillation of the VCO 209. The differentiating circuit 211 produces a narrow pulse when the trailing edge of the signal from a gate circuit 203 is reached. The adder 216 has the same characteristics as the adder 208 and adds a reference voltage V_r generated by a

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reference voltage source 217 to the output from the filter 21 to control a second voltage-controlled oscillator (VCO) 218, which is designed so as to have the same characteristics as the VCO 209.

Thus the VFO is comprised of a first phase-locked loop, which
5 contains the phase comparator 204, the filter 206 or the filter 207, and the VCO 209, and a second phase-locked loop, which contains the second phase comparator 214, the filter 215 and the VCO 218.

In operation of the VFO constructed as described above, the second phase-locked loop is locked in step with the output signal
10 frequency divider circuit 212, which divides the output frequency of the crystal oscillator 202 down into a lower frequency and delivers a signal of the free-running frequency needed by the VCO 209. Of course, in a state where the second phase-locked loop is locked, the frequency of one input signal to the comparator 214 is equal to
15 that of the other signal and the phase difference between the two signals is kept constant. In other words the VCO 218 also oscillates at the free-running frequency. Even if the constants of the VCO 218 vary due to changes in the power supply voltage or ambient temperature, ageing, scatter in the constants of the components or other factors,
20 the output from the filter 215 is controlled so that the VCO 218 always oscillates at the free-running frequency by virtue of the action of the negative feedback loop.

When the reference voltage V_x , for example half the power supply voltage, is applied to one input terminal of the adder 216 and
25 the output from the filter 215 is applied to one input terminal of

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the adder 208 as shown in Figure 1, the VCO 209 should oscillate at the free-running frequency at the time the output from the filter 206 or the filter 207 equals the reference voltage V_r . As long as the adders and the VCOs are symmetrically accurate, respectively, a VCO entirely free from drift and initial deviation can be attained even if such VCOs are employed that could otherwise not be put into practical use due to their instability. This VCO oscillates at the free-running frequency when the control voltage V_r is applied. The configuration described so far can stabilise the operation of the VCO 209 in the first phase-locked loop.

Referring next to Figure 2(a), the counter circuit 201 is shown in detail. The counter circuit 201 receives a fetched data pulse train (waveform (a) of Figure 5) and delivers pulses whose pulse width is one-fourth the length of 1 bit cell (waveform (b)), that is, flip-flops 302, 303 and a gate 304 produce a short pulse to reset a frequency divider circuit 301 and set a flip-flop 305 on the leading edge of each fetched data pulse which is applied to a terminal 306. A terminal 308 is connected to the crystal oscillator 202 whose output frequency is divided into a lower frequency by the divider circuit 301. When the divider circuit 301 receives pulses of the lower frequency, it delivers a carrier to set a flip-flop 207.

The configuration described thus far offers a one-shot multivibrator stably producing pulses having an accurate pulse width. Also, as can be understood by comparison with the prior art VFO, the

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novel configuration does not require resistor R_1 and capacitor C_1 . The output from the counter circuit 201 is applied to the phase comparator 204, and it is compared in phase with the output waveform (c) of Figure 5 from the VCO 209 and with the waveform (d) during sync field and data field periods, respectively, by the action of the gate circuit 203. The resultant phase difference signal is supplied to the filter 206 responding quickly during sync field periods and to the filter 207 responding slowly during data field periods by the action of the switching circuit 205 to filter out unwanted high frequency components. The output from either filter is applied to the adder 208 to control the frequency of oscillation of the VCO 209. The other input to the adder 208 comes from the second phase-locked loop and causes the VCO 209 to oscillate at the free-running frequency when the output from the filter 206 or the filter 207 is the reference voltage V_x as described previously. The output voltage from the filter 206 or the filter 207 assumes a value of V_x under steady state by making the free-running frequency equal to the window frequency. The absolute value of the current flowing into, or out of, the low-pass filter can be invariably kept constant by setting the voltage V_x to the average value of the output voltage derived when the output from the comparator 204 assumes a logic high state and the output voltage derived when the output from the comparator 204 assumes a logic low state. Further, since the output from the filter can be brought quite close to the voltage V_x under steady state, use of a charge

pumping circuit connected to the output of the comparator 204 dispenses with active filters used in conventional devices as low-pass filters. This makes it very easy to fabricate the VFO in the form of an integrated circuit. The output from the VCO 209 is fed back from the comparator 204 via the gate circuit 203 to form a loop. Thus stable and precise windows can be formed.

In the conventional VFO, a one-shot multivibrator is used as the output waveform shaping circuit 409 to delay each waveform (d) in Figure 5 so that it is moved to the centre of each window (see waveform (c)). The embodiment of the present invention shown in Figure 1 shapes waveforms in a different way. In particular, the differentiating circuit 211 produces short pulses (waveform (g) of Figure 5) on the trailing edge of the waveform (d) and can easily be fabricated by including the flip-flops 302, 303 and the gate 304 of Figure 2(a). The fetched data pulse train takes the waveform (g) of Figure 5, and it is not passed through a delay circuit, thus dispensing with resistors R_{16} , R_{17} and capacitors C_5 , C_6 contrary to the shaping circuit 409 as shown in Figure 6(a). In the embodiment of the invention, as each fetched data pulse (waveform (g)) is brought to the centre of each window, the phase-shift circuit 210 shifts the phase of the windows an angle of 90° or 270° (waveform (f) of Figure 5). This phase shift circuit can be readily constructed by forming a $1/2$ frequency divider circuit by a master-slave flip-flop, because the phases of the output waveforms of the master and slave flip-flops are 90° out of phase. In the conventional VFO

and as shown in Figure 6 a $1/2$ frequency divider circuit 602 is incorporated into the VCO 408 to set the duty cycle of the output waveforms to 50%. The waveforms (c) and (f) of Figure 5 can be readily obtained by feeding the output from the master flip-flop back to the gate circuit 203 and supplying the inverted output of the slave flip-flop to the terminal 221.

All the components of the VFO of Figure 1 except for the low-pass filters 206, 207, 215, adders 208, 216, reference voltage source 217, VCOs 209, 218 and the crystal oscillator can be made as digital circuits. Further, any part externally attached to that semiconductor integrated circuit is not required. In addition VCOs do not need high accuracy or stability as described above.

The circuit stages beginning from the phase comparator 204 and ending with the VCO 209 as well as the circuit stages beginning from the phase comparator 214 and ending with the VCO 218 can be made simpler and can be fabricated in the form of an integrated circuit. Referring next to Figure 2(b), the phase comparators 204, 214, switching circuit 205, low-pass filters 206, 207, 215, adders 208, 216, VCOs 209, 218 and the phase-shift circuit 210 are shown in detail. The blocks surrounded by phantom lines are denoted by the same reference numerals as the components of Figure 1 for correspondence to them except that a low-pass filter 309 corresponds to both the filters 206, 207. The filter 309 includes a portion equivalent to the portion common to both filters 206, 207. Also, because the phase-shift circuit 210 can be attained only by the slave flip-flop

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of the circuit 305 in the VCO 209 as described already, the flip-flop 305 is divided into two by a phantom line. Since the phase comparator 214 and the adder 216 have exactly the same internal configurations as the comparator 204 and the adder 208, respectively, they are not shown in detail. Also, as the VCO 218 is the same as the combination of the VCO 209 and the phase-shift circuit 210, its circuitry is also not shown.

Terminals 301, 302, 303, 304 are connected to the counter circuit 201, gate circuit 203, frequency divider circuit 212 and one input of the gate circuit 203, respectively. The combination of AND gates G_1, G_2 to which transistors T_1, T_2 are connected and the combination of AND gates G_3, G_4 to which transistors T_3, T_4 are connected are alternatively enabled, depending on whether sync field signal or data field signal is applied to a terminal 220. This causes the combination of the transistors T_1, T_2 and the combination of the transistors T_3, T_4 to conduct selectively whereby the phase difference signal is alternately transmitted to a quick response low-pass filter consisting of resistors R_{201}, R_{204} and a capacitor C_{202} and a slow response low-pass filter consisting of resistors $R_{202}, R_{203}, R_{204}$ and capacitors C_{201}, C_{202} . The drain currents of transistors T_{16}, T_{17} are summed in the adder circuits 216, 208, and then the resultant current is converted into a voltage by a transistor T_5 to control the VCO 209. If transistors $T_5, T_6, T_7, T_8, \dots T_9, T_{17}, T_{18}, T_{19}, T_{20}, \dots T_{21}$ have the same constants, then their drain current will be equal to that of the transistor T_5 in the saturation region.

In other words, the drain current of these transistors can be controlled by the gate voltage of the transistors T_{16} , T_{17} . Transistors T_{10} , T_{13} , T_{11} , T_{14} ... T_{12} , T_{15} constitute inverters and their odd-numbered stages are connected together to form ring oscillators whose frequency of oscillation is controlled as the current fed to them is controlled by the gate voltage of the transistors T_{16} , T_{17} . For this purpose, transistors limiting current are connected to the sources of those transistors. The output of the ring oscillators is fed to the flip-flop 305 via a buffer 306, so that the frequency is halved and the duty cycle is modified. No additional phase shift circuit is required by utilising terminal 304 of the master flip-flop of the circuit 305. Since the VCO 209 is stabilised in the manner described previously, it is assured that even ring oscillators whose instability could otherwise not be accepted can be employed. The ring oscillators can be made simply by connecting an odd number of inverter stages to one another, and the ring oscillators do not have parts, such as capacitors, which are required to be externally attached to the semiconductor integrated circuit, and therefore they are quite easy to fabricate in the form of a semiconductor circuit. A reference voltage source 217 has resistors R_{206} , R_{207} for dividing the power supply voltage down to a reference voltage. If the relative accuracy between the resistances of both resistors is good, the derived voltage will be accurately a desired fraction of the power voltage, thereby they easy to incorporate into a semiconductor integrated circuit.

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Of course, a voltage generated using, for example, zener diodes can equally well be used. The current I_0 of a current source 307 is converted into a voltage by a transistor T_{22} to control the gate voltages of transistors T_{26} , T_{28} for limiting the channel currents of the transistors T_{26} , T_{28} . If the transistors T_{22} , T_{26} , T_{28} have the same constants, the currents will be limited to I_0 . A transistor T_{23} converts the current I_0 to a voltage to limit the channel current of a transistor T_{24} . If transistors T_{25} , T_{23} , T_{24} have the same constants, then the currents will be also limited to I_0 . Transistors T_{25} , T_{27} form a switch called a charge pumping circuit which has the same function as the combination of the transistors T_1 , T_3 and the combination of the transistors T_2 , T_4 in the switching circuit 205. The phase difference signal from the comparator 214 causes a capacitor C_{203} to be charged or discharged to control the voltage applied to the second adder 216. As a result, the output phase of the VCO 218 is advanced or retarded.

The low-pass filter 215 consists of the current-limiting transistor T_{24} or T_{28} , the resistor R_{205} and the capacitor C_{203} . Because the currents of the transistors T_{24} , T_{28} are limited to I_0 , the quantity of charge conveyed from the transistor T_{25} or T_{27} to the resistor R_{205} and the capacitor C_{203} is not affected by changes in the potential across the terminals of the capacitor C_{203} , that is, the input voltage of the adder 216. That is, the potential across the capacitor C_{203} can be varied substantially due to changes in constants of the VCO 218, but changes, for example, in the response

constant of the second phase-locked loop caused thereby is held to a minimum.

It will be noted by comparing Figure 1 with Figure 2(b) that the points from which signals are derived for application to the adders 208, 216, respectively, are different from each other. The resistor R_{205} is inserted to stabilise the operation of the second phase-locked loop and so this resistor can be neglected when the circuit of Figure 2(b) is discussed in principle. As such, the two points may be deemed to be the same.

It is to be understood that nearly all components of Figure 2(b) can be fabricated in the form of a complementary MOS integrated circuit. Of course, bipolar or other semiconductor devices may be used with equal utility. The remaining seven resistors and three capacitors are also incorporated into an integrated circuit in the following fashion. First, the resistors R_{206} , R_{207} can be incorporated into the integrated circuit only if their resistances have a sufficient relative accuracy. The accuracy required for the capacitor C_{203} and the resistor R_{205} is relatively low and so these are also capable of being incorporated into the integrated circuit. Likewise, the accuracy necessary for the resistors and capacitors in the filter 309 is not so high and hence they can be incorporated into the integrated circuit. However, the constant of the filter must be varied depending on the kind, that is the dimensions and so on, of the floppy disk connected and so it may be desired that they are attached to the integrated circuit externally. The oscillation

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frequency of each of the VCOs 209, 218 can be increased by the reciprocal of the frequency division factor of a frequency divider circuit connected to the terminal 213 of Figure 1 and the time constant of the filter 215 can be reduced by connecting all or a
5 portion of the frequency divider circuit 212 in series with the terminal 213 and connecting the crystal oscillator 202 directly or the remaining portion of the divider circuit 212 with the second phase comparator 214. This permits the miniaturisation of the capacitor C_{203} , the resistor R_{205} and other elements, whereby the VFO circuit
10 of Figure 1 can be fabricated in the form of an integrated circuit with greater ease.

The VFO of Figure 1 requires an expensive and stable oscillator circuit, such as the crystal oscillator 202. The conventional VFO of Figure 4 does not need such an oscillator circuit when data is read
15 by the floppy disk drive, but needs it when data is written. In the present invention, the crystal oscillator used for the writing operation can also be used for the reading operation and, consequently, neither complication of the configuration nor increase in manufacturing costs is introduced, thus resulting in no problem. One might suppose
20 that the VFO of Figure 1 is more complex than the conventional VFO of Figure 4 and that the manufacturing cost is increased by the addition of a second phase-locked loop. In fact, however, the opposite is the case, Since externally attached parts are reduced substantially, the area occupied by bonding pads for access to the integrated
25 circuit as well as the area required for buffer transistors connected

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to the input and output can be reduced to a great extent. These
occupy a major portion of a semiconductor integrated circuit, and
the area occupied by them is usually considerably larger than the
whole area of the second phase-locked loop. Therefore, it is
5 possible to reduce the cost. The substantial reduction in the
number of externally attached parts further permits decrease in the
cost of parts, assembly cost and the packaging space and increase in
reliability. Furthermore, VCOs dispense with adjustments during
assembly operation because the free-running frequency is adjusted
10 automatically.

As described so far, in accordance with the present invention,
the addition of a second phase-locked loop permits stabilisation of
components including VCOs and so accurately fabricated components
are not required, so that the components can be fabricated in the
15 form of a semiconductor integrated circuit with greater ease.
Also, the circuit can be fabricated in the form of a digital circuit
by making the best use of the reference frequency signal generated
by the crystal oscillator and replacing a conventionally used one-shot
multivibrator with a counter circuit. The result is that the circuit
20 is made more accurate and the number of components is reduced.

A variable frequency oscillator circuit according to the present
invention can be formed into a semiconductor integrated circuit with
greater extent than the conventional VFO, thus permitting simplification
of design of instruments and apparatus, increase in reliability of
25 apparatus, decrease in the number of steps for assembly, miniaturisation

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of apparatus and reduction in the manufacturing cost.

It is to be noted that the present invention can find application in VFOs for hard disks and other phase-locked loops in the form of semiconductor integrated circuits.

CLAIMS

1. A variable frequency oscillator comprising: a first phase-locked loop including a first voltage controlled oscillator; a second phase-locked loop including a second voltage controlled oscillator having the same constants as the first voltage controlled oscillator;
5 an oscillator means for generating a stable pulse train; the arrangement being such that, in operation, the first phase-locked loop is synchronised with a sequence of input data, the second phase-locked loop is synchronised with the pulse train from the oscillator means, and the first voltage controlled oscillator in
10 the first phase-locked loop is stabilised by a control voltage applied to the second voltage controlled oscillator in the second phase-locked loop; and a digital circuit for counting pulses generated at regular intervals and delaying the pulses by a predetermined period of time to delay the sequence of the input data before
15 application to the first phase-locked loop.
2. A variable frequency oscillator as claimed in claim 1 including a ring oscillator for controlling the frequency of oscillation of each voltage controlled oscillator by controlling the current flowing into the ring oscillator.
- 20 3. A variable frequency oscillator as claimed in claim 1 or 2 comprising shifting means for shifting the phase of each output pulse from the first voltage controlled oscillator in the first phase-locked loop by 90° , a flip-flop circuit arranged to be set by the input data and reset by the output from the shifting means,
25 and a circuit arranged to be triggered on the trailing edge of the



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output from the flip-flop circuit for delivering a pulse having a predetermined pulse width.

4. . A variable frequency oscillator substantially as herein described with reference to Figures 1, 2(a) and 2(b) of the
- 5 accompanying drawings.
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