

Description

This invention relates generally to a monolithic integrated circuit switch which buffers output circuitry coupled thereto from extreme voltage transients that may occur at the input of the switch. More particularly, the present invention relates to a three terminal integrated low resistance switch circuit suitable for use in an automotive application to protect load electronics coupled therewith from voltage transients that may occur at the input thereof which otherwise could damage or destroy the load electronics.

Any electronic circuit utilized in an automotive system may be subjected to abnormal transients that occur on the battery bus. For example, the nominal battery voltage appearing on the battery bus is +12 volts but under jump start conditions, when two batteries are placed in series, +24 volts may be supplied to the electronics coupled to the battery bus. Another abnormal condition that can occur results from the battery terminals being reversed. Under this condition upwards to -13 volts may be present on the battery bus.

Still another abnormal condition specified by the automotive industry is referred to as voltage load dump therein it may be possible to have 60 volts occurring on the battery bus. One other condition specified by most automotive manufacturers is that all electronics must be able to withstand ± 125 volts inductive transients on the battery bus.

Most semiconductor manufacturing processes used today to fabricate monolithic integrated circuits for use in automotive systems can withstand 24 volts applied to the integrated chip. However, in almost all cases, present day solid state electronics cannot stand the 60 volt load dump condition due to breakdown problems as well as power dissipation problems of the integrated chip.

Thus, at least one automotive manufacturer uses a discrete transient protection circuit to protect the load electronics connected thereto from the above described abnormal conditions. This circuit comprises a 100 joule varistor connected from the battery bus to ground, a high current Schottky diode coupled in series between the positive terminal of the battery and the output of the circuit, and a Zener diode connected in series with a diode-clamp between the battery bus and ground. The varistor protects the electronics from positive voltage transients while the Zener diode and diode clam protect the Schottky diode from destructive reverse voltage transients.

Although the above discrete protection circuit functions quite well, the discrete components compromise space, and performance needs. Additionally, the several discrete components are relatively expensive to the automotive manufacturer.

A monolithic integrated circuit in accordance with the prior art portion of claim 1 is disclosed in US-A-4,319,181.

The invention seeks to provide a simple, reliable

and rather inexpensive solid state circuit to replace the discrete protection circuit described above.

According to the invention the base of said vertical PNP transistor is formed by a region in the epitaxial layer of the integrated circuit, the emitter of said vertical PNP transistor is formed by a region of said epitaxial layer, the control circuit means is formed in said epitaxial layer and is arranged to drive said vertical PNP transistor into saturation upon application of said external signal, whereby said substrate is maintained at a more positive potential than said epitaxial layer, and the sense circuit means comprises a separate region of semiconductor material of like conductivity as said emitter region of said vertical PNP transistor in close proximity to said vertical PNP transistor, the control circuit means being responsive to the feedback control signal provided by the sense circuit means to minimise the base current drive of said saturated vertical PNP transistor with respect to the collector current thereof.

Embodiments of the present invention may provide; a 3-terminal integrated low resistant switch which buffers load circuitry coupled thereto from otherwise extreme damaging voltage conditions that may occur across the input thereof;

a low resistance, monolithic integrated switch circuit suited for use in automotive systems to minimize loss of voltage between the input to output thereof while protecting the load connected to the switch from voltage transients that otherwise may damage the same;

monolithic integrated protection circuit having a series-pass transistor switch having a collector formed by the substrate of the integrated circuit which is normally operated at a potential greater than that of the control circuitry components;

circuitry for controlling the conduction of a transistor switch, which circuitry is operated with all epitaxial regions biased at a voltage substantially equal to the input voltage applied to the transistor switch.

The single Figure is a schematic illustrating the monolithic integrated circuit of the present invention.

Turning to the Figure there is shown protection circuit 10 of the present invention which is suited to be manufactured in monolithic integrated circuit form using known process techniques. protection circuit 10 is a three terminal circuit including input terminal 12, output terminal 14 and common terminal 16. Protection circuit 10 may be packaged in a standard, three-terminal TO-220 power package.

A series-pass PNP transistor 20 has its emitter and collector path comprising collector 20a coupled between input and output terminals 12 and 14 respectively. As will hereafter be discussed, in response to an external signal being applied across terminals 12 and 16, transistor 20 provides a low resistance path to supply an output signal between output terminal 14 and common terminal 16 to drive load circuitry which would be coupled thereacross.

The conduction of series-pass switch transistor

20 is controlled by a control circuit comprising DMOS FIELD EFFECT TRANSISTOR (FET) 22 which has its source-drain path coupled between the base of transistor 20 and common terminal 16. As the magnitude of the externally applied signal exceeds a low threshold value, which forward biases PNP transistor 24, current flows from collector 24a through resistor 26 which pulls up the gate of DMOS FET 28 thereby rendering it conductive. FET 28 provides a current path via its source-drain for current to flow from the base of transistor 24 through resistor 30 to common terminal 16. The gate of NMOS FET 32 therefore is forward biased rendering this FET conductive thereby providing a feedback action to the gate of FET 28. This causes collector 24a to be regulated to source a current of value equal to the threshold potential value of FET 32 divided by the magnitude of resistor 30, plus a small current through resistor 26. Collector 24b of transistor 24 mirrors this current to provide a source of current through resistor 33 that causes FET 22 to become conductive as a positive potential is applied, via resistor 34, to the gate of the transistor. Transistor 20 is thus rendered conductive as a base conduction path is thereby provided.

As the externally applied signal increases beyond the aforementioned threshold value, transistor 20 is driven hard toward saturation independent of any load connected across terminals 14 and 16. As will be later explained the structure of transistor 20, comprising collector 20a is such that a low input-to-output voltage drop occurs across the emitter and collector wherein the voltage developed at output terminal 14 is substantially equal to the magnitude of the applied external signal. Hence, as the applied signal increases beyond the aforementioned threshold value, transistor 20 is driven into saturation and the current is regulated by the control circuit to only that base value necessary to supply only that current required by the load electronics coupled to output terminal 14. The current through transistor 20 is regulated by controlling the conduction of FET 22. By reducing the flow of current through FET 22, transistor 20 is rendered less conductive and vice-versa.

Several mechanisms are provided for regulating the current through transistor 20. An important aspect of the present invention is the efficiency of the protection circuit, i.e., the amount of base current required versus the output current supplied at output terminal 14. For maximum efficiency, only enough base current should be sourced from transistor 20, through FET 22, as is required by the load. To insure maximum efficiency a saturation sense and shut down feedback path is provided which senses when transistor 20 goes into saturation. Current is sourced via the feedback path that includes sense collector 36, resistors 38 and 40, to terminal 16 as transistor 20 becomes saturated. This feedback path forward biases the gate-source of NMOS FET 42. FET 42 is therefore rendered conductive to pull the gate of transistor 22 down thereby reducing base current

drive to transistor 20 to only that value required to maintain saturation of transistor 20 at the required load current.

Transistor 20, comprising collector 20a, is a vertical PNP structure, i.e., the collector 20a is formed by a portion of the P-type substrate of the integrated circuit. The base of transistor is formed by the epitaxial region which is formed on the substrate and the emitter is formed by a P type region that may be diffused into the epitaxial layer as understood. The saturation sense feedback path is nominally formed by a transistor which would have its emitter formed by the substrate, its base formed by the epitaxial layer common with transistor 20 and a collector region formed by a separate P-type region. The feedback current is collected by sense collector 36 of the saturation sense transistor as the substrate-epitaxial junction of the integrated circuit is forward biased by transistor 20 becoming saturated.

In view of the above, it should be noted that in typical operation, the substrate (collector 20a of transistor 20) is operated at a greater potential than the control circuitry. This is not generally the case as typically the substrate of a bipolar integrated circuit is maintained at the most negative potential.

Protection circuit 10 also provides short circuit current protection to limit the output current sourced at terminal 14 to a predetermined maximum value. The output current is continually monitored via collector 20b. Collector 20b is laterally formed with respect to the emitter-base regions of transistor 20. The current source through collector 20b flows through resistor 40 to ground reference through terminal 16. If a short condition occurs, the currents flowing through collectors 20a and 20b will increase proportionally until a value is reached at which the voltage drop across resistor 40 is sufficient to render transistor 42 conductive. This condition will forward bias FET 42 to reduce base current drive to transistor 20 flowing through FET 22 as this device is rendered less conductive. Thus, the current sourced by series-pass transistor 20 to terminal 14 can only increase to a maximum value which thereafter remains constant.

Over voltage protection is provided by circuitry comprising multi-collector transistor 44 and series-connected Zener diodes 46, 48 and 50 and resistor 52. If the voltage applied at input terminal 12 exceeds a predetermined value, for example, +28 volts, the combined breakdown voltage of the Zener diodes is exceeded. This condition produces a voltage at the gate of transistor 42 to render it conductive thereby rendering FET 22 nonconductive. This action inhibits base drive to transistor 20. Hence, positive voltage transients that exceed a predetermined value (set by the Zener breakdown voltages of the Zener diodes) are buffered from appearing at output terminal 14.

Protection circuit 10 also includes a thermal shut-down circuit for turning off transistor 20 when the power consumption and/or ambient

temperature of the integrated chip exceeds a predetermined temperature value. Thus, if the ambient temperature plus the temperature of the integrated circuit, due to power consumption, exceeds this predetermined temperature, transistor 20 is shut down to protect both the protection circuit and the load electronics connected therewith. Thermal shut-down is provided by current source 54, transistor 56 and resistor 58.

Current source 54 generates a positive temperature coefficient (TC) current utilizing any known $\Delta V_{BE}/R$ current generating circuit. The positive TC current is sourced through resistor 58 to common terminal 16. Hence, a voltage is developed across resistor 58 which has a predetermined positive temperature coefficient as understood. As the temperature of the chip increases, the voltage developed across resistor 58 increases while the VBE threshold voltage of transistor 56 decreases. At the predetermined temperature transistor 56 will be turned on to pull up the gate of FET 42. This causes both transistors 22 and 20 to regulate the circuit power dissipation and, in turn, limit the chip temperature to a nondestructive value.

Zener diode 60 is coupled between the gate of FET 42 and common terminal 16 to provide gate protection by clamping the gate at a predetermined voltage. Thus, diode 60 is rendered conductive as the voltage at the gate of transistor 42 reaches the break-down voltage of the Zener, due to a high potential appearing at input 12, to shunt excess current supplied through Zener diodes 46-50.

Negative voltage transient protection is provided by, in every case, having a PN junction connected to input terminal 12, i.e., the emitters of transistors 20, 24, and 44. The emitter-base junction of these transistors exhibit a high reverse voltage break-down characteristic to buffer the output terminal 14 from any negative voltage transients that may appear at input terminal 12.

An additional feature incorporated into protection circuit 10 is the extension of the reverse break-down voltage (BV_{CEO}) of transistor 20 during high positive transient input voltages appearing at input terminal 12. The additional collector of transistor 44 that is tied to the base of transistor 20 supplies any leakage current from the base-to-collector of transistor 20 when transistor 44 is rendered conductive. Thus, any high input voltage condition that essentially cause the base of transistor 20 to be open-circuited due to transistor 22 being rendered non-conductive allows transistor 44 to provide the leakage current drawn by transistor 20.

Typically, protection circuit 10 buffers the load electronics from abnormal voltage transients by causing one of the above described mechanisms to shut down transistor 20 by open circuiting the base-electrode thereto. Under normal operating conditions transistor 20 operates as a low resistance switch that is caused to be opened, to disconnect the load electronics from the input, under high input voltage conditions.

It is recognized that in today's microprocessor controlled automotive systems that series-pass transistor 20 could be opened, or turned off, anytime by a suitable control signal from the microprocessor to render transistor 22 nonconductive by causing the gate of transistor 42 to go positive. In this manner, increased functionality of protection circuit 10 is possible which would require a single additional control pin coupled to the gate of transistor 42.

Still further, it is deemed well within the skill of one in the art in view of the above described protection circuit to implement additional functional elements on the same IC chip such as a regulated standby voltage supply drive memory circuits that may be included on the chip with the protection circuit.

Additionally, it is also deemed within the skills of one familiar to the art in view of the teachings of the present invention to implement circuitry for controlling the series pass transistor in the linear (non-saturated) mode to provide output voltage or current regulation.

In summary, several key features are provided by protection circuit 10 of the present invention. The integrated protection circuit can withstand ± 125 volt transients appearing at the input thereof while buffering the load electronics therefrom. Additionally, the protection circuit exhibits an extremely low input-to-output voltage drop thereacross such that the output voltage nearly tracks the input voltage up to a predetermined value after which the output becomes open-circuited. Another novel feature of the present invention is, due to the vertical structure of the switching series-pass transistor 20, the substrate (collector of transistor 20) is operated at a voltage level greater than the epitaxial layer within which the control circuitry is formed. Moreover, the use of the vertical PNP structure provides several advantages among which is the severe reduction in die size required to fabricate the protection circuit. Further, the vertical PNP structure increases the efficiency of the protection circuit since a higher beta is realized that produces a much lower stand-by current.

An aspect of the present invention is the combination of bipolar process technology with MOS process technology on a single integrated chip wherein the DMOS controlling circuitry is operated at a lower potential than the collector of the vertical PNP series pass device. The use of DMOS is required to withstand the high positive voltage excursion that may occur at the input of the protection circuit which standard bipolar devices could not withstand.

Claims

1. A monolithic integrated circuit comprising:
a vertical structured PNP transistor (20) having an emitter and a collector (20a) coupled respectively to the input (12) and the output (14) of the integrated circuit and a base, said collector (20a) being formed by a portion of the substrate com-

temperature of the integrated chip exceeds a predetermined temperature value. Thus, if the ambient temperature plus the temperature of the integrated circuit, due to power consumption, exceeds this predetermined temperature, transistor 20 is shut down to protect both the protection circuit and the load electronics connected therewith. Thermal shut-down is provided by current source 54, transistor 56 and resistor 58.

Current source 54 generates a positive temperature coefficient (TC) current utilizing any known $\Delta V_{BE}/R$ current generating circuit. The positive TC current is sourced through resistor 58 to common terminal 16. Hence, a voltage is developed across resistor 58 which has a predetermined positive temperature coefficient as understood. As the temperature of the chip increases, the voltage developed across resistor 58 increases while the VBE threshold voltage of transistor 56 decreases. At the predetermined temperature transistor 56 will be turned on to pull up the gate of FET 42. This causes both transistors 22 and 20 to regulate the circuit power dissipation and, in turn, limit the chip temperature to a nondestructive value.

Zener diode 60 is coupled between the gate of FET 42 and common terminal 16 to provide gate protection by clamping the gate at a predetermined voltage. Thus, diode 60 is rendered conductive as the voltage at the gate of transistor 42 reaches the break-down voltage of the Zener, due to a high potential appearing at input 12, to shunt excess current supplied through Zener diodes 46-50.

Negative voltage transient protection is provided by, in every case, having a PN junction connected to input terminal 12, i.e., the emitters of transistors 20, 24, and 44. The emitter-base junction of these transistors exhibit a high reverse voltage break-down characteristic to buffer the output terminal 14 from any negative voltage transients that may appear at input terminal 12.

An additional feature incorporated into protection circuit 10 is the extension of the reverse break-down voltage (BV_{CEO}) of transistor 20 during high positive transient input voltages appearing at input terminal 12. The additional collector of transistor 44 that is tied to the base of transistor 20 supplies any leakage current from the base-to-collector of transistor 20 when transistor 44 is rendered conductive. Thus, any high input voltage condition that essentially cause the base of transistor 20 to be open-circuited due to transistor 22 being rendered non-conductive allows transistor 44 to provide the leakage current drawn by transistor 20.

Typically, protection circuit 10 buffers the load electronics from abnormal voltage transients by causing one of the above described mechanisms to shut down transistor 20 by open circuiting the base-electrode thereto. Under normal operating conditions transistor 20 operates as a low resistance switch that is caused to be opened, to disconnect the load electronics from the input, under high input voltage conditions.

It is recognized that in today's microprocessor controlled automotive systems that series-pass transistor 20 could be opened, or turned off, anytime by a suitable control signal from the microprocessor to render transistor 22 nonconductive by causing the gate of transistor 42 to go positive. In this manner, increased functionality of protection circuit 10 is possible which would require a single additional control pin coupled to the gate of transistor 42.

Still further, it is deemed well within the skill of one in the art in view of the above described protection circuit to implement additional functional elements on the same IC chip such as a regulated standby voltage supply drive memory circuits that may be included on the chip with the protection circuit.

Additionally, it is also deemed within the skills of one familiar to the art in view of the teachings of the present invention to implement circuitry for controlling the series pass transistor in the linear (non-saturated) mode to provide output voltage or current regulation.

In summary, several key features are provided by protection circuit 10 of the present invention. The integrated protection circuit can withstand ± 125 volt transients appearing at the input thereof while buffering the load electronics therefrom. Additionally, the protection circuit exhibits an extremely low input-to-output voltage drop thereacross such that the output voltage nearly tracks the input voltage up to a predetermined value after which the output becomes open-circuited. Another novel feature of the present invention is, due to the vertical structure of the switching series-pass transistor 20, the substrate (collector of transistor 20) is operated at a voltage level greater than the epitaxial layer within which the control circuitry is formed. Moreover, the use of the vertical PNP structure provides several advantages among which is the severe reduction in die size required to fabricate the protection circuit. Further, the vertical PNP structure increases the efficiency of the protection circuit since a higher beta is realized that produces a much lower stand-by current.

An aspect of the present invention is the combination of bipolar process technology with MOS process technology on a single integrated chip wherein the DMOS controlling circuitry is operated at a lower potential than the collector of the vertical PNP series pass device. The use of DMOS is required to withstand the high positive voltage excursion that may occur at the input of the protection circuit which standard bipolar devices could not withstand.

Claims

1. A monolithic integrated circuit comprising:
a vertical structured PNP transistor (20) having an emitter and a collector (20a) coupled respectively to the input (12) and the output (14) of the integrated circuit and a base, said collector (20a) being formed by a portion of the substrate com-



prising the integrated circuit, control circuit means (24, 42, 22) which is responsive to an external signal applied to the input (12) of the integrated circuit for controlling the conduction of said vertical PNP transistor (20), and sense circuit means (36) for providing a feedback control signal to an input of said control circuit means (24, 42, 22), characterised in that the base of said vertical PNP transistor is formed by a region in the epitaxial layer of the integrated circuit, the emitter of said vertical PNP transistor is formed by a region of said epitaxial layer, the control circuit means (24, 42, 22) is formed in said epitaxial layer and is arranged to drive said vertical PNP transistor (20) into saturation upon application of said external signal, whereby said substrate is maintained at a more positive potential than said epitaxial layer, and the sense circuit means comprises a separate region (36) of semiconductor material of like conductivity as said emitter region of said vertical PNP transistor (20) in close proximity to said vertical PNP transistor (20), the control circuit means (24, 42, 22) being responsive to the feedback control signal provided by the sense circuit means (36) to minimise the base current drive of said saturated vertical PNP transistor (20) with respect to the collector current thereof.

2. The circuit of claim 1 wherein said control circuit means includes: a first field effect transistor (FET) (22) having a gate, source and drain electrodes, said source-drain electrodes being coupled in series between said base of said PNP transistor (20) and a common terminal (16) of the circuit;

a first transistor (24) of like conductivity type as said PNP transistor (20) having an emitter coupled to the input (12) of the circuit, a base, first and second collectors (24a, 24b);

latch circuit means (28, 32) coupled between said base and first collector (24a) of said first transistor (24) to said common terminal (16) for regulating the collector current sourced from said first collector (24a);

and first circuit means (33, 34) for coupling said second collector (24b) of said first transistor (24) with said gate of said first FET (22).

3. The circuit of claim 2 wherein said control circuit means further includes a second FET (42) having a source-to-drain path coupled in series between said gate of said first FET (22) and said common terminal (16), the gate thereof being coupled to said input of said control circuit means.

4. The circuit of claim 2 or 3 wherein said latch circuit means includes:

a third FET (28) having a gate and a source-drain path coupled in series between said base of said first transistor (24) and a common node;

a fourth FET (32) having a gate coupled to said common node and a source-drain path coupled in series between said base of said first transistor (24) and said common terminal (16).

5. The circuit of any one of claims 1 to 4 including protection circuit means (44, 46, 48, 50)

coupled between the input 12 of the circuit and said input of said control circuit means (24, 42, 22) for providing a control signal thereto in response to said external signal exceeding a predetermined value such that said PNP transistor (20) is rendered nonconductive.

6 The circuit of any preceeding claims including short circuit protection means (20b, 40) coupled to said input of said control circuit means which is responsive to said collector current of said PNP transistor exceeding a predetermined value for providing a control signal to said control circuit means (42, 22) to regulate said collector current at substantially said predetermined value.

7. The circuit of claim 5 wherein said protection circuit means includes.

a second transistor (44) having an emitter coupled to the input (12) of the circuit, a base and a collector, said base and collector being interconnected; and

Zener diode means (46, 48, 50) coupled between said interconnected base and collector of said second transistor (44) and said input of said control circuit means (42, 22).

8. The circuit of claim 6 wherein said short circuit protection means comprises a second collector region (20b) of said PNP transistor (20) formed in lateral spaced relationship to said emitter and base of said PNP transistor (20) said second collector region (20b) being coupled to said input of said control circuit means (42, 22).

9. The circuit of claim 7 wherein said second transistor (44) of said protection circuit includes a second collector coupled to said base of said PNP transistor (20).

Patentansprüche

1. Monolithische integrierte Schaltung, enthalten:

Einen vertikal aufgebauten PNP-Transistor (20), der einen Emittor und einen Kollektor (20a) hat, die mit dem Eingang (12) beziehungsweise dem Ausgang (14) der integrierten Schaltung verbunden sind, und mit einer Basis, wobei der Kollektor (20a) durch eine Abschnitt des Substrats gebildet ist, der die integrierte Schaltung enthält, mit einer Steuerschaltungseinrichtung (24, 42, 22), die auf ein äußeres Signal anspricht, das dem Eingang (12) der integrierten Schaltung zugeführt wird, um die leitung des genannten vertikalen PNP-Transistors (20) zu steuern, und eine Fühlerschaltungseinrichtung (36) zum Erzeugen eines Rückkopplungssteuersignals zu einem Eingang der genannten Steuerschaltungseinrichtung (24, 42, 22), dadurch gekennzeichnet, daß die Basis des genannten vertikalen PNP-Transistors durch einen Bereich in der epitaxialen Schicht der integrierten Schaltung gebildet ist, der Emittor des vertikalen PNP-Transistors von einem Bereich der epitaxialen Schicht gebildet ist, die Steuerschaltungseinrichtung (24, 42, 22) in der epitaxialen Schicht gebildet ist und dazu eingerichtet ist, den vertikalen PNP-Transistor (20) bei Anliegen des genannten äußeren Signals in die Sätti-



gung zu treiben, wodurch das Substrat in einem mehr positiven Potential gehalten wird, als die Epitaxialschicht und die Fühlschaltungseinrichtung einen getrennten Bereich (36) des Halbmateriale von gleicher Leitfähigkeit wie der genannte Emittierbereich des vertikalen PNP-Transistors (20) in dichter Nachbarschaft zu dem vertikalen PNP-Transistor (20) aufweist, die Steuerschaltungseinrichtung (24, 42, 22) auf das Rückkopplungssteuersignal anspricht, das von der Fühlschaltungseinrichtung (36) zur Verfügung gestellt wird, um die Basisstromansteuerung des gesättigten vertikalen PNP-Transistors (20) in Bezug auf den Kollektorstrom desselben zu minimieren.

2. Schaltung nach Anspruch 1, bei der die genannte Steuerschaltungseinrichtung enthält:

Einen ersten Feldeffekt-Transistor (FET) (22) mit Gate-, Source- und Drainelektroden, wobei die Source-Drainelektroden in Serie zwischen die Basis des PNP-Transistors (20) und einen gemeinsamen Anschluß (16) der Schaltung geschaltet ist;

einen ersten Transistor (24) vom selben Leitfähigkeitstyp wie der genannte PNP-Transistor (20), mit einem Emittier, der mit dem Eingang (12) der Schaltung verbunden ist, einer Basis und ersten und zweiten Kollektoren (24a, 24b);

eine Verriegelungsschaltungseinrichtung (28, 32), die zwischen der Basis und dem ersten Kollektor (24a) des ersten Transistors (24) und dem gemeinsamen Anschluß (16) angeordnet ist, um den Kollektorstrom, der von dem ersten Kollektor (24a) kommt, zu regeln;

eine erste Schaltungseinrichtung (33, 34) zum Verbinden des zweiten Kollektors (24b) des ersten Transistors (24) mit dem Gate des ersten FET (22).

3. Schaltung nach Anspruch 2, bei der die Steuerschaltungseinrichtung weiterhin einen zweiten FET (42) enthält, der eine Source-Drain-Strecke hat, die in Serie zwischen das Gate des ersten FET (22) und dem genannten gemeinsamen Anschluß (16) geschaltet ist und dessen Gate mit dem Eingang der Steuerschaltungseinrichtung verbunden ist.

4. Schaltung nach Anspruch 2 oder 3, bei der die Verriegelungsschaltungseinrichtung enthält:

Einen dritten FET (28), mit einem Gate und einer Source-Drain-Strecke, die in Serie zwischen die Basis des ersten Transistors (24) und einem gemeinsamen Verbindungspunkt geschaltet ist;

einen vierten FET (32) mit einem Gate, das mit dem gemeinsamen Verbindungspunkt verbunden ist, und einer Source-Drain-Strecke, die in Serie zwischen die Basis des ersten Transistors (24) und den genannten gemeinsamen Anschluß (16) geschaltet ist.

5. Schaltung nach einem der Ansprüche 1 bis 4, enthaltend eine Schutzschaltungseinrichtung (44, 46, 48, 50), die zwischen den Eingang (12) der Schaltung und den Eingang der Steuerschaltungseinrichtung (24, 42, 22) geschaltet ist, um ihr ein Steuersignal in Abhängigkeit davon zuzuführen, daß das genannte äußere Signal einen vorbestimmten Wert übersteigt, so daß der PNP-Transistor (20) nicht-leitend gemacht wird.

6. Schaltung nach einem der vorhergehenden Ansprüche, enthaltend eine Kurzschluß-Schutz-einrichtung (20b, 40), die mit dem Eingang der Steuerschaltungseinrichtung verbunden ist und die darauf anspricht, daß der Kollektorstrom des PNP-Transistors einen vorbestimmten Wert übersteigt, um ein Steuersignal an die Steuerschaltungseinrichtung (42, 44) abzugeben, um den Kollektorstrom auf den im wesentlichen vorbestimmten Wert zu regeln.

7. Schaltung nach Anspruch 5, bei der die Schutzschaltungseinrichtung enthält:

Einen zweiten Transistor (44) mit einem Emittier, der mit dem Eingang (12) der Schaltung verbunden ist, einer Basis und einem Kollektor, wobei die Basis und der Kollektor miteinander verbunden sind;

eine Zenerdiodeneinrichtung (46, 48, 50), die zwischen die miteinander verbundenen Basis und Kollektor des zweiten Transistors (44) und den genannten Eingang der Steuerschaltungseinrichtung (42, 22) geschaltet ist.

8. Schaltung nach Anspruch 6, bei der die Kurzschluß-Schutz-einrichtung einen zweiten Kollektorbereich (20b) des PNP-Transistors (20) enthält, der in quer beabstandeten Verhältnis zu dem genannten Emittier und der Basis des PNP-Transistors (20) ausgebildet ist, wobei der zweite Kollektorbereich (20b) mit dem Eingang der Steuerschaltungseinrichtung (42, 22) verbunden ist.

9. Schaltung nach Anspruch 7, bei der zweite Transistor (44) der genannten Schutzschaltung einen zweiten Kollektor enthält, der mit der Basis des PNP-Transistors (20) verbunden ist.

Revendications

I. Circuit intégré monotithique comportant;
un transistor PNP (20) de structure verticale comprenant un collecteur et un émetteur (20a) couplés respectivement avec l'entrée (12) et la sortie (14) du circuit intégré et une base, ledit collecteur (20a) étant formé par une partie du substrat constituant le circuit intégré, un circuit de commande (24,42,22) qui réagit à un signal extérieur appliqué à l'entrée (12) du circuit intégré en commandant la conduction dudit transistor PNP vertical (20) et un circuit de détection (36) qui produit un signal de commande de réaction à une entrée dudit circuit de commande (24,42,22), caractérisé en ce que la base dudit transistor PNP vertical est formée par une région dans la couche épitaxiale du circuit intégré, l'émetteur dudit transistor PNP vertical est formé par une région de ladite couche épitaxiale, le circuit de commande (24,42,22) est formé dans ladite couche épitaxiale et il est agencé pour attaquer ledit transistor PNP vertical (20) à saturation, à l'application dudit signal extérieur, dans lequel ledit substrat est maintenu à un potentiel plus positif que ladite couche épitaxiale et le circuit de détection comporte une région séparée (36) de matière semi-conductrice de même conductivité que ladite région d'émetteur dudit transistor PNP vertical (20) en toute proximité dudit transistor



PNP vertical (20), le circuit de commande (24,42,22) réagissant au signal de commande de réaction produit par le circuit de détection (36) en réduisant au minimum l'attaque de courant de base dudit transistor PNP vertical (20) saturé par rapport à son courant de collecteur.

2. Circuit selon la revendication 1, dans lequel ledit circuit de commande comporte; un premier transistor à effet de champ (FET) (22) comprenant des électrodes de grille, de source et de drain, lesdites électrodes de source-drain étant connectées en série entre ladite base dudit transistor PNP (20) et une borne commune (16) du circuit;

un premier transistor (24) du même type de conductivité que ledit transistor PNP (20) comprenant un émetteur connecté à l'entrée (12) du circuit, une base, un premier et un second collecteurs (24a,24b);

un circuit de verrouillage (28,32) couplé entre ladite base et le premier collecteur (24a) dudit premier transistor (24) et ladite borne commune (16) pour réguler le courant de collecteur émis par le dit premier collecteur (20a); et

un premier circuit (33,34) pour coupler ledit second collecteur (24b) dudit premier transistor (34) avec ladite grille dudit premier FET (22).

3. Circuit selon la revendication 2, dans lequel ledit circuit de commande comporte en outre un second FET (42) comprenant un circuit source-drain couplé en série entre ladite grille dudit premier FET (22) et ladite borne commune (16), sa grille étant couplée avec ladite entrée dudit circuit de commande.

4. Circuit selon la revendication 2 ou 3, dans lequel ledit circuit de verrouillage comporte;

un troisième FET (28) comprenant une grille et un circuit source-drain couplé en série entre ladite base dudit premier transistor (24) et un point commun;

un quatrième FET (32) comprenant une grille couplée avec ledit point commun et un circuit source-drain couplé en série entre ladite base

audit premier transistor (24) et ladite borne commune (16).

5. Circuit selon l'une quelconque des

revendications 1 à 4, comportant un circuit de protection (44,46,48,50) couplé entre l'entrée (12) du circuit et ladite entrée dudit circuit de commande (24,42,22) pour produire un signal de commande en réponse audit signal extérieur dépassant une valeur prédéterminée de manière que ledit transistor PNP (20) soit rendu non conducteur.

6. Circuit selon l'une quelconque des revendications précédentes, comprenant un circuit de protection des courts-circuits (20b,40) couplé avec la dite entrée dudit circuit de commande, qui réagit audit courant de collecteur dudit transistor PNP dépassant une valeur prédéterminée en produisant un signal de commande pour ledit circuit de commande (42,22) afin de réguler ledit courant de collecteur à pratiquement ladite valeur prédéterminée.

7. Circuit selon la revendication 5, dans laquelle circuit de protection comporte;

un second transistor (44) comprenant un émetteur couplé avec l'entrée (12) du circuit, une base et un collecteur, ladite base et le collecteur étant interconnectés; et

un circuit à diodes Zéner (46,48,50) couplé entre ladite base et ledit collecteur interconnectés dudit second transistor (44) et ladite entrée dudit circuit de commande (42,22).

8. Circuit selon la revendication 6, dans lequel ledit circuit de protection contre les courts-circuits comporte une première région de collecteur (20b) dudit transistor PNP (20) formée dans une relation d'espacement latéral avec ledit émetteur et ladite base dudit transistor PNP (20), ladite seconde région de collecteur (20b) étant couplée avec ladite entrée dudit circuit de commande (42,22).

9. Circuit selon la revendication 7; dans lequel ledit second transistor (44) dudit circuit

de protection comporte un second collecteur couplé avec ladite base dudit transistor PNP (20).

