

ABSTRACT**PROCESS FOR FABRICATING A CFET DEVICE**

5 The invention relates to a process for fabricating a CFET device, characterized in that it comprises:

- forming a double semiconductor-on-insulator substrate comprising, in succession, from its base to its surface: a carrier substrate (1), a first electrically insulating layer (2a), a first single-crystal semiconductor layer (2b), a second electrically insulating layer (3a) and
10 a second single-crystal semiconductor layer (3b);

- forming trenches from the surface of said substrate, to the first electrically insulating layer (2a), so as to form at least one fin (F),

- in each fin (F), forming a channel of a first transistor in the first semiconductor layer (2b) and a channel of a second transistor of opposite type to the first transistor in the
15 second semiconductor layer (3b),

the formation of the double semiconductor-on-insulator substrate comprising:

- a first layer-transfer step in order to transfer the first electrically insulating layer (2a) and the first single-crystal semiconductor layer (2b) to the carrier substrate (1), so as to form a first semiconductor-on-insulator substrate, said first layer-transfer step comprising
20 a heat treatment at a sufficiently high temperature to smooth the first single-crystal semiconductor layer to a roughness lower than 0.1 nm RMS,

- after said heat treatment, a second layer-transfer step in order to transfer the second electrically insulating layer (3a) and the second single-crystal semiconductor layer (3b) to the first single-crystal semiconductor layer of the first semiconductor-on-insulator
25 substrate.

Fig. 1