DISCONTINUOUS PATTERNED BONDS FOR SEMICONDUCTOR DEVICES AND ASSOCIATED SYSTEMS AND METHODS

TECHNICAL FIELD

[0001] The present technology is directed generally to discontinuous bonds for semiconductor devices, and associated systems and methods. Discontinuous bonds in accordance with the present technology are suitable for solid-state transducers, including light-emitting diodes.

BACKGROUND

[0002] Solid state transducer devices include light-emitting diodes ("LEDs"), organic light emitting diodes ("OLEDs"), and polymer light-emitting diodes ("PLEDS"). The energy efficiency and small size of solid state transducer devices has led to the proliferation of these devices in a multitude of products. Televisions, computer monitors, mobile phones, digital cameras, and other electronic devices utilize LEDs for image generation, object illumination (e.g., camera flashes) and/or backlighting. LEDs are also used for signage, indoor and outdoor lighting, traffic lights, and other types of illumination. Improved fabrication techniques for these semiconductor devices have both lowered device cost and increased device efficiency.

[0003] Manufacturing processes for solid-state transducer devices and other semiconductor devices often include the use of multiple substrates. In one conventional method, semiconductor fabrication techniques are used to construct LEDs on a device substrate. A bonding material is then used to bond the device substrate to a carrier substrate, with the LEDs sandwiched therebetween. The device substrate can then be removed and the carrier substrate with the attached LEDs can be further processed to singulate individual LEDs.

[0004] Although this fabrication method can yield reasonable results, the bonding process can produce significant stresses on the substrates and the attached LEDs. These stresses can flex and bow the substrates causing, warping, delamination or other separations, and/or can lead to misalignments during the singulation process. Additionally, singulating the LEDs through both the bonding material and the substrate can create significant stresses and complicate the singulation process. Accordingly, there is a need for a solid-state transducer device and a method of fabrication that can avoid these limitations.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Figure 1 is a partially schematic, cross-sectional diagram of a portion of a device assembly configured in accordance with an embodiment of the present technology.

[0006] Figure 2 is a partially schematic, cross-sectional diagram of a portion of a carrier assembly configured in accordance with an embodiment of the present technology.

[0007] Figure 3 is a partially schematic, cross-sectional diagram of the device assembly of Figure 1 having a pattern in accordance with an embodiment of the present technology.

[0008] Figure 4 is a partially schematic, top plan view of the device assembly of Figure 3.

[0009] Figure 5 is a partially schematic, cross-sectional diagram of a patterned carrier assembly configured in accordance with an embodiment of the present technology.

[0010] Figure 6 is a partially schematic, top plan view of the carrier assembly of Figure 5.

[0011] Figure 7 is a partially schematic, cross-sectional diagram of the device assembly and the carrier assembly of Figures 3 and 5 positioned in alignment prior to bonding.

[0012] Figure 8 is a partially schematic, cross-sectional diagram of a bonded assembly configured in accordance with an embodiment of the present technology.

[0013] Figure 9 is a partially schematic, cross-sectional diagram of the bonded assembly of Figure 8 after the device substrate has been removed in accordance with an embodiment of the present technology.

[0014] Figure 10 is a partially schematic, cross-sectional diagram of a device assembly and a carrier assembly prior to formation of a bonded assembly in accordance with an embodiment of the present technology.

[0015] Figure 11 is a partially schematic, cross-sectional diagram of a bonded assembly configured in accordance with an embodiment of the present technology.

[0016] Figure 12 is a partially schematic, cross-sectional diagram of a device assembly and a carrier assembly prior to formation of a bonded assembly in accordance with another embodiment of the present technology.

[0017] Figure 13 is a partially schematic, cross-sectional diagram of a bonded assembly configured in accordance with an embodiment of the present technology.

DETAILED DESCRIPTION

[0018] Specific details of several embodiments of wafer-level assemblies for semiconductor devices and associated systems and methods are described below. The embodiments below include solid-state transducers ("SSTs"). However, other embodiments of the presently disclosed technology may include other semiconductor devices, such as photocells, diodes, transistors, integrated circuits, etc. The term "SST" generally refers to solid-state devices that include a semiconductor material as the active medium to convert electrical energy into electromagnetic radiation in the visible, ultraviolet, infrared, and/or other spectra. For example, SST devices include solid-state light emitters (e.g., LEDs, laser diodes, etc.) and/or other sources of emission other than electrical filaments, plasmas, or gases. The term SST can also include solid-state devices that convert electromagnetic radiation into electricity. Additionally, depending upon the context in which it is used, the term "substrate" can refer to a wafer-level substrate or to a singulated device-level substrate. A person skilled in the relevant art will also understand that the technology may have additional embodiments, and that the technology may be practiced without several of the details of the embodiments described below with reference to Figures 1-13.

[0019] Figure 1 is a partially schematic, cross-sectional diagram of a portion of a wafer-level assembly, or device assembly 100 having a device substrate 102, a transducer structure 104 and a first bond metal 106 in accordance with an embodiment of the present technology. Figure 2 is a partially schematic, cross-sectional diagram of a portion of a wafer-level assembly, or carrier assembly 200, having a carrier substrate 208 and a second bond metal 206 in accordance with an embodiment of the present technology. The wafer-level assemblies of Figures 1 and 2 may be constructed using various semiconductor fabrication techniques. The device substrate 102 and the carrier substrate 208, for example, can be made from silicon, polycrystalline aluminum nitride, sapphire, and/or other suitable materials including both metals and non-metals. Additionally, the device substrate 102 and/or the carrier substrate 208 may be a composite substrate or an engineered substrate. In such embodiments, the engineered substrate may include two or more materials bonded together, and/or materials chosen or engineered to improve fabrication or assembly of the device assembly 100 or carrier assembly 200. The transducer structure 104 can be formed via a variety of processes, including metal organic chemical vapor deposition ("MOCVD"), molecular beam epitaxy ("MBE"), liquid phase epitaxy ("LPE"), and/or hydride vapor phase epitaxy ("HVPE"). In other embodiments, at least a portion of the transducer structure 104 may be formed using other suitable techniques, e.g.,

epitaxial growth techniques. The first bond metal 106 and the second bond metal 206 of Figures 1 and 2 may be composed of any of a variety of suitable metals including copper, aluminum, gold, tin, nickel, palladium, indium, and/or various alloys including combinations of these and/or other metals. In some embodiments, the first bond metal 106 and the second bond metal 206 may be composed of the same metal or alloy. In other embodiments, the first bond metal 106 and the second bond metal 206 may be composed of different metals or alloys. Furthermore, in yet other embodiments, a bonding material other than a metal may be used in place of the bond metals 106 and 206. Various semiconductor adhesives, for example, may be used as a bonding material.

[0020] Figure 3 is a partially schematic, cross-sectional diagram of the device assembly 100 of Figure 1 after having been patterned in accordance with an embodiment of the present technology. In the illustrated embodiment, the pattern formed in the device assembly 100 includes a plurality of trenches 310 formed by removing sections of the first bond metal 106 and the transducer structure 104. Figure 4 is a partially schematic, top plan view of the device assembly 100 of Figure 3. Referring to Figures 3 and 4 together, the trenches 310 can form a grid that separates the transducer structure 104 into a plurality of solid-state transducers ("SSTs") 312. The pattern of the trenches 310 and the SSTs 312 is shaped similarly to an inverted waffle shape, with sections or segments of the trenches 310 surrounding each of the SSTs 312. The trenches 310 can be formed by positioning a mask (not shown) over the areas above the SSTs 312 and etching (e.g., wet etching, dry etching, etc.) the exposed sections of the first bond metal 106 and the transducer structure 104. In other embodiments, the trenches 310 can be formed using other suitable semiconductor fabrication techniques.

[0021] Figure 5 is a partially schematic, cross-sectional diagram of a patterned carrier assembly 500 having a pattern in accordance with an embodiment of the present technology. In the illustrated embodiment, the pattern in the carrier assembly 500 includes a plurality of intermediate regions (e.g. recesses 514) separated by raised portions or projections 516. Figure 6 is a partially schematic, top plan view of the carrier assembly 500 of Figure 5. Referring to Figures 5 and 6 together, the recesses 514 and the projections 516 form a waffle pattern with the projections 516 surrounding individual recesses 514 on all sides. As will be described in further detail below, the projections 516 can form dicing streets 617 that can be used to singulate the SSTs 312. In some embodiments, the recesses 514 can be configured to have a depth of from about 5 to about 15 microns. In other embodiments, the depth of the recesses 514 may be smaller or larger than depths included in this range. The recesses 514 can be formed in a

manner similar to that used to form the trenches 310 in the device assembly 100. A mask (not shown), for example, can be used to cover the projections 516 of the carrier substrate 208, and exposed sections of the carrier substrate 208 can be etched to form the recesses 514. The recesses 514 can include blind ends 515 at least partially defined by the remaining carrier substrate 208 and/or the second bond metal 206 disposed in the recesses 514 to facilitate bonding with the device assembly 100.

[0022] Figure 7 is a partially schematic, cross-sectional diagram of the device assembly 100 of Figures 3 and 4 and the carrier assembly 500 of Figures 5 and 6 in alignment prior to bonding. In the illustrated embodiment, the inverted waffle pattern of the device assembly 100 is aligned with the waffle pattern of the carrier assembly 500, prior to bonding. In particular, the projections 516 of the carrier assembly 500 are aligned to be inserted into the trenches 310, while the SSTs 312 with attached sections of the first bond metal 106 are aligned to be inserted into the recesses 514. Optical alignment techniques and/or other semiconductor fabrication techniques can be used to align the device assembly 100 to the carrier assembly 500 in two orthogonal directions, and can be used to position the device assembly 100 and the carrier assembly 500 in parallel planes to facilitate consistent bonds between these assemblies. Additionally, the patterns of the assemblies described herein are created with suitable fabrication tolerances to allow for the assemblies to be mated. For example, the projections 516 may be slightly narrower than the trenches 310 to avoid an interference between these components.

[0023] Figure 8 is a partially schematic, cross-sectional diagram of a bonded assembly 800, including the device assembly 100 and the carrier assembly 500 of Figure 7, configured in accordance with an embodiment of the present technology. Referring to Figures 7 and 8 together, the bonded assembly 800 can be formed by bringing the device assembly 100 and the carrier assembly 500 together after alignment. When the device assembly 100 and the carrier assembly 500 are brought fully together to create the bonded assembly 800, the individual SSTs 312 of the device assembly 100 are contained at least partially within the individual recesses 514 of the carrier assembly 500. The first bond metal 106 of the device assembly 100 and the second bond metal 206 of the carrier assembly 500 combine to form a bond metal structure 818, which bonds the SST's 312 to the recesses 514. The bond metal structure 818 may be formed in a high temperature and pressure environment to facilitate bonding. The resulting bonded assembly 800 includes a discontinuous bond 820 composed of individual bond sections or segments 821 between the SSTs 312 and the bond metal structure 818 in the recesses 514. In particular embodiments, the projections 516 of the carrier assembly 500 that separate the

recesses 514 are not bonded to the device assembly 100, and each individual projection 516 represents a discontinuity between the segments 821 of the discontinuous bond 820.

[0024] Figure 9 is a partially schematic, cross-sectional diagram of the bonded assembly 800 shown in Figure 8 after the device substrate 102 (not shown in Figure 9) has been removed in accordance with an embodiment of the present technology. The device substrate 102 may be removed by various semiconductor fabrication techniques including backgrinding, etching, chemical-mechanical planarization and/or other suitable removal methods. After the device substrate 102 has been removed, the bonded assembly 800 includes individual SSTs 312 separated by projections 516. The projections 516 run across the bonded assembly 800, as shown in the overhead view of the carrier assembly 500 in Figure 6, to form the dicing streets 617. A dicing saw or other singulation tool (not shown in Figure 9) is then used to cut through the carrier substrate 208 along the dicing streets 617 to singulate the SSTs 312. Dicing the bonded assembly along the streets 617 does not require the saw to singulate through more than one material, e.g., the saw need only cut through the carrier substrate 208. Dicing through a single material can reduce the stresses on the bonded assembly 800 and can limit the potential for misalignments and defects caused by the singulation process. Additionally, the present technology further reduce stresses on the bonded assembly 800 by reducing or eliminating the need to singulate through a high stress bonding material.

[0025] Figure 10 is a partially schematic, cross-sectional diagram of the device assembly 100 of Figure 1 and a carrier assembly 1000 in alignment prior to bonding in accordance with an embodiment of the present technology. Similar to the carrier assembly 500 of Figures 5 and 6, the carrier assembly 1000 includes a plurality of recesses 1014 separated by streets or projections 1016. The recesses 1014 and the projections 1016 form a waffle pattern with the projections 1016 surrounding individual recesses 1014 on all sides. In the illustrated embodiment, the recesses 1014 in the carrier assembly 1000 may be substantially filled with the second bond metal 206 to facilitate bonding with the device assembly 100.

[0026] Figure 11 is a partially schematic, cross-sectional diagram of a bonded assembly 1100 including the device assembly 100 and the carrier assembly 1000 of Figure 10 configured in accordance with an embodiment of the present technology. Referring to Figures 10 and 11 together, after alignment, the device assembly 100 is brought together with and bonded to the carrier assembly 1000. The resulting bonded assembly 1100 includes a bond metal structure 1018 that is formed from the first bond metal 106 of the device assembly 100 and the second bond metal 206 of the carrier assembly 1000. The bond metal structure 1018 bonds the

transducer structure 104 of the device assembly 100 to the carrier substrate 208 with a discontinuous bond 1120. The discontinuous bond 1120 includes bond segments 1121 between the transducer structure 104 and the recesses 1014. The projections 1016 of the carrier assembly 1000 are not bonded to the device assembly 100. Accordingly, each individual projection 1016 represents a discontinuity between the bond segments 1121 of the discontinuous bond 1120.

[0027] Figure 12 is a partially schematic, cross-sectional diagram of the device assembly 100 of Figures 3 and 4 and the carrier assembly 200 of Figure 2 in alignment prior to bonding. As previously discussed, the trenches 310, and the SSTs 312 define an inverted waffle shape, with sections of the trenches 310 surrounding each of the SSTs 312.

[0028] Figure 13 is a partially schematic, cross-sectional diagram of a bonded assembly 1300 including the device assembly 100 and the carrier assembly 200 of Figure 12 configured in accordance with an embodiment of the present technology. As shown in Figure 13, the device assembly 100 and the carrier assembly 200 can be aligned and brought together to form the bonded assembly 1300. Bonding the device assembly 100 with the carrier assembly 200 combines the first bond metal 106 with the second bond metal 206 to form a bond metal structure 1318. Accordingly, the SSTs 312 of the device assembly 100 are bonded to the carrier assembly 200 with the bond metal structure 1318. In the illustrated bonded assembly 1300, the trenches 310 (or at least portions of the trenches 310) remain open, forming a void or gap. The bonded assembly 1300 thereby includes a discontinuous bond 1320 composed of bond segments 1321 between the SSTs 312 and the carrier assembly 200. The trenches 310 that separate the SSTs 312 represent a discontinuity between the bond segments 1321 of the discontinuous bond 1320.

[0029] Conventional semiconductor fabrication techniques typically produce significant stresses across wafers that can cause the wafers to bow or warp. This in turn can cause the wafer components to separate and/or become misaligned, potentially creating immediate or delayed defects in the components. These negative effects can be especially pronounced in larger wafers in which stresses can build up over larger distances. In contrast to the foregoing conventional techniques, the discontinuous bonds of the present disclosure decrease the mechanical stress across the bonded assemblies. As discussed above, in the bonded assembly 800, for example, the projections 516 of the carrier assembly 500 are not bonded to the device assembly 100, and the projections 516 represent discontinuities in the discontinuous bond 820. The discontinuities can decrease stress across the bonded assembly 800 and reduce or eliminate bowing and warping. The bonded assemblies 1100 and 1300 include similar stress reducing discontinuous

bonds. Accordingly, the bonded assemblies of the present disclosure can be constructed on larger substrates because the lower stresses produce smaller amounts of bowing and warping for a given size substrate. In one embodiment, for example, the bonded assemblies can be constructed on eight inch diameter substrates. These larger wafers produce economies of scale not available with smaller wafers. Although the advantages of the systems and methods of the present technology may be more pronounced with larger diameter substrates, the advantages may also be present in smaller substrates. Accordingly, in other embodiments, the bonded assemblies may be constructed on smaller diameter substrates as well as larger diameter substrates.

[0030] A further advantage of embodiments of the present technology is that the second bond metal 206 can be contained during the fabrication process. The recesses 514, for example, can contain the second bond metal 206 within the projections 516. By containing the second bond metal 206 within the recesses 514, the distribution of the second bond metal 206 can be limited to only areas where it is needed for bonding. Accordingly, the second bond metal 206 can be prevented from migrating to other areas of the carrier assembly 500, and either interfering with other components (which can cause defects, such as short circuits), or creating waste by migrating to areas not used for bonding. By reducing defects and waste, systems and methods in accordance with embodiments of the present disclosure increase the efficiency and throughput with which SSTs and/or other semiconductor devices are manufactured.

[0031] From the foregoing it will be appreciated that specific embodiments of the disclosed technology have been described herein for purposes of illustration, but that various modifications may be made without deviating from the disclosure. For example, carrier assemblies, device assemblies and bonded assemblies disclosed herein can include trenches, patterned recesses, and/or projections with different sizes and/or shapes. Rectangular recesses and SSTs, for example, may be used in some embodiments. Additionally, different materials may be used in place of those described herein, or additional components may be added or removed. For example, a bonding material may be applied to only one of either the carrier assembly or the device assembly prior to bonding. In particular embodiments the trenches surround a single SST. In other embodiments, the smallest region enclosed by the trenches can include multiple SSTs. Such a technique can be used, for example, in instances for which grouping multiple SSTs together without a bond discontinuity does not create an unacceptable warping and/or other effects, and/or instances for which the SSTs remain together as a functional unit after dicing. Moreover, while various advantages and features associated with

certain embodiments have been described above in the context of those embodiments, other embodiments may also exhibit such advantages and/or features, and not all embodiments need necessarily exhibit such advantages and/or features to fall within the scope of the technology. Accordingly, the disclosure and associated technology can encompass other embodiments not expressly shown or described herein.

CLAIMS

We claim:

1. A semiconductor device, comprising:

a first substrate;

a second substrate having a plurality of projections and a plurality of intermediate regions, with individual intermediate regions bounded by neighboring projections and having a blind end, at least one of the first and second substrates having a plurality of solid-state transducers, wherein individual solid-state transducers are disposed at least partially within corresponding intermediate regions; and

a discontinuous bond between the first substrate and the second substrate, the discontinuous bond comprising a bonding material bonded to the second substrate at the blind end of the intermediate regions, with the solid-state transducers disposed between the first substrate and the bonding material.

2. The semiconductor device of claim 1 wherein the plurality of intermediate regions and the projections form a first pattern at the second substrate, and wherein the plurality of solid-state transducers and the bonding material form a second pattern, the second pattern being the inverse of the first pattern.

3. The semiconductor device of claim 2 wherein the bonding material comprises a bonding metal, and wherein the first pattern comprises a waffle pattern and the second pattern comprises an inverted waffle pattern.

4. The semiconductor device of claim 1 wherein the plurality of solid-state transducers comprise light-emitting diodes.

5. A bonded assembly, comprising:

a first substrate carrying a transducer structure and a bonding material with the transducer structure disposed between the first substrate and the bonding material; and

a second substrate, the second substrate having a series of projections forming a pattern, wherein the first substrate is bonded to the second substrate with a discontinuous bond in regions between the projections.

6. The bonded assembly of claim 5 wherein the discontinuous bond comprises a series of sections of the bonding material bonded to the second substrate, separated by sections of the bonding material not bonded to the second substrate.

7. The bonded assembly of claim 5 wherein the bonding material comprises a bonding metal, and wherein the transducer structure comprises a light-emitting diode.

8. A semiconductor device, comprising:

a first substrate carrying a bonding material and a plurality of solid-state transducers disposed between the first substrate and the bonding material; and

a second substrate bonded to the first substrate with a discontinuous bond, the discontinuous bond comprising a plurality of spaced-apart bond segments, with individual bond segments including a portion of the bonding material bonded to both the solid-state transducers and to the second substrate.

9. The semiconductor device of claim 8 wherein the second substrate includes projections that at least partially define a plurality of regions in the second substrate, wherein individual regions are partially occupied by the bonding material and partially occupied by one of the plurality of solid-state transducers, wherein the projections form a grid pattern of streets between neighboring solid-state transducers.

10. The semiconductor device of claim 8 wherein the individual bond segments are separated by sections of void space defined at least partially by a gap between neighboring solid-state transducers.

11. A semiconductor device, comprising:

a carrier substrate, wherein the carrier substrate includes a plurality of projections separated by intermediate regions; and

a plurality of solid-state transducers, with individual solid-state transducers disposed at least partially within corresponding intermediate regions, wherein the individual solid-state transducers are bonded to the carrier substrate with bonding material.

12. The semiconductor device of claim 11 wherein the projections and the intermediate regions form a rectilinear pattern in the carrier substrate.

13. The semiconductor device of claim 11 wherein the plurality of solid-state transducers comprise light-emitting diodes.

14. A method for fabricating a semiconductor device, the method comprising:

forming a plurality of solid-state transducers in a device substrate;

forming a plurality of recesses in a carrier substrate; and

bonding the carrier substrate to the device substrate with a discontinuous bond, wherein the discontinuous bond comprises bonding material between individual solid-state transducers and a blind end of corresponding individual recesses.

15. The method of claim 14 wherein the plurality of recesses form a first pattern and the plurality of solid-state transducers form a second pattern that is the inverse of the first pattern, and wherein bonding the carrier substrate to the device substrate includes aligning the first pattern with the second pattern and bringing the device substrate and the carrier substrate together.

16. The method of claim 15 wherein aligning the first pattern with the second pattern includes optically aligning the first pattern with the second pattern.

17. The method of claim 14, further comprising at least restricting the bonding material from flowing across the carrier substrate by confining the bonding material to the plurality of recesses.

18. The method of claim 14 wherein the individual recesses are separated by projections of the carrier substrate, and wherein the projections form streets, the method further comprising:

removing the device substrate without removing the plurality of solid-state transducers; and

dicing the carrier substrate along the streets to form a plurality of individual semiconductor devices.

19. A method for fabricating a semiconductor assembly, the method comprising:

aligning a carrier substrate having a plurality of recesses with a device substrate having a plurality of solid-state transducers;

containing a bonding material in the plurality of recesses; and

bonding the device substrate to the carrier substrate with a discontinuous bond while containing the bonding material in the plurality of recesses.

20. The method of claim 19 wherein bonding the device substrate to the carrier substrate includes optically aligning the plurality of solid-state transducers with the plurality of recesses.

21. The method of claim 19 wherein bonding the device substrate to the carrier substrate with a discontinuous bond includes:

forming individual segments of the discontinuous bond by bonding individual solid-state transducers to a blind end of a corresponding recess with the bonding material;

inserting projections of the carrier substrate into trenches, wherein the trenches surround the individual solid-state transducers, and wherein the projections at least partially define discontinuities in the discontinuous bond; and

elevating a temperature of the carrier substrate and the device substrate while containing the bonding material in the plurality of recesses.