

The present invention relates to fuses used in MOS technology integrated circuits.

Fuses are used in such circuits in order to configure them. That is to say to define, at a given moment, their functions, their components and the modes or paths of access to these components. For example, in memory cards fuses of this kind make it possible to partition an initially EPROM or EEPROM memory array into zones accessible for reading or writing and others accessible solely for reading.

Several successive configurations are sometimes necessary. They each correspond to a particular level of utilization, this utilization being more restricted, more specialised, with each new configuration. For example, three utilization levels may be defined for a smart card or memory card. The first is that obtained after the manufacture of the card and may be called the factory mode; it is the most open, the least specialised. It is characterized by few restrictions or prohibitions of access paths. The smart card may be used for various applications: telephoning, banking, etc. A first configuration is therefore performed which provides the card with specific features: for example the card in the factory mode is configured with a view to a banking application. It may then be supplied to a bank. This is an intermediate configuration. The functions and access modes have been limited, being configured to correspond to the appropriate procedures for a bank card which are recorded in the bank specifications. The bank may then program its own secret information items, such as an identification number, the account number, the operations authorized, etc., in a predetermined zone. It must then prevent any subsequent reprogramming of this zone. It thus performs a second configuration which transforms the card in the intermediate configuration to a final, user configuration. It can then be sent to the user.

This non exhaustive example of utilization clearly indicates the importance of fuses which make configuration possible and also the reliability and security characteristics which these fuses must

be provided with in order to ensure the irreversible nature of the successive, or otherwise, configurations of an integrated circuit. A function cannot be modified in any way. In practice, to quote just one example, a user must not be able to alter the secret data.

Various types of fuses which can be used in integrated circuits are known, produced for example in the form of a very thin layer of polycrystalline silicon and supplied with current by a transistor for example. When a current passes for a certain time a local heating is produced because of the very narrow cross-section of the fuse. This heating suffices to volatilise the metal: the fuse is blown. In fact it sometimes happens that the fuse does not blow. In practice such a fuse is not reliable.

The very widespread use of EPROM memories and in particular EEPROM memories in smart cards should also be noted. The necessity in practice to protect records of certain data and operations in a smart card sometimes with a voltage applied (in the reader) and sometimes with no voltage applied, has excluded the use of volatile RAM memories and non-volatile ROM memories programmable by masking during manufacture.

The lack of necessity to permanently protect records of all the operations, but in the case of some, such as the balance of the account in a banking application, only to protect them from one time of use of the memory card to another, has given a definite advantage to EEPROM memories, which are electrically erasable in the reader. The impossibility of erasing an EPROM memory at the reader location leads in practice to all the programmable memory becoming used up, which makes it necessary to change the card when the said memory has been completely programmed. Whilst this concept of a disposable card is still used, the idea of using a card which is rechargeable on site is preferred to it, in particular for simple economic reasons. An advantage of a fuse in accordance with the invention is that it can form part of such an EEPROM memory array.

In the invention a fuse is provided by using the known properties of EEPROM memory cells. In accordance with the invention the non-blown fuses are like a memory cell: they form part of the memory array. They are not different, supplementary components and the method of access to them is the same as that for access to the memory cells of the memory array. It is as a result of a programming of a memory cell that the latter will be the equivalent of a blown fuse.

In fact an object of the invention is a programmable MOS fuse comprising a tunnel oxide EEPROM memory cell in a memory array composed of similar cells, a controller of the programming/erasure voltage V_{pp} supplying, by programming a command for switching, a programming/erasure voltage V_{pp} having a gently sloping edge or a steeply sloping edge, a gently sloping edge allowing normal programming/erasure of the memory cell and a steeply sloping edge breaking down the tunnel oxide and thus putting the memory cell in an irreversible state.

The invention will be better understood and other characteristics will emerge by means of the following description, given by way of non-limiting illustration of the invention, with reference to the attached Figures in which:

- Figure 1 is a diagram in cross-section of a programmable floating gate MOS cell,
- Figure 2 is an electrical diagram corresponding to the normal programming of an EEPROM memory cell in accordance with the invention,
- Figure 3 is a block diagram of an embodiment of a generator of a programming voltage having a gently sloping or a steep edge,
- Figures 4a and 4b are timing diagrams of electrical signals corresponding to Figure 3.

Figure 1 is a diagram in cross-section of a known MOS EEPROM cell C. It comprises a source region S and a drain region D which are constituted for example by N^+ diffusions in a P substrate. It also comprises a control gate GC which covers a floating gate GF both consisting of polycrystalline silicon. The floating gate GF is surrounded

by the silicon oxide 100 which isolates it in particular from the control gate GC and from the substrate. In practice the silicon oxide behaves like a dielectric, on the one hand between the control gate GC and the floating gate GF and on the other hand between the floating gate GF and the drain D or the source S, and also the substrate. This is called capacitive coupling.

Preferably a tunnel oxide region 0 is formed adjacent to the drain D. This is a thinner region of silicon oxide adjacent to the drain which facilitates the transfer of charges between the drain D and the floating gate GF, and conversely, under the influence of an electric field. The tunnel oxide thus facilitates the programming and erasure of such a memory cell.

In practice, erasure of the cell C is performed by bringing its control gate GC to a positive high potential V_{pp} of about 20 volts, and its drain D to the electrical ground potential V_{ss} of the circuit. By capacitive coupling between the control gate GC and the floating gate GF the floating gate GF is also brought to a positive high potential of about 10 volts. An intense electric field is thus created between the floating gate and the drain D, the source S of the cell not being connected, that is to say "floating". Electrons are then stored on the floating gate GF. They induce a barrier potential which opposes the conduction of the memory cell: the threshold voltage of the cell is high, about 5 volts. It will be remembered that the threshold voltage is the minimal voltage which has to be applied to the control gate GC for the memory cell C to start to conduct.

Programming an erased EEPROM memory cell consists of causing the electrons stored on the floating gate GF to leave it: the direction of the field previously applied is reversed. Thus the drain D is brought to the potential V_{pp} and the control gate GC to the potential V_{ss} , the source S still not being connected: the stored electrons are then removed. To ensure the programming, this electric field is maintained for a sufficiently long time. While this is done, free electrons which

contribute to the electrical neutrality of the material of the floating gate are also caused to leave the floating gate. In this manner, a type of holes is made in the floating gate.

To read the memory cell C a read voltage V_1 is applied to the control gate GC and a voltage V_{cc} of about 5 volts to the drain D. V_1 is typically 1.5 volts. Lastly, a read circuit 200 (Figure 2) centred on a threshold voltage between 0 and 5 volts, and in general 2.5 volts, has its input 201 connected to the drain D at a point A. This read circuit will for example detect a "1" if the cell is programmed and a "0" if it is erased. The programmed cell in practice behaves like a closed circuit because the voltage V_1 on its control gate GC is greater than the threshold voltage by about -2 volts. The voltage at the point A falls and it is this fall which is detected by the read circuit.

The erased cell itself behaves like an open circuit, the voltage V_1 being then less than the threshold voltage by about 5 volts. The voltage at the point A does not fall.

However, programming and erasure, which are the operations for writing in the cell, are delicate operations. The tunnel oxide O is in practice fragile because of its thinness (90 Angstroms). Thus a voltage controller RG is used which calibrates the potential V_{pp} . Thus it is possible to avoid any peaks or voltage surges which could damage the oxide and thus reduce the number of possible programming and erasure operations. In practice a slow switching of the potential V_{pp} is also provided: the rise time is typically about 2ms. These programming/erasure conditions make it possible to perform about 100,000 programming/erasure operations before the cell is declared "dead".

In the invention the voltage controller RG, when it receives a command for switching C_{com} , supplies a signal V_{pp} which has either a gently sloping edge f_l ($\approx 2ms$) or a steeply sloping edge f_r (100 μs) and which is well regulated (no voltage surges). Such a signal will then blow the tunnel oxide O, that is to say will break through it thus short circuiting the drain D and the floating gate GF without damaging the

remainder of the cell or the associated circuitry. This break down is caused by the sudden application (steep edge) of the voltage V_{pp} .

The short circuit created between the drain D and the floating gate GF is irreversible. It is not possible in any way to reconstitute the tunnel oxide O: it is an irreversible state. But what is this state?

The short circuit between the drain D and the floating gate GF no longer allows storage of positive or negative charges on the said floating gate GF. The corresponding threshold voltage is then substantially zero.

Reading of the "blown" cell with a circuit such as is described hereinabove then gives a logic output "1" which is a state called programmed. In practice in the read circuit the read voltage V_I applied to the gate is about 1.5 volts: V_I is greater than the zero threshold voltage of the blown cell. The blown cell C will then conduct and the voltage at the point A will fall (Figure 2).

With another type of read circuit, using for example a value of V_I of about -1 volts, a cell said to be erased (which does not conduct) is then read.

In all cases an irreversible state is obtained which is "distinguishable" by reading from a preceding state: a fuse having a tunnel oxide which can be broken down is provided which is programmable by a switching command for Ccom producing a gently sloping edge or a steeply sloping edge. It is therefore programmable at any time in an application.

Furthermore, the fuse has two operational states. Before being blown it is an undifferentiated memory cell in a memory array (not shown). This makes it possible to validate the circuitry associated with the cell (access, decoding, programming/erasure, reading) and to increase the reliability of such a fuse in accordance with the invention. In practice conventional fuses have an initial state and an irreversible

final state. In the invention, first of all a fuse has an initial state and a reversible final state, then, as a result of programming (or switching) by a steeply sloping edge, an irreversible final state. It can thus be said that cells are available in the memory array which may exist in three states: erased, programmed or blown. The features of electrical programming and erasure of an EEPROM memory cell have thus been combined with the irreversibility of a fuse to provide a very reliable fuse which is programmable as and when required.

In practice it is possible that a single steeply sloping edge will not suffice to blow the fuse in accordance with the invention. It then suffices to reread the state of the cell and to reapply a steeply sloping edge if the cell is not blown. This of course assumes that this starts from the different state to that in which the cell exists after blowing, this state being that read by the read circuit. In the example with a read voltage V_1 of 1.5 volts, the cell must be erased before proceeding to the switching on of the steeply sloping edge.

It is possible to have up to 10 successive applications of a steeply sloping edge of the signal V_{pp} , or 10 loops for example of programming followed by reading. This "blowing algorithm" may easily be generated by a microprocessor. Or, of course, 10 successive steeply sloping edges may be applied systematically using a counter for example.

Figures 3, 4a and 4b illustrate an example of a voltage controller RG which makes it possible to obtain, by programming, a signal V_{pp} having a gently sloping edge or a steeply sloping edge in accordance with the invention. It has been mentioned that the programming/erasure circuits use a controller of the voltage V_{pp} to regulate this signal correctly. In a known manner this controller is supplied by an external voltage or preferably by a voltage booster (charge pump) which receives the voltage V_{cc} of the circuit (≈ 5 volts) and generates a higher voltage V_H rapidly (for example $20 \mu s$) and which is integrated in the circuit. The voltage V_H supplied by the charge pump is equal to or greater than the voltage V_{pp} . For example it may be 25 volts.

Conventionally the first stage of a controller is constituted by a chain of transistors connected as diodes (gate and drain short circuited) so that each establishes between its source and its drain a voltage equal to its threshold voltage. Depending on the technology employed, the threshold voltage varies and the number of transistors in series makes it possible to define the controlled voltage at the output of the controller.

For example, with transistors mounted in series as diodes having a threshold voltage of about 1 volt, 20 transistors are required to establish a controlled voltage V_{pp} of about 20 volts.

At the output of the first stage there is an analog circuit which constitutes the second stage of the controller.

This circuit receives the output voltage of the first stage and supplies a voltage in the form of a ramp increasing from 0 to V_{pp} volts.

The slope of the increase is about 1 to 2 milliseconds to rise to V_{pp} : this is the signal V_{pp} having a gently sloping edge.

To obtain a steeply sloping edge, it then suffices to use a second analog circuit the parameters of which are calculated to supply a slope requiring about 100 μs to go from 0 to V_{pp} .

It then suffices to operate a switch by the command for switching C_{com} in order to select a steeply sloping edge or a gently sloping edge. However, these analog circuits are complex (typically several tens of transistors), bulky (they use capacitors) and they are very dependent on their technological construction and on temperature.

Consequently a preferred alternative embodiment is proposed which comprises a digital means of command. The controller RG (Figure 3) comprises in a first stage a set of k transistors in series, each transistor being mounted to act as a diode, having its gate connected to its drain, so that between the source and the drain of each transistor a

voltage equal to the threshold voltage of this transistor is generated. Consequently at the terminals of the set of k transistors in series, after the voltage at the terminals of the said set puts them into a saturation regime, a voltage equal to the sum of the threshold voltages of all the transistors is generated, that is to say a voltage equal to k times the threshold voltage of the transistors if they all have the same threshold voltage V_{tp} .

In the example shown, the set comprises k P channel transistors in series in the case of an embodiment on a P type substrate, each of the transistors being formed in an island separated from the others to have a more stable threshold voltage (suppression of the effect called "substrate effect" on the threshold voltage). One end of the set of P type transistors in series is connected to the ground potential V_{ss} . The other end is connected to the output voltage V_H of the charge pump PC.

The controller, constituted in this manner by a set of transistors mounted in series between the voltage V_H and the ground V_{ss} , limits the voltage V_H to a voltage kV_{tp} . The number k of transistors necessary is chosen in dependence on the value of voltage V_{pp} desired and in dependence on the threshold voltages of the P type transistors.

Optionally k P type transistors and k' N type transistors may be used. However the stability of the controlled voltage would not be as good.

In a numerical example, the threshold voltage V_{tp} is about 1 volt. About twenty P type transistors are required to have a voltage V_{pp} of about twenty volts.

The rise time of the signal V_{pp} is obtained by digital control of these transistors. This digital control utilizes a counter CT to supply a rise time depending on the desired profile. This is the second stage of the controller.

The counter CT comprises k outputs S1, S2, S3, ...Sk. The counter is controlled by a clock H1.

The outputs of the clock control switches I1, I2, ...Ik able to short circuit or to open the short circuit of each of the transistors in the set of k transistors in series in the controller. The said counter operates in counting and in counting down mode, the selection of the direction of counting being controlled by the command for switching of the controller Ccom.

When the gently sloping edge is selected by Ccom, and preferably the gently sloping edge is selected when the controller is switched on, the counter operates in counting mode. Thus the output S1 makes it possible to short circuit the P type transistor closest to Vpp, the output of S2 the following one, and so on, the output Sk making it possible to short circuit the P type transistor connected to ground. The logic levels present on the outputs S1, S2, ...Sk are between zero volts and Vpp, the counter consequently being supplied by the voltage Vpp produced.

Counting is triggered after a command for production of a voltage Vpp, this command being supplied for example by a write signal W of the memory cell. The outputs of the counter are initially all in a logic state such that they short circuit all the transistors. In the example shown, the switches controlled by the outputs of the counter are N channel transistors and they are short circuited by a high level voltage on their gates. It will be assumed, therefore, that at the start all the outputs of the counter provide a high logic state.

The signal W then authorizes counting by the counter. The counter is not a binary counter (or if it is it is followed by a decoder). It generates on the first pulse of the clock a low state on the output S1, then, on the second pulse of the clock, a low state on the output S2 without changing the low state of S1, and in a similar manner it then generates a low state on each of the successive outputs up to Sk whilst leaving each time the preceding output in the state into which it was put

on the preceding clock pulse. In twenty clock pulses, in an example where there are twenty P type transistors, the outputs have all changed to the low logic state and the short circuits of all the transistors of the controller are all opened.

When the last output S_k changes to the low logic state it prevents counting (for example by blocking the clock H1) so that the controller remains in this configuration until the end of the command for production of V_{pp} or even, in practice, until there is a new command for the production of V_{pp} (new write signal W).

As a result, even if the charge pump produces a high voltage very rapidly, which is the case in practice ($\approx 20\mu s$ for example), the controller will limit this voltage to a value which will be zero, then V_{tp} , then $2V_{tp}$, etc. up to kV_{tp} , in other words the final voltage V_{pp} desired.

The voltage V_{pp} thus limited by the variable threshold regulator will increase in steps at the frequency of the clock H1 (which can be easily be controlled exactly).

When the steeply sloping edge is selected by Ccom the counter operates in counting down mode. Consequently the outputs S_1 to S_k open the short circuits of all the P type transistors simultaneously.

Counting down also is triggered by a command for the production of a voltage V_{pp} which is supplied, in the example, by the signal W. Initially all the outputs of the counter are in a high logic state: they short circuit all the N type transistors (switches $I_1, \dots, I_k$).

The signal W then authorizes counting down by the counter.

Counting down is stopped after the first pulse of the clock H1. In practice, the first counting down operation causes all the outputs of the counter to change to the low logic level. It has been arranged that when

the last output S_k changes to the low logic state it blocks the clock H_1 : it thus stops the counting down. In this manner the controller remains in this configuration until the end of the command for production of V_{pp} or even, in practice, until there is a new command for the production of V_{pp} (new write signal W). It would be possible to prevent the counting down on the change to the low logic state of any one of the outputs S_1 to S_k because they all change state simultaneously.

Figures 4a and 4b show this increase in the voltage limit of the controller (and consequently the increase in V_{pp}) in relation to the successive (Figure 4a) or simultaneous (Figure 4b) switching of the logic states of the outputs S_1 to S_k of the counter CT .

If there are 20 P channel transistors having threshold voltages of about 1 volt, the counter will have 20 outputs. During counting, to obtain a voltage changing from 0 to about 20 volts in a little less than 2 milliseconds it is necessary to use a 10 kilohertz clock H_1 . During counting down the rise time, which is equal to one pulse of the clock, will then be 100 μ s.

More generally, in order to obtain a slow rise time T_m in the case of a counter comprising k outputs and a controller having k possible voltage limits, a clock with a frequency of k/T_m will be used. The frequency may be between $k/2$ and k kilohertz for a rise time of 1 to 2 milliseconds. The rapid rise time is T_m/k .

Experience shows that the steps in the voltage V_{pp} obtained on counting (gently sloping edge) are not very inconvenient. On the one hand they only occur during the transitory rising phase of V_{pp} . On the other hand the numerous resistances and parasitic capacitances of the circuits which V_{pp} is designed to supply very greatly attenuate these steps.

Furthermore, a controller RG having a digital control of the kind described makes it possible to use for blowing a fuse a steep edged voltage V_{pp} which has a value greater than that having a gently sloping

edge. For example, the steep edged voltage V_{pp} may be greater by several V_{tp} than the voltage V_{pp} having a gently sloping edge. It suffices in practice to have available $k+n$ P type transistors, mounted in series as diodes, in the first stage and a counter having $n+k$ outputs (S_1 to S_{k+n}). During counting (production of a gently sloping edge) only the short circuits of the first k transistors are successively opened in the manner described hereinabove. In contrast, during counting down the short circuits of the $n+k$ transistors are all opened simultaneously. In the first case V_{pp} equals kV_{tp} and in the second case V_{pp} equals $(k+n)V_{tp}$.

If k equals 20 and n equals 5, then for example the voltage V_{pp} is equal to about 20 volts for programming and erasure and equal to about 25 volts for fusing of the memory cell. This is possible provided always that the value of V_H supplied at the input of the controller is at least equal to the required value, 25 volts in this case. In fact the output voltage which the controller can supply is only equal to V_H at most.

A greater fusing voltage of this kind combined with a steep edge make it possible to improve the break down of the tunnel oxide. The stopping of counting and of counting down may always occur at the change to the low logic state of the output S_k of the counter because for the counting down the states of the outputs S_1 to S_{k+n} are all generated simultaneously.

Similarly, a counter for which a value may be initialised, for example by programming a register of the counter in a controller in accordance with the invention, is within the field of the invention. This facility makes it possible for example to select by programming the counter the value of V_{pp} for causing fusing. For example this value may be equal to kV_{tp} or $(k+1)V_{tp}$, etc. and may be initialised by programming in the counter. For example the value for fusing may be determined by the blowing algorithm.

CLAIMS

1. A programmable MOS fuse comprising a tunnel oxide (O) EEPROM memory cell (C) in a memory array composed of similar cells, a controller (RG) of the programming/erasure voltage (V_{pp}) supplying, by programming a command for switching (Ccom), a programming/erasure voltage (V_{pp}) having a gently sloping edge (fl) or a steeply sloping edge (fr), a gently sloping edge allowing a normal programming/erasure of the memory cell (C) and a steeply sloping edge breaking down the tunnel oxide and thus putting the memory cell in an irreversible state.

2. A fuse as claimed in claim 1, characterized in that the voltage controller (RG) comprises a set of transistors in series, connected to act as diodes and establishing between the source and the drain a voltage equal to their threshold voltage (V_{tp}) and in that a digital control means comprises a counter (CT) adapted to generate a defined logic state on each of its outputs, either successively in the case of a command for switching (Ccom) when a gently sloping edge (fl) is concerned or simultaneously in the case of a command for switching when a steeply sloping edge (fr) is concerned, and a means (I_1 to I_k) controlled by the outputs of the counter initially to short circuit the transistors mounted to act as diodes then to open the short circuits, either progressively one after the other as the counting proceeds in order to produce a gently sloping edge, or all at the same time by counting down in order to produce a steeply sloping edge.

3. A fuse as claimed in claim 2, characterized in that the counter is a circuit comprising k outputs which on each pulse of the clock during counting generates a defined logic level on a new output whilst leaving, each time, the level established on the preceding output, and which during counting down on each pulse of the clock generates a defined logic level on all the outputs, and in that a means is provided for stopping the counting and the counting down when the last output has been set at the defined level.



4. A fuse as claimed in claim 2, characterized in that the counter is a circuit comprising $k+n$ outputs which, during counting, on each pulse of the clock generates a defined logic level on a new output, one after the other, on the k first outputs ($S_1, \dots S_k$) which have the order numbers 1 to k , whilst leaving each time the level established on the preceding output, and which, during counting down, on each pulse of the clock generates a defined logic level on all the $k+n$ outputs (S_1 to S_{k+n}), and in that a means is provided for stopping the counting and the counting down when the output of order k has been set at the defined level.

