CLAIMS

1. A voltage level shifter, comprising: a first NOR gate having a first input configured to receive a first input signal in a first power domain, a second input configured to receive an enable signal in a second power domain, a third input, and an output; and a second NOR gate having a first input configured to receive a second input signal in the first power domain, a second input configured to receive the enable signal in the second power domain, a third input coupled to the output of the first NOR gate, and an output coupled to the third input of the first NOR gate; wherein the first and second NOR gates are powered by a supply voltage of the second power domain.

2. The voltage level shifter of claim 1, wherein each of the first and second input signals has a voltage range approximately equal to a first voltage range, the enable signal has a voltage range approximately equal to a second voltage range, and the second voltage range is greater than the first voltage range.

3. The voltage level shifter of claim 2, wherein the output of each of the first and second NOR gates has a voltage range approximately equal to the second voltage range.

4. The voltage level shifter of claim 1, wherein the first and second input signals are complementary.

5. The voltage level shifter of claim 1, wherein the first NOR gate comprises: first, second and third p-type metal-oxide-semiconductor (PMOS) transistors coupled in series between the supply voltage of the second power domain and the output of the first NOR gate; and first, second and third n-type metal-oxide-semiconductor (NMOS) transistors coupled in parallel between the output of the first NOR gate and a ground; wherein each of the first, second and third inputs of the first NOR gate is coupled to a gate of a respective one of the first, second and third PMOS transistors, and each of the first, second and third inputs of the first NOR gate is coupled to a gate of a respective one of the first, second and third NMOS transistors.

6. The voltage level shifter of claim 1, wherein the first input of the first NOR gate is coupled to a buffer in the first power domain.

7. The voltage level shifter of claim 1, wherein the first and second NOR gates are configured to output logic zero at the outputs of the first and second NOR gate when the enable signal is logic

one, and to level shift the first and second input signals from the first power domain to the second power domain when the enable signal is logic zero.

8. A method for performing voltage level shifting using a voltage level shifter, the voltage level shifter comprising first and second cross-coupled NOR gates, the method comprising: inputting a first input signal in a first power domain to the first NOR gate; inputting a second input signal in the first power domain to the second NOR gate; and inputting an enable signal in a second power domain to the first and second NOR gates to enable the voltage level shifter.

9. The method of claim 8, wherein each of the first and second input signals has a voltage range approximately equal to a first voltage range, the enable signal has a voltage range approximately equal to a second voltage range, and the second voltage range is greater than the first voltage range.

10. The method of claim 9, wherein an output of each of the first and second NOR gates has a voltage range approximately equal to the second voltage range.

11. The method of claim 8, wherein the first and second NOR gates are powered by a supply voltage of the second power domain.

12. The method of claim 8, wherein inputting the enable signal in the second power domain to the first and second NOR gates to enable the voltage level shifter comprises transitioning the enable signal from logic one to logic zero.

13. The method of claim 12, wherein each of the first and second input signals has a voltage range approximately equal to a first voltage range, the enable signal has a voltage range approximately equal to a second voltage range, and the second voltage range is greater than the first voltage range.

14. An interface, comprising: a first buffer in a first power domain; and a voltage level shifter, comprising: a first NOR gate having a first input configured to receive a first input signal from the first buffer in the first power domain, a second input configured to receive an enable signal in a second power domain, a third input, and an output; and a second NOR gate having a first input configured to receive a second input signal in the first power domain, a second input configured to receive the enable signal in the second power domain, a third input coupled to the output of

the first NOR gate, and an output coupled to the third input of the first NOR gate; wherein the first and second NOR gates are powered by a supply voltage of the second power domain.

15. The interface of claim 14, further comprises a second buffer in the second power domain, wherein the output of one of the first and second NOR gates is coupled to the second buffer.

16. The interface of claim 14, wherein each of the first and second input signals has a voltage range approximately equal to a first voltage range, the enable signal has a voltage range approximately equal to a second voltage range, and the second voltage range is greater than the first voltage range.

17. The interface of claim 16, wherein the output of each of the first and second NOR gates has a voltage range approximately equal to the second voltage range.

18. The interface of claim 14, wherein the first and second input signals are complementary.

19. The interface of claim 14, wherein the first NOR gate comprises: first, second and third p-type metal-oxide-semiconductor (PMOS) transistors coupled in series between the supply voltage of the second power domain and the output of the first NOR gate; and first, second and third n-type metal-oxide-semiconductor (NMOS) transistors coupled in parallel between the output of the first NOR gate and a ground; wherein each of the first, second and third inputs of the first NOR gate is coupled to a gate of a respective one of the first, second and third PMOS transistors, and each of the first, second and third inputs of the first NOR gate is coupled to a gate of a respective one of the first, second and third NMOS transistors.

20. The interface of claim 14, wherein the first and second NOR gates are configured to output logic zero at the outputs of the first and second NOR gate when the enable signal is logic one, and to level shift the first and second input signals from the first power domain to the second power domain when the enable signal is logic zero.

21. The interface of claim 14, further including a decoder configured to receive an address signal, to set the enable signal to logic zero if the address signal addresses the first buffer, and to set the enable signal to logic one if the address signal does not address the first buffer.

22. The interface of claim 21, wherein each of the first and second input signals has a voltage range approximately equal to a first voltage range, the enable signal has a voltage range approximately equal to a second voltage range, and the second voltage range is greater than the first voltage range.