

Description

The invention relates to an arrangement for protecting a television apparatus from a power supply fault, such as excessive ultor voltage which may produce x-rays.

GB-A-2103029 discloses a high voltage hold-down circuit which is used in a television receiver or display and which derives high voltage potential from horizontal flyback pulses, and which provides horizontal rate signals to the horizontal deflection circuit via a high frequency countdown circuit. The hold-down circuit operates by changing the divider modulus of the countdown circuit during an over-voltage condition which reduces the amplitude of the flyback pulses and consequently reduces the high voltage.

A typical deflection circuit in a television receiver includes an output stage that generates a deflection current in a deflection winding and that generates retrace pulses used for generating an ultor voltage. The output stage is controlled by a horizontal rate switching control signal.

Timing of the deflection current produced by the horizontal deflection circuit output stage may vary in a manner dependent upon loading of the ultor voltage source. For example, such loading may be dependent upon the brightness of the image being displayed on a kinescope of the receiver. Variation in such loading causes, for example, a corresponding variation in a delay of the horizontal retrace pulses and of the deflection current. Furthermore, disadvantageously, it may cause a distortion of the image being displayed.

A typical deflection circuit includes a dual feedback loop arrangement that is used for preventing the occurrence of the variation in the delay of the deflection current relative to, for example, a horizontal synchronizing signal. In such arrangement, a horizontal oscillator generates a signal at, for example, a frequency greater than the horizontal frequency. The oscillator generated signal is divided down in a frequency divider and a first output signal that is at or near the horizontal frequency is generated. The oscillator, frequency divider and a first phase detector are included in a phase-lock-loop circuit (PLL) that is synchronized by the horizontal synchronizing signal that is obtained, for example, from a sync separator of the television receiver.

The PLL, having a relatively long time constant, controls the oscillator to maintain the first output signal in frequency and phase synchronism with the horizontal synchronizing signal.

In order to compensate for such load dependent variations in the delay associated with the horizontal deflection circuit output stage, a phase-control-loop circuit (PCL) is used. The PCL in-

cludes a second phase detector, a first input terminal of which is coupled to the first output signal of the PLL and a second input terminal of which is coupled to the deflection circuit output stage for responding to the retrace pulse generated by the output stage. The phase detector produces a phase difference indicative signal from the signals at the first and second input terminals. A low-pass loop filter generates a control signal from the phase difference indicative signal. A phase shifting arrangement that is responsive to the control signal produces a horizontal-rate output signal having pulses at the horizontal rate and at a variable delay which makes, for example, the retrace pulses synchronous with the horizontal synchronizing signal even when variations of beam current loading occur.

The PLL may be internal to an integrated circuit (IC) such as, for example, TA 7777 that is made by Toshiba Co. (the Toshiba IC). The Toshiba IC produces, at corresponding output terminals, the first output signal at the horizontal frequency and the aforementioned second output signal at the frequency that is greater than the horizontal frequency and that is synchronized to the first output signal.

In a typical television display system, the high voltage ultor accelerating potential is applied to the final anode electrode of a picture tube to accelerate an electron beam generated at a picture tube cathode onto a phosphor screen. To ensure that the television receiver will not be operated under a fault condition at excessive ultor potential level, a high voltage protection circuit is incorporated in the television receiver circuitry. Thus, for example, the Toshiba IC includes such a high voltage protection circuit. An excessive ultor potential level, for example, will disable, in the Toshiba IC, the generation of the horizontal rate first output signal, but not of the second output signal at the frequency that is greater than the horizontal frequency.

The PCL that, in a circuit embodying the invention, may be internal to a second IC, may be constructed in such a way that it utilizes the second output signal of the PLL of the Toshiba IC that is at the frequency that is greater than the horizontal frequency for its internal operation. Utilization of the second output signal advantageously simplifies the design of the PCL. The output signal of the PCL that is synchronized to the first output signal of the PLL controls the switching timing in the deflection circuit output stage.

When the Toshiba IC is used to provide the PLL operation that was described before, the output signal of the PCL may be generated as a result of the presence of the second output signal at the greater frequency even when the first output signal, as a result of the fault condition, is disabled. Disad-

vantageously, the fault protection circuit of the Toshiba IC, by itself, will not prevent the generation of the output signal of the PCL and, hence, will not prevent the generation of the ultor voltage.

In accordance with the invention, a television apparatus power supply with a fault protection arrangement includes a source of an input signal at a frequency that is related to a deflection frequency. A fault indicative signal is generated when a fault condition occurs in the power supply. A first signal is generated at a first terminal during normal operation, having transition edges at a frequency that is related to that of the input signal. When the fault indicative signal is generated, the occurrence of the transition edges of the first signal is prevented. A second signal is generated at a second terminal during normal operation, and possibly also when the fault indicative signal occurs, at a frequency that is related to that of the input signal. A third signal is generated when a transition edge within the first signal is missing. Switching means, switching in response to the second signal and coupled to a load and to a source of input supply voltage develops an output supply voltage for the load during normal operation. The third signal prevents the occurrence of the switching operation that substantially reduces the output supply voltage when the third signal is generated.

In the Drawing:

FIGURE 1 illustrates a deflection apparatus that includes a fault protection arrangement, embodying the invention; and

FIGURES 2a-2f illustrate timing diagrams that are useful for explaining the fault protection arrangement of FIGURE 1.

Horizontal sync pulses S_H of FIGURE 1 having a period H , that in NTSC systems is 63.5 microseconds, and having a corresponding frequency f_H , are coupled, illustratively, from a conventional sync separator of a television receiver, not shown in the figure, to an input terminal 30a of a first phase detector 30. A signal O'_H that, as described later on, at steady state operation, is at the frequency f_H , is coupled via a "NAND" gate 300 and a capacitor C_c to a second input terminal 30b of phase detector 30. A phase difference indicative signal PH that is indicative of the phase difference between signal S_H and signal O_H is coupled to a frequency control input terminal 31a of a voltage controlled oscillator 31. Oscillator 31 generates an output signal O_{32H} at a frequency $32xf_H$. Signal O_{32H} is frequency divided by 32 in a frequency divider 32 to produce signal O'_H . Thus, detector 30, oscillator 31 and frequency divider 32 form a phase-lock-loop circuit (PLL) 20 that may be included in a first integrated circuit 100 and its externally located associated circuitry such as, for example, capacitor C_c . The operation of PLL 20 causes a corresponding transition edge in a

corresponding period of each of signals O'_H and O_{32H} to be in phase with that of signal S_H .

A phase-control-loop (PCL) 25, having a control section that may be internal to a second integrated circuit 200, generates a signal D_H at the frequency f_H , as described later on. Signal D_H is coupled to a horizontal driver 33 that generates a drive signal 33a that is coupled to a base electrode of a switching transistor Q_1 of, for example, a conventional horizontal output stage 99. Output stage 99 produces, in a winding 34 of a flyback transformer T_0 , a retracé pulse at a high voltage that is used, in a high voltage supply 35 for generating an ultor voltage U . Voltage U is coupled to an ultor electrode of a cathode ray tube of the television receiver, not shown in the FIGURES.

During normal operation, signal O'_H is coupled via enabled "NAND" gate 300 to form a corresponding signal O_H at a terminal 300a. PCL 25 is synchronized to signal O_H in such a way that deflection current I_y in a deflection winding L_y is maintained during normal operation in a corresponding constant phase relationship relative to signal O_H despite varying beam current loading that loads winding 34, as described in detail later on.

IC 200, that includes the control section of PCL 30, includes a flip-flop 40 having a clock receiving terminal 40a that receives signal O_{32H} that is at the frequency $32xf_H$. Flip-flop 40 generates an output signal E_{16H} that toggles, or changes states, each time a clocking edge of signal O_{32H} occurs. Signal E_{16H} is at a frequency $16xf_H$ that is one-half of the frequency of signal O_{32H} . Flip-flop 40 forms the first stage in a five-stage cascaded-coupled frequency dividing arrangement 45 that includes flip-flops 40-44. Arrangement 45 generates corresponding output signals E_{16H} , E_{8H} , E_{4H} , E_{2H} and E_H at frequencies $16xf_H$, $8xf_H$, $4xf_H$, $2xf_H$ and f_H , respectively, at corresponding output terminals of flip-flops 40-44. Signal O_H is coupled via an "AND" gate 52 to a corresponding reset pulse receiving terminal RESET of each of flip-flops 40-44 for insuring a predetermined phase relationship between each of signals E_{16H} , E_{8H} , E_{4H} , E_{2H} and E_H and of signal O_H . Each of flip-flops 40-44 assumes a FALSE state when a leading edge O_{Ha} of signal O_H occurs. A flip-flop 51 delays signal O_H by approximately one microsecond to form a delayed signal 51a that is inverted relative to signal O_H . The one microsecond delay time is caused by the relative timings between a corresponding clocking edge signal O_{32H} that is coupled to a clock receiving terminal of flip-flop 51 and a corresponding transition edge of signal O_H . Delayed signal 51a that is coupled to an input terminal 52a of "AND" gate 52 disables AND gate 52 one microsecond after leading edge O_{Ha} of signal O_H occurs. Thus, a

pulse 50 is generated on a conductor 49 when both signals 51a and O_H are simultaneously at corresponding TRUE states. Pulse 50, that has a duration of approximately one microsecond, and that is at the horizontal rate f_H , is synchronized to signal O_H .

When pulse 50 occurs, each of flip-flops 40-44 is initialized to provide the corresponding output signal at a corresponding predetermined state such as, for example, a FALSE state. Thus, each of the output signals of flip-flops 40-44 is also periodic at the frequency f_H of signal O_H or 50. If no significant phase perturbation in signals O_H and O_{32H} of PLL 20 occurs, after being initialized by signal 50, each of the corresponding output signals of flip-flops 40-44 will remain, in each subsequent period H , in a corresponding constant phase relationship with respect to signal O_H .

Signals E_{16H} , E_{8H} , E_{4H} , E_{2H} and E_H that are synchronized to signal O_H are used to provide timing signals that are required for the operation of IC 200 at corresponding predetermined instants that occur during each period H of signal O_H . The timing resolution by which each of such timing pulse is formed is determined by the period of signal O_{32H} . A signal 36 is an example of such timing pulses. Signal 36 that is used, as described later on, for operating PCL 30 is a horizontal rate signal that is produced at an output terminal 53a of a flip-flop 53.

To generate signal 36, signals E_{4H} , E_{2H} and E_H are coupled to corresponding input terminals of an "AND" gate 54, that produces a signal 54a having the TRUE state when each of such input signals is at the TRUE state simultaneously with the other ones. Signal 54a is coupled to a data input receiving terminal 53c of a flip-flop 53. Signal E_{8H} is coupled to a clock input receiving terminal 53b of flip-flop 53. Flip-flop 53 delays signal 54a by an interval having a duration that is determined by signal E_{8H} to form signal 36. Signal 36 is at the TRUE state during approximately 8 microseconds and at the FALSE state during the rest of period H . Thus, signal 36 is delayed relative to signal O_H by a predetermined delay that is determined by signals E_{8H} , E_{4H} , E_{2H} and E_H . Signal 36 is used for controlling the timing of a ramp generator 37 of IC 200 that is used by PCL 25, as described below.

Ramp generator 37 generates a sawtooth signal 37a that is coupled to an input terminal 38a of a voltage comparator 38. Generator 37 includes a current source I_{cs} that is coupled to a capacitor C_{37} that is, for example, located externally to IC 200. A switch 37b of generator 37 is coupled across capacitor C_{37} for discharging capacitor C_{37} and for maintaining, afterward, sawtooth signal 37a across capacitor C_{37} at a constant level as long as horizontal rate control signal 36 is at the TRUE state.

When signal 36 is at the FALSE state, current source I_{cs} charges capacitor C_{37} to form an upramping portion 37c of signal 37a.

Signal O_H is also coupled via a flip-flop 39 to an input terminal 57a of a second phase detector 57. Flip-flop 39 is clocked by signal E_{8H} to provide a delayed signal 39a that is delayed relative to signal O_H by approximately 4 microseconds. The purpose of the 4 microsecond delay is to compensate for various delays in PLL 25. A signal F_H , developed in a winding 136 of flyback transformer T0, is coupled via a delay and pulse shaping network 58 to a second input terminal 57b of second phase detector 57. Signal F_H is indicative of the phase of deflection current i_y in deflection winding L_y . An output signal 59 of second phase detector 57 that is indicative of the phase difference between signal 39a and signal F_H is coupled via a low-pass filter 66 to form a phase control signal 66a at a second input terminal 38b of comparator 38.

When, during a given period H , ramping portion 37b of signal 37a becomes greater than signal 66a at terminal 38b of comparator 38, comparator 38 generates a transition edge of a signal 60 that is coupled to a trigger receiving input terminal 61a of a one-shot flip-flop 61. Consequently, flip-flop 61 generates a pulse D_{Ha} having, illustratively, a constant duration. Pulse D_{Ha} is coupled, during normal operation, via a transistor Q2 to form signal D_H . Signal D_H at the collector of transistor Q2 is coupled to horizontal driver 33. Pulse D_{Ha} of signal D_H causes transistor Q1 to be conductive. During normal operation, pulse D_{Ha} occurs, relative to signal O_H , after an interval having a variable duration that is controllable in accordance with phase control signal 66a of filter 66. A change in the ultor loading at a terminal 35a of high voltage supply 35 that tends to cause a change in the phase of signal F_H , will cause a corresponding change in the delay of signal D_H in a negative feedback manner that will maintain constant the phase of signal F_H and that of deflection current i_y relative to signal O_H , despite varying ultor loading.

IC 100 includes a well known high voltage protection circuit 301 responsive to a signal OV that is proportional to ultor voltage U , that prevents signal O_H from changing states when a fault condition occurs. The fault condition occurs, for example, when ultor voltage U exceeds a predetermined permitted level. When such fault condition occurs, circuit 301 generates an inhibit signal 301a. Signal 301a that is coupled to an input terminal of "NAND" gate 300 causes signal O_H to remain at a disabled or TRUE state as long as signal 301a is generated. Therefore, signal transitions in signal O_H are prevented when the fault condition occurs.

On the other hand, signal O_{32H} is generated

even when the fault condition occurs. As a result of the operation of frequency dividing arrangement 45, ramp generator 37, comparator 38 and flip-flop 61, pulses D_{Ha} will be generated at an output terminal 61a of one shot flip-flop 61 even when signal O_H is disabled. Pulse D_{Ha} will continue to be generated because, when signal O_H remains at the TRUE state indefinitely, signal 66a of low-pass-filter 66a is less positive than the peak of signal 37a that will enable the generation of pulses D_{Ha} .

Embodying an aspect of the invention, pulses D_{Ha} that are coupled to the base electrode of transistor Q2 through a resistor 302 are prevented from causing the generation of signal D_H , when ultor voltage U exceeded the predetermined permitted level. In carrying out this feature of the embodiment, a flip-flop 303 is used for detecting the presence of pulses in signal O_H . When signal O_H is at the disabled state because of, for example, the disabling operation of protection circuit 301, flip-flop 303, as described below, maintains transistor Q2 at a nonconductive state as long as, for example, generation of signal transitions in signal O_H are prevented. Consequently, the generation of signal D_H and of ultor voltage U are, advantageously, also prevented.

FIGURES 2a-2f illustrate timing diagrams that are useful in explaining the operation of a protection arrangement 333 that includes flip-flop 303 and transistor Q3 of FIGURE 1. Arrangement 333 maintains transistor Q2 nonconductive as long as signal transitions in signal O_H are prevented. Similar numbers and symbols in FIGURES 1 and 2a-2f indicate similar items or functions.

Flip-flop 303 of FIGURE 1, that is of the RESET-SET (R-S) type, has a terminal 303b that is coupled to a signal 306a. Signal 306a is generated by an "AND" gate 306, an "AND" gate 305 and "AND" gate 54 when all of signals E_H , E_{2H} , E_{4H} , E_{8H} and E_{16H} are, each, at a corresponding TRUE state. Thus, signal 306a of FIGURE 2c is generated during an interval t_2 - t_3 of signal O_{32H} of FIGURE 2a that, in normal operation, occurs immediately prior to leading edge O_{Ha} of signal O_H of FIGURE 2b. As a result of signal 306a of FIGURE 1, flip-flop 303 is set at time t_2 of FIGURE 2c, causing an output signal 303a to be generated at a TRUE state immediately after time t_2 of FIGURE 2e.

Pulse 50 that, as described before, initializes arrangement 45, is also coupled to a reset terminal 303c of flip-flop 303. During normal operation, pulse 50 of FIGURE 2d occurs, at time t_3 , immediately after edge O_{Ha} of FIGURE 2b at time t_3 . Consequently, during normal operation, flip-flop 303 of FIGURE 1 is reset and signal 303a of FIGURE 2e returns to the FALSE state immediately after time t_3 .

During normal operation, pulse D_{Ha} has a fall-

ing edge at a time t_1 of FIGURE 2f, that occurs approximately 5 microseconds prior to time t_2 of FIGURE 2e. Time t_2 occurs, as described before, when signal 303a of flip-flop 303 of FIGURE 1 changes states. Pulse D_{Ha} has a rising edge at a time t_4 of FIGURE 2f, that occurs approximately 18 microseconds after time t_3 of FIGURE 2e. Thus, during normal operation, the duration of pulse D_{Ha} of FIGURE 2f overlaps that of signal 303a of FIGURE 2e.

At its TRUE state, signal 303a, that is coupled to the base electrode of a transistor Q3 of FIGURE 1, causes transistor Q3 to operate as a conductive switch. When conductive, transistor Q3 forms a low impedance between the base electrode of transistor Q2 and ground that maintains transistor Q2 nonconductive.

During normal operation, pulse D_{Ha} of FIGURE 2f maintains transistor Q2 of FIGURE 1 nonconductive throughout interval t_1 - t_4 of FIGURE 2f. At time t_4 , pulse D_{Ha} goes high, tending to render transistor Q2 conductive. As the output of flip-flop 303 is FALSE at this time, transistor Q3 is non-conductive and the voltage at the base of transistor Q2 is permitted to rise under the influence of pulse D_{Ha} . Thus transistor Q2 becomes conductive. This causes D_H at the collector of Q2 to become LOW, and the horizontal driver transistor is turned off. Through the action of transformer T1 of the driver 33, transistor Q1 is thus turned on at time t_4 . Similarly, at time t_1 , D_{Ha} goes LOW, turning transistor Q2 off, and D_H goes HIGH turning the horizontal driver transistor on. Through the action of transformer T1 of driver 33, transistor Q1 is consequently turned off at time t_1 . From time t_2 to t_3 , signal 303a is high, and transistor Q3 is on, holding transistor Q2 off, but during this period, signal D_{Ha} would also hold transistor Q2 off anyway. Consequently, during normal operation, signal 303a of FIGURE 1 has no effect on the conduction of transistors Q2 and Q1.

When, as a result of excessive ultor voltage, for example, signal O_H remains indefinitely at the TRUE state, signal 51a of flip-flop 51 prevents the generation of pulse 50 of FIGURE 2d at the TRUE state, as shown by the dashed line. Flip-flop 303 is not reset. Consequently, signal 303a of FIGURE 2e remains, after the fault condition occurs, at the TRUE state for an indefinite duration, as shown by the dashed line in FIGURE 2e.

When the fault condition occurs, signal 303a that remains at the TRUE state indefinitely maintains transistor Q3 conductive, and thus transistor Q2 non-conductive. Thus, when pulse D_{Ha} rises at time t_4 , transistor Q2 is nevertheless held non-conductive by the conduction of transistor Q3, and pulse D_H is replaced by a constant high level input to driver 33. Thus the horizontal driver transistor

does not turn off at time t_4 and transistor Q1 is not turned on. Therefore, in the fault condition, transistor Q1 remains in cutoff even after time t_4 and is evented from performing its switching operation. Therefore, ultor voltage U becomes zero.

Thus signal 303a of flip-flop 303 disables high voltage supply 35 when, as a result of the fault condition, high voltage protection circuit 301 prevents the generation of transition edges in signal O_H .

Claims

1. A television apparatus having a power supply with a fault protection arrangement, comprising:

a source of an input signal (S_H) at a frequency (f_H) that is related to a deflection frequency;

means (301) for generation of a fault indicative signal (301a) when a fault condition occurs in said power supply;

means (31,32,300) responsive to said input signal (S_H) for generating a first signal (O_H) at a first terminal (300a) during normal operation having transition edges at a frequency that is related to that of said input signal (S_H) such that when said fault indicative signal (301a) is generated, the occurrence of said transition edges of said first signal (O_H) is prevented, and for generating a second signal (O_{32H}) at a second terminal (40a), at least during normal operation, at a frequency ($32f_H$) that is related to that of said input signal (S_H);

a source of input supply voltage ($B+$);

a load (35); and

switching means (Q1), switching in response to said second signal (O_{32H}) and coupled to said load (35) and to said source of input supply voltage ($B+$) for developing an output supply voltage (at 34) for said load (35) during normal operation;

characterized by

means (303) for detecting a missing edge of said first signal (O_H) for generating a third signal (303a) when a transition edge within said first signal (O_H) is missing; and

means (Q3) responsive to said third signal (303a) and coupled to said switching means (Q1) for generating a signal (V_{BQ2}) that prevents the occurrence of said switching operation in order to substantially reduce said output supply voltage (at 34) when said third signal (303a) is generated.

2. An apparatus according to Claim 1 characterized in that said first signal (O_H) is at a frequency (f_H) that is related to a horizontal frequency

and wherein said second signal (O_{32H}) is at a higher frequency than that of said first signal (O_H).

3. An apparatus according to Claim 1 or Claim 2 characterized by a deflection winding (L_Y) that forms with said switching means (Q1) a deflection circuit output stage (99).

4. An apparatus according to Claim 3 characterized in that said load (35) coupled to said switching means (Q1) comprises means for generating an ultor voltage, wherein said fault indicative signal generating means (301) generates said fault indicative signal (301a) when said ultor voltage exceeds a predetermined level so as to prevent subsequent generation of said ultor voltage.

5. An apparatus according to any one of the preceding claims characterized in that said third signal (303a) remains indefinitely at a first state when said fault indicative signal (301a) occurs to prevent the generation of said first signal (O_H), and wherein said third signal (303a) is coupled in a signal path that is between said switching means (Q1) and said second signal (O_{32H}) for decoupling said second signal (O_{32H}) from said switching means (Q1).

6. An apparatus according to any one of Claims 1 to 4 characterized in that, during normal operation, said third signal (303a) changes alternately between a first and a second state in a manner that maintains said switching operation in said switching means (Q1) substantially unaffected, and when said fault indicative signal (301a) occurs, said means (303) for detecting a missing edge generates said third signal (303a) at one of said first and second states.

7. An apparatus according to Claim 5 or 6 characterized in that said third signal generating means comprises a flip-flop (303) having a first input terminal (303c) that is coupled to said first signal (O_H) and a second input terminal (303b) that is coupled to said second signal (O_{32H}) such that when the occurrence of said transition edges in said first signal (O_H) is prevented, said flip-flop (303) assumes a first state indefinitely.

8. An apparatus according to any one of the preceding claims characterized in that said first and second signal generating means comprise a phase-lock-loop circuit (20) that is synchronized to said input signal (S_H).



does not turn off at time t_4 and transistor Q1 is not turned on. Therefore, in the fault condition, transistor Q1 remains in cutoff even after time t_4 and is prevented from performing its switching operation. Therefore, ultor voltage U becomes zero.

Thus signal 303a of flip-flop 303 disables high voltage supply 35 when, as a result of the fault condition, high voltage protection circuit 301 prevents the generation of transition edges in signal O_H .

Claims

1. A television apparatus having a power supply with a fault protection arrangement, comprising:

a source of an input signal (S_H) at a frequency (f_H) that is related to a deflection frequency;

means (301) for generation of a fault indicative signal (301a) when a fault condition occurs in said power supply;

means (31,32,300) responsive to said input signal (S_H) for generating a first signal (O_H) at a first terminal (300a) during normal operation having transition edges at a frequency that is related to that of said input signal (S_H) such that when said fault indicative signal (301a) is generated, the occurrence of said transition edges of said first signal (O_H) is prevented, and for generating a second signal (O_{32H}) at a second terminal (40a), at least during normal operation, at a frequency ($32f_H$) that is related to that of said input signal (S_H);

a source of input supply voltage ($B+$);

a load (35); and

switching means (Q1), switching in response to said second signal (O_{32H}) and coupled to said load (35) and to said source of input supply voltage ($B+$) for developing an output supply voltage (at 34) for said load (35) during normal operation;

characterized by

means (303) for detecting a missing edge of said first signal (O_H) for generating a third signal (303a) when a transition edge within said first signal (O_H) is missing; and

means (Q3) responsive to said third signal (303a) and coupled to said switching means (Q1) for generating a signal (V_{BQ2}) that prevents the occurrence of said switching operation in order to substantially reduce said output supply voltage (at 34) when said third signal (303a) is generated.

2. An apparatus according to Claim 1 characterized in that said first signal (O_H) is at a frequency (f_H) that is related to a horizontal frequency

and wherein said second signal (O_{32H}) is at a higher frequency than that of said first signal (O_H).

3. An apparatus according to Claim 1 or Claim 2 characterized by a deflection winding (L_y) that forms with said switching means (Q1) a deflection circuit output stage (99).

4. An apparatus according to Claim 3 characterized in that said load (35) coupled to said switching means (Q1) comprises means for generating an ultor voltage, wherein said fault indicative signal generating means (301) generates said fault indicative signal (301a) when said ultor voltage exceeds a predetermined level so as to prevent subsequent generation of said ultor voltage.

5. An apparatus according to any one of the preceding claims characterized in that said third signal (303a) remains indefinitely at a first state when said fault indicative signal (301a) occurs to prevent the generation of said first signal (O_H), and wherein said third signal (303a) is coupled in a signal path that is between said switching means (Q1) and said second signal (O_{32H}) for decoupling said second signal (O_{32H}) from said switching means (Q1).

6. An apparatus according to any one of Claims 1 to 4 characterized in that, during normal operation, said third signal (303a) changes alternately between a first and a second state in a manner that maintains said switching operation in said switching means (Q1) substantially unaffected, and when said fault indicative signal (301a) occurs, said means (303) for detecting a missing edge generates said third signal (303a) at one of said first and second states.

7. An apparatus according to Claim 5 or 6 characterized in that said third signal generating means comprises a flip-flop (303) having a first input terminal (303c) that is coupled to said first signal (O_H) and a second input terminal (303b) that is coupled to said second signal (O_{32H}) such that when the occurrence of said transition edges in said first signal (O_H) is prevented, said flip-flop (303) assumes a first state indefinitely.

8. An apparatus according to any one of the preceding claims characterized in that said first and second signal generating means comprise a phase-lock-loop circuit (20) that is synchronized to said input signal (S_H).



9. An apparatus according to Claim 1 characterized by a ramp generator (37) responsive to said second signal (O_{32H}) for generating a ramp signal (37a) having a sawtooth waveform at a phase that is determined by that of said second signal (O_{32H}), means (99) for generating a deflection current (i_y) in a deflection winding (L_y) and for generating a phase indicative signal (F_H) that is indicative of said phase of said deflection current, a phase detector (57) responsive to said first signal (O_H) and to said phase indicative signal (F_H) for generating a phase difference indicative signal (59) in accordance with a phase difference between said phase indicative signal (F_H) and said first signal (O_H), phase shifting means (38) responsive to said phase difference signal (59) and to said ramp signal (37a) for generating an output signal (60) at least during normal operation that is at a frequency that is determined by that of said ramp signal (37a) and at a phase that is determined by said phase difference signal (59), and coupling means (Q2) responsive to said output signal (60) of said phase shifting means (38) and to said third signal (303a) for coupling said output signal (60) of said phase shifting means (38) to said switching means (Q1) during normal operation, and for decoupling said output signal (60) of said phase shifting means (38) from said switching means (Q1) when said third signal (303a) is generated.
10. An apparatus according to Claim 9 characterized in that said first (O_H) and second (O_{32H}) signals generating means comprise a phase-lock-loop circuit (20) and wherein said phase shifting means (38), said phase detector (57) and said phase indicative signal (F_H) form a phase-control-loop circuit (25).
11. An apparatus according to Claim 10 characterized in that said phase-lock-loop circuit (20) is included in an integrated circuit (IC100) and wherein said first (300a) and second (40a) terminals where said first (O_H) and second (O_{32H}) signals, respectively, are generated are coupled to said phase-control-loop circuit (25) that is located outside said integrated circuit (IC100).
12. An apparatus according to any one of Claims 9 to 11 in which said phase shifting means (38) generates said output signal (60) during both normal operation and when said fault indicative signal (301a) occurs.
13. An apparatus according to any one of the

preceding claims in which said second signal (O_{32H}) is generated both during normal operation and when said fault indicative signal (301a) occurs.

Patentansprüche

1. Fernsehgerät mit einer eine Fehlerschutzschaltung enthaltenden Stromversorgung;
 - mit einer Quelle zur Erzeugung eines Eingangssignals (S_H) mit einer Frequenz (f_H), die auf eine Ablenkfrequenz bezogen ist;
 - mit Mitteln (301) zur Erzeugung eines einen Fehler anzeigenden Signals (301a), wenn in der Stromversorgung ein Fehlerzustand auftritt;
 - mit Mitteln (31, 32, 300), die auf das Eingangssignal (S_H) ansprechen, um ein erstes Signal (O_H) an einer ersten Klemme (300a) während des Normalbetriebes zu erzeugen, das Flanken bei einer Frequenz hat, die auf die Frequenz des Eingangssignals (S_H) so bezogen ist, daß bei Erzeugung des einen Fehler anzeigenden Signals (301a) das Auftreten der Flanken des ersten Signals (O_H) verhindert wird, und um ein zweites Signal (O_{32H}) wenigstens während des Normalbetriebes an einer zweiten Klemme (40a) mit einer Frequenz ($32f_H$) zu erzeugen, die auf die Frequenz des Eingangssignals (S_H) bezogen ist;
 - mit einer Quelle zur Erzeugung einer Eingangs-Versorgungsspannung ($B+$);
 - mit einer Last (35); und
 - mit Schaltmitteln (Q1), die in Abhängigkeit von dem zweiten Signal (O_{32H}) schalten und mit der Last (35) und der Quelle zur Erzeugung der Eingangs-Versorgungsspannung ($B+$) verbunden sind, um eine Ausgangs-Versorgungsspannung (bei 34) für die Last (35) während des Normalbetriebes zu entwickeln; gekennzeichnet durch:
 - Mittel (303) zur Feststellung einer fehlenden Flanke des ersten Signals (O_H), um ein drittes Signal (303a) zu erzeugen, wenn eine Flanke in dem ersten Signal (O_H) fehlt;
 - Mittel (Q3), die auf das dritte Signal (303a) ansprechen und mit den Schaltmitteln (Q1) verbunden sind, um ein Signal (V_{BQ2}) zu erzeugen, das das Auftreten der Schaltoperation verhindert, um die Ausgangs-Versorgungsspannung (bei 34) beträchtlich zu verringern, wenn das dritte Signal (303a) erzeugt wird.
2. Gerät nach Anspruch 1, dadurch gekennzeichnet, daß das erste Signal (O_H) eine Frequenz (f_H) hat, die auf eine Horizontalfrequenz bezogen ist, und daß das zweite Signal (O_{32H}) eine höhere Frequenz als das erste Signal (O_H) hat.



3. Gerät nach Anspruch 1 oder 2, gekennzeichnet durch eine Abenkwicklung (L_V), die mit den Schaltmitteln (Q1) eine Ausgangsstufe (99) einer Ablenkschaltung bildet.
4. Gerät nach Anspruch 3, dadurch gekennzeichnet, daß die mit den Schaltmitteln (Q1) verbundene Last (35) Mittel enthält, um eine Endanodenspannung zu erzeugen, wobei die Mittel (301) zur Erzeugung des einen Fehler anzeigenden Signals dieses Signal (301a) erzeugen, wenn die Endanodenspannung einen vorgegebenen Pegel überschreitet, um so eine anschließende Erzeugung der Endanodenspannung zu verhindern.
5. Gerät nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß das dritte Signal (303a) in einem ersten Zustand unbestimmt bleibt, wenn das den Fehler anzeigende Signal (301a) auftritt, um die Erzeugung des ersten Signals (O_H) zu verhindern, und daß das dritte Signal (303a) einem Signalweg zwischen den Schaltmitteln (Q1) und dem zweiten Signal (O_{32H}) zugeführt wird, um das zweite Signal (O_{32H}) von den Schaltmitteln (Q1) abzukoppeln.
6. Gerät nach einem der Ansprüche 1 bis 4, dadurch gekennzeichnet, daß das dritte Signal (303a) während des Normalbetriebes zwischen einem ersten und einem zweiten Zustand so wechselt, daß die Schalteroperation in den Schaltmitteln (Q1) weitgehend unbeeinträchtigt bleibt, und daß bei Auftreten des einen Fehler anzeigenden Signals (301a) die Mittel (303) zur Feststellung einer fehlenden Flanke das dritte Signal (303a) bei dem ersten oder zweiten Zustand erzeugen.
7. Gerät nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die Mittel zur Erzeugung des dritten Signals einen Flip-Flop (303) enthalten, der eine erste Eingangsklemme (303c) hat, der das erste Signal (O_H) zugeführt wird, und der eine zweite Eingangsklemme (303b) hat, der das zweite Signal (O_{32H}) zugeführt wird, so daß, wenn das Auftreten der Flanken in dem ersten Signal (O_H) verhindert wird, der Flip-Flop einen ersten Zustand unbestimmt einnimmt.
8. Gerät nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die das erste und das zweite Signal erzeugenden Mittel eine PLL (phase-lock-loop)-Schaltung (20) enthalten, die mit dem Eingangssignal (S_H) synchronisiert ist.
9. Gerät nach Anspruch 1, gekennzeichnet durch einen Sägezahn-Generator (37), der auf das zweite Signal (O_{32H}) anspricht, um ein ansteigendes Signal (37a) mit Sägezahnform mit einer Phase zu erzeugen, die durch die Phase des zweiten Signals (O_{32H}) bestimmt ist, durch Mittel (99) zur Erzeugung eines Ablenkstroms (I_V) in einer Ablenkwicklung (L_V) und zur Erzeugung eines Signals (F_H), das die Phase des Ablenkstroms angibt, durch einen Phasendetektor (57), der auf das erste Signal (O_H) und auf das die Phase anzeigende Signal (F_H) anspricht, um ein die Phasendifferenz anzeigendes Signal (59) entsprechend einer Phasendifferenz zwischen dem die Phase anzeigenden Signal (F_H) und dem ersten Signal (O_H) zu erzeugen, durch Phasenschiebermittel (38), die auf das Phasendifferenzsignal (59) und auf das Sägezahnsignal (37a) ansprechen, um ein Ausgangssignal (60) wenigstens während des Normalbetriebes zu erzeugen, dessen Frequenz durch die Frequenz des Sägezahnsignals (37a) und dessen Phase durch das Phasendifferenzsignal (59) bestimmt ist, und durch Kopplungsmittel (Q2), die auf das Ausgangssignal (60) der Phasenschiebermittel (38) und das dritte Ausgangssignal (303a) ansprechen, um das Ausgangssignal (60) der Phasenschiebermittel (38) den Schaltmitteln (Q1) während des Normalbetriebes zuzuführen, und um das Ausgangssignal (60) der Phasenschiebermittel (38) von den Schaltmitteln (Q1) abzukoppeln, wenn das dritte Signal (303a) erzeugt wird.
10. Gerät nach Anspruch 9, dadurch gekennzeichnet, daß die das erste Signal (O_H) und das zweite Signal (O_{32H}) erzeugenden Mittel eine PLL (phase-lock-loop)-Schaltung (20) enthalten, und daß die Phasenschiebermittel (38), der Phasendetektor (57) und das die Phase anzeigende Signal (F_H) eine PCL (phase-control-loop)-Schaltung (25) bilden.
11. Gerät nach Anspruch 10, dadurch gekennzeichnet, daß die PLL-Schaltung (20) sich in einer integrierten Schaltung (IC 100) befindet, und daß die erste Klemme (300a) und die zweite Klemme (40a), an denen das erste Signal (O_H) bzw. das zweite Signal (O_{32H}) erzeugt wird, mit der PCL-Schaltung (25) verbunden sind, die sich außerhalb der integrierten Schaltung (IC 100) befindet.
12. Gerät nach einem der Ansprüche 9 bis 11, bei dem die Phasenschiebermittel (38) das Ausgangssignal (60) sowohl während des Normalbetriebes als auch bei Auftreten des einen Fehler anzeigenden Signals (301a) erzeugen.



13. Gerät nach einem der vorhergehenden Ansprüche, bei dem das zweite Signal (O_{32H}) sowohl während des Normalbetriebes als auch bei Auftreten des einen Fehler anzeigenden Signals (301a) erzeugt wird.

Revendications

1. Appareil de télévision comportant une source de puissance avec un circuit de protection contre les défauts comprenant :

- une source et un signal d'entrée (S) à une fréquence (f_H) qui est fonction d'une fréquence de déviation ;
- des moyens (301) pour générer un signal indiquant un défaut (301a) lorsqu'un état de défaut survient dans ladite source de puissance ;
- des moyens (31,32,300) agissant en réponse audit signal d'entrée (S_H) pour générer un premier signal (O_H), sur une première borne (300a) lors d'un fonctionnement normal, présentant des bords de transition à une fréquence qui est fonction de celle dudit signal d'entrée (S_H) de manière que, lorsque ledit signal indiquant le défaut (301a) est généré, on évite l'apparition desdits bords de transition dudit premier signal (O_H), et, pour générer un second signal (O_{32H}) sur une seconde borne (40a), au moins pendant le fonctionnement normal, à une fréquence ($32f_H$) qui est fonction de celle dudit signal d'entrée (S_H) ;
- une source de tension d'alimentation d'entrée ($B+$) ;
- une charge (35), et
- des moyens de commutation ($Q1$), commutant en réponse audit second signal (O_{32H}) et couplés à ladite charge (35) et à ladite source de tension d'alimentation d'entrée ($B+$) pour développer une tension d'alimentation de sortie (en 34) pour ladite charge (35) lors d'un fonctionnement normal, caractérisé par
- des moyens (303) pour détecter un bord manquant dudit premier signal (O_H) afin de générer un troisième signal (303a) lorsqu'un bord de transition est absent dans ledit premier signal (O_H) et,
- des moyens ($Q3$) agissant en réponse audit troisième signal (303a) et couplés auxdits moyens de commutation ($Q1$) pour générer un signal (V_{BQ2}) qui empêche l'apparition dudit fonctionnement de la commutation afin de réduire sensiblement ladite tension d'alimentation de sor-

tie (en 34) lorsque ledit troisième signal (303a) est généré.

2. Appareil selon la revendication 1 caractérisé en ce que ledit premier signal (O_H) est à une fréquence (f_H) qui est fonction d'une fréquence horizontale et dans lequel ledit second signal (O_{32H}) est à une fréquence plus élevée que celle dudit premier signal (O_H).
3. Appareil selon la revendication 1 ou la revendication 2, caractérisé par un enroulement de déviation (L_V) qui forme un étage de sortie (99) du circuit de déviation, avec lesdits moyens de commutation ($Q1$).
4. Appareil selon la revendication 3 caractérisé en ce que ladite charge (35), couplée auxdits moyens de commutation ($Q1$), comprend des moyens pour générer une tension d'accélération finale, dans lequel lesdits moyens générateurs du signal indiquant un défaut (301) génèrent ledit signal indicateur de défaut (301a) lorsque ladite tension d'accélération finale dépasse un niveau prédéterminé de manière à empêcher une génération ultérieure de ladite tension d'accélération finale.
5. Appareil selon l'une quelconque des revendications précédentes caractérisé en ce que ledit troisième signal (303a) demeure indéfiniment dans un premier état lorsque survient ledit signal indiquant un défaut (301a) pour empêcher la génération dudit premier signal (O_H) et dans lequel ledit troisième signal (303a) est couplé dans une trajectoire de signal qui est située entre lesdits moyens de commutation ($Q1$) et ledit second signal (O_{32H}) pour découpler ledit second signal (O_{32H}) desdits moyens de commutation ($Q1$).
6. Appareil selon l'une quelconque des revendications 1 à 4, caractérisé en ce que, lors du fonctionnement normal, ledit troisième signal (303a) change alternativement entre un premier et un second état de manière à ne pas affecter sensiblement l'opération de commutation desdits moyens de commutation ($Q1$), et, lorsque survient un signal indiquant un défaut (301a), lesdits moyens (303) de détection d'un bord manquant génèrent ledit troisième signal (303a) à l'un ou l'autre desdits premier et second états.
7. Appareil selon la revendication 5 ou 6 caractérisé en ce que lesdits moyens générant le troisième signal comprennent un flip-flop (303) ayant une première borne d'entrée (303c) qui



est couplée audit premier signal (O_H) et une seconde borne d'entrée (303b) qui est couplée audit second signal (O_{32H}) de manière que, lorsque l'apparition desdits bords de transition dans ledit premier signal (O_H) est empêchée, ledit flip-flop (303) assure indéfiniment un premier état.

8. Appareil selon l'une quelconque des revendications précédentes caractérisé en ce que lesdits moyens générant le premier et le second signal comprennent un circuit en boucle à verrouillage de phase (20) qui est synchronisé audit signal d'entrée (S_H).

9. Appareil selon la revendication 1 caractérisé par un générateur de rampe (37) agissant en réponse audit second signal (O_{32H}) pour générer un signal de rampe (37a) ayant une forme d'onde en dents de scie pour une phase qui est déterminée par celle dudit second signal (O_{32H}), des moyens (99) pour générer un courant de déviation (I_y) dans un enroulement de déviation (L_y) et pour générer un signal indicatif de phase (F_H) qui indique ladite phase dudit courant de déviation, un détecteur de phase (57) agissant en réponse audit premier signal (O_H) et audit signal indicatif de phase (F_H) pour générer un signal indiquant une différence de phase (59) selon une différence de phase entre ledit signal indicatif de phase (F_H) et ledit premier signal (O_H), des moyens de décalage de phase (38) agissant en réponse audit signal de différence de phase (59) et audit signal de rampe (37a) pour générer un signal de sortie (60), au moins pendant le fonctionnement normal, qui est à une fréquence déterminée par celle du signal de rampe (37a) et à une phase qui est déterminée par ledit signal de différence de phase (59) et, des moyens de couplage (Q2) agissant en réponse audit signal de sortie (60) des moyens de décalage de phase (38) et audit troisième signal (303a) pour coupler ledit signal de sortie (60) desdits moyens de décalage de phase (38) auxdits moyens de commutation (Q1) lors d'un fonctionnement normal, et, pour découpler des moyens de commutation Q1, ledit signal de sortie (60) desdits moyens de décalage de phase (38), lorsque ledit troisième signal (303a) est généré.

10. Appareil selon la revendication 9 caractérisé en ce que lesdits premiers (O_H) et seconds (O_{32H}) moyens de génération de signaux comprennent un circuit en boucle à verrouillage de phase (20) et dans lequel lesdits moyens de décalage de phase (38), ledit détecteur de phase (57) et ledit signal indicatif de phase

(F_H) forment un circuit en boucle à commande de phase (25).

11. Appareil selon la revendication 10 caractérisé en ce que ledit circuit en boucle à verrouillage de phase (20) est inclus dans un circuit intégré (IC100) et dans lequel lesdites première (300a) et seconde (40a) bornes, où sont respectivement générés lesdits premier (O_H) et second (O_{32H}) signaux, sont couplées audit circuit en boucle à commande de phase (25) qui est situé à l'extérieur dudit circuit intégré (IC100).

12. Appareil selon l'une quelconque des revendications 9 à 11 dans lequel lesdits moyens de décalage (38) génèrent ledit signal de sortie (60) à la fois pendant un fonctionnement normal et lorsque ledit signal indicatif de défaut (301a) survient.

13. Appareil selon l'une quelconque des revendications précédentes dans lequel ledit second signal (O_{32H}) est généré à la fois lors d'un fonctionnement normal et lorsque survient ledit signal indicatif de défaut (301a).