A MATERIAL ARCHITECTURE FOR THE FABRICATION OF LOW TEMPERATURE TRANSISTOR

ABSTRACT

A structure and method for forming a carbon-containing layer in at least a portion of the end of range regions of implanted PAI and/or doped regions. The C-containing layer/region getters defects from the implanted PAI region or doped region. Example embodiments show a C-containing layer under at FET. Other example embodiments show an implanted C-containing regions implanted into the EOR region of implanted doped regions, such as pocket regions, S/D regions and SDE regions. Low temperature anneals can be used because the carbon-containing layer reduces defects.

FIGURE 1B