

An Interconnect Structure And A Method Of Fabricating The Same

FIELD OF INVENTION

The present invention relates broadly to an interconnect structure, to an interconnect structure for interconnecting first and second components, to an interconnect structure for interconnecting a multiple component stack and a substrate, and to a method of fabricating an interconnect structure.

BACKGROUND

Bonded wires, solder bumps and metal pillars are common microstructures formed on micro devices which are usually fabricated on silicon wafers. Wire bonding is the earliest technique for interconnecting electronic devices. Thermosonic wire bonding is a commonly used technique. Conventional wire bonding allows Input/Output (I/O) pad bonding only on a chip perimeter near edges of a chip. Low profile and flexible long loop wire can be bonded across multiple chips and substrates. However, the trade-off in long wire interconnection is its high impedance and parasitic inductance and capacitance. Wire bonding is usually not suitable for high frequency and RF applications. Further, wire bonding over an active portion of a silicon chip may damage the delicate circuitry beneath it. This restriction limits the design for optimal power distribution and chip size shrinkage.

Flip-chip technology is an important development for the microelectronic industry. An optimized flip-chip device provides improvement in cost, reliability and performance over a wire-bonded device. The flip-chip device also has better electrical performance and lower impedance, inductance and capacitance. Aided by a self-alignment characteristic of solder, flip-chip packaging using solder bump has excellent yield. An area array interconnection format on flip-chip allows large number of I/Os to be distributed across the chip surface. This improves pitch spacing and power distribution. With no additional packaging material over the bare chip, the flip-chip has the smallest

possible size. As the flip-chip array pitch decreases, the interconnect solder bump diameter on the flip-chip may decrease correspondingly.

One disadvantage for reducing a solder bump size is the increase in the volume ratio of the IMC to bulk solder in an interconnecting joint. A higher percentage of the IMC in the solder joint is undesirable as the IMC is brittle and the fatigue life of the solder joint can be reduced. Another disadvantage is the increase in current density as the solder bump size decreases. As current density increases, electromigration will become a reliability concern in package interconnection.

Figure 1 shows a schematic drawing of a typical solder bump interconnection 100. The typical solder bump interconnection 100 comprises an under-bump-metallization (UBM) 102, a solder bump 104 and a matching substrate bond pad 106. However, the typical solder bump interconnection 100 has several inherent weaknesses. During reflow, the solder bump 104 will collapse and become barrel-shaped upon solidification. This limits the height and pitch of solder joints and applications of the solder bump interconnection 100 in high-density miniaturized packages. Further, truncated spherical ends 108 of the solder bump 104 are the main load bearing points and high stress concentrations occur at these spherical ends 108. UBM 102 interacts with the solder bump 104 and weakens the solder joints. Embrittlement at the IMC-solder interfaces 110 and coefficient of thermal expansion (CTE) mismatch in these IMC-solder interfaces 110 creates node for crack initiation and propagation.

Unlike solder bump, copper (Cu) pillar does not collapse during reflow soldering. Pillars can be packed closer together, increasing the interconnection density. If plating is done directly on the chip metal pads, intermetallic compound (IMC) formation on the chip interface is avoided. The concern of solder diffusion and interaction with the thin films on the chip is also eliminated. In addition, failure is unlikely to happen on the chip interface since Cu mechanical properties are much better than solder. The pillar structure can also be engineered such that stress concentration and shear strain on solder is reduced.

Figures 2a and 2b show a schematic drawing of a conventional pillar interconnect design 200 with a larger and a smaller pillar diameter respectively. A key issue of the conventional pillar interconnect design 200 is that the solder volume 204 and its wetting surface 206 vary as the diameter of the pillar 202 changes. The pillar 202 with a smaller diameter, as shown in Figure 2b, increases compliance as compared to the pillar 202 with a larger diameter, as shown in Figure 2a. However, the wetting surface 206 decreases when the diameter of the pillar 202 becomes smaller. A decrease in the wetting surface 206 may affect joint reliability. In addition, solder bumping cannot be done on a device with varying pillar diameters as this will result in non-planarity.

Hence, there is a need to provide an alternative interconnect structure, and method which seek to address at least one of the above-mentioned problems.

SUMMARY

In accordance with a first aspect of the present invention, there is provided an interconnect structure comprising: a base portion formed on a mounting surface of a first component; a pillar portion extending from the base portion and substantially perpendicularly to the mounting surface; and a head portion formed on the pillar portion and having larger lateral dimensions than the pillar portion; wherein the base portion and the pillar portion are integrally formed of a homogeneous material.

The base portion may have larger lateral dimensions than the pillar portion.

The base portion, the pillar portion and the head portion may be integrally formed of the homogeneous material.

The interconnect structure may further comprise an intermediate layer formed between the head portion and the pillar portion, the intermediate layer comprising materials other than the homogenous material.

The intermediate layer may comprise TiW and Cu, Ti and Cu, or Cr and Cu.

The base portion may be formed on a contact layer formed on the mounting surface of the first component.

The contact layer may comprise TiW and Cu, Ti and Cu, or Cr and Cu

The homogenous material may comprise a metal or a conducting material suitable for electroplating.

The metal may comprise one or more of a group consisting of Cu, Ni, and Au.

The pillar portion and the head portion may have a same cross sectional shape.

The pillar portion and the head portion may have a different cross sectional shape.

The pillar portion and the base portion may have a same cross sectional shape.

The pillar portion and the base portion may have a different cross sectional shape.

The head portion and the base portion may have a same cross sectional shape.

The head portion and the base portion may have a different cross sectional shape.

The head portion may have a surface disposed for facing a second component to which the first component is to be mounted.

The surface may be convex.

The surface may be planar.

A dielectric or passivation layer may be deposited on the first component and such that the pillar portion and the base portion are either encapsulated or remain exposed.

At least one of the base portion, the pillar portion and the head portion may be uniformly coated or selectively coated with one or more selected from a group consisting of a wetting layer, a diffusion barrier layer and a oxidation resistant layer.

In accordance with a second aspect of the present invention, there is provided an interconnect structure for interconnecting first and second components, the interconnect structure comprising: a base portion formed on a mounting surface of the first component; a pillar portion extending from the base portion and substantially perpendicularly to the mounting surface; and a head portion formed on the pillar portion and having larger lateral dimensions than the pillar portion; a contact pad formed on a mounting surface of the second component; and a connection for connecting the head portion of the interconnect structure to the contact pad; wherein the base portion and the pillar portion are integrally formed of a homogeneous material.

The connection for connecting the head portion of the interconnect structure to the contact pad may comprise one or more of a group consisting of solder, adhesive bonding, surface activated bonding, compression bonding and diffusion bonding.

A solder bump may be formed between facing surfaces of the head portion and the contact pad respectively.

The head portion and the contact pad may be substantially encapsulated by solder.

In accordance with a third aspect of the present invention, there is provided an interconnect structure for interconnecting a multiple component stack and a substrate, the interconnect structure comprising: a first base portion formed on a first mounting surface of a first component of the stack; a first pillar portion extending from the first base portion and substantially perpendicularly to the first mounting surface; and a second head portion formed on the second pillar portion and having larger lateral dimensions than the second pillar portion; a second base portion formed on a second mounting surface of a second component of the stack; a second pillar portion extending from the second base portion and substantially perpendicularly to the second mounting surface; and a second head portion formed on the second pillar portion and having larger lateral dimensions than the second pillar portion; a first and a second contact pad formed on a mounting surface of the substrate; and a connection for connecting the head portions to the respective contact pads respectively; wherein the base portions and the pillar portions are integrally formed of a homogeneous material pillar and the first pillar portion is higher than the second pillar portion.

The interconnect structure may further comprise a spacer disposed between the first and second components of the stack.

The connection for connecting the head portion of the interconnect structure to the contact pad may comprise one or more of a group consisting of solder, adhesive bonding, surface activated bonding, compression bonding and diffusion bonding.

In accordance with a fourth aspect of the present invention, there is provided a method of fabricating an interconnect structure, the method comprising: forming a base portion on a mounting surface of a first component; forming a pillar portion, the pillar portion extending from the base portion and substantially perpendicularly to the mounting surface; and forming a head portion on the pillar portion, the head portion having larger lateral dimensions than the pillar portion; and integrally forming the base portion and the pillar portion with a homogeneous material.

The method may further comprise forming the pillar portion and the head portion using different masks in a photolithography process.

The step of forming the pillar portion and the head portion may comprise an imprinting process

A mould for the imprinting process may be patterned and may comprise polymer, composite or metal materials.

The method may further comprise forming an intermediate layer between the head portion and the pillar portion.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will be better understood and readily apparent to one of ordinary skill in the art from the following written description, by way of example only, and in conjunction with the drawings, in which:

Figure 1 shows a schematic drawing of a typical solder bump interconnection.

Figures 2a and 2b show a schematic drawing of a conventional pillar interconnect design with a larger and a smaller pillar diameter respectively.

Figure 3a shows a schematic drawing of an assembly of a micro device chip and a substrate, which are connected by a pin-head interconnect structure and a solder bump, according to an example embodiment.

Figure 3b shows a schematic drawing of the assembly with a pin-head interconnect structure having a smaller diameter as compared to that shown in Figure 3a.

Figure 4a shows a schematic drawing of the pin-head interconnect of Figure 3.

Figures 4b and 4c show schematic drawings of variations of the pin-head interconnect of Figure 4a.

Figure 4d shows a schematic drawing of a variation of the pin-head interconnect of Figure 4b.

Figures 4e to 4g show top sectional views of the pin-head interconnect having different designs of horizontal portions.

Figures 5a to 5j show a process flow for fabricating a pin-head interconnect using photolithography-plating, according to an example embodiment.

Figures 6a to 6g show a continuation of a process for fabricating the pin-head interconnect using photolithography-plating from Figure 5e.

Figures 7a to 7g show an alternative continuation of a process for fabricating the pin-head interconnect using photolithography-plating from Figure 5e.

Figure 8a to 8j shows a process flow for fabrication of a pin-head interconnect using low cost imprinting-plating process, according to an example embodiment.

Figure 9a show a schematic drawing of pin-head interconnects connected to a micro device.

Figure 9b show a schematic drawing of planarized pin-head interconnects connected to the micro device.

Figures 10a to 10c show schematic drawings of one micro device interconnected to a substrate using different interconnect structures embodying the present invention.

Figures 11a and 11b show schematic drawings of two micro devices interconnected to the substrate using different interconnect structures embodying the present invention.

DETAILED DESCRIPTION

The embodiments described herein provide an interconnect structure to overcome the inherent weaknesses in solder bump interconnection. The embodiments also provide an improved interconnect structure to overcome the current limitations that metal interconnects and solder bumps have in micro devices packaging or integration.

Figure 3a shows a schematic drawing of an assembly 300 of a micro device chip 302 and a substrate 304, which are connected by a pin-head interconnect structure 306 and a solder bump 308. A base material of the micro device chip 302 can be, for example but not limited to, semiconductor materials such as silicon, ceramic, glass or polymer materials, or the like. The base material of the micro device chip 302 can be passivated with dielectric materials, metallized, patterned and circuited with channels, metal traces and pads. The pin-head interconnect 306 comprises a substantially vertical pillar portion 310 and a substantially horizontal head portion 312. The head portion 312 is disposed at one end of the pillar portion 310. The other end of the pillar portion 310 of the pin-head interconnect 306, i.e. the end opposite that having the head portion 312, is in contact with a micro device chip 302. The solder bump 308 is deposited between the head portion 312 and a metal pad 314 of a substrate 304. The pillar portion 310 and the head portion 312 of the pin-head interconnect 306 are made of a homogeneous metal. One example of the homogeneous metal is copper. It is preferred that the solder bump 308 is lead-free. The substrate 304 can be made of any polymer, composite or inorganic materials such as polyimide, glass-epoxy, ceramic or silicon etc. It will be appreciated by a person skilled in the art that other materials can be used for the micro device chip 302, the pin-head interconnect 306, the solder bump 308 and the substrate 304 in other embodiments.

Figure 3b shows a schematic drawing of the assembly 300 with a pillar portion 310 of a pin-head interconnect 306 having a smaller width 316 as compared to that of Figure 3a. By comparing Figures 3a and 3b, it can be observed that the size of the solder bump 308 does not change when the width 316 of the pillar portion 310 of the pin-head interconnect 306 decreases. Further, the assembly 300 advantageously allows a variation of a width to height aspect ratio of the pillar portion 310 of the pin-head

interconnect 306 to increase compliance of the assembly 300, without changing the solder bump size. This advantageously reduces the local shear strain on the interconnection due to coefficient of thermal expansion (CTE) mismatch between the micro device chip 302 and the substrate 304. The pin-head interconnect 306 advantageously allows standard solder pads and solder bumps to be used on the micro device chip 302 even if the widths 316 of the pillar portions 310 of the pin-head interconnects 306 across the micro device chip 302 are varied to give an optimal compliance at different locations of the micro device chip 302.

Figure 4a shows a schematic drawing of the pin-head interconnect 302 of Figure 3. The pin-head interconnect 302 comprises a substantially round pillar portion 306. The pin-head interconnect 302 further comprises a head portion 308 and a substantially horizontal base portion 402. The head portion 308 and the base portion 402 are disposed at respective ends of the pillar portion 306. Figure 4b shows a schematic drawing of a variation of the pin-head interconnect 302 of Figure 4a. In this embodiment, the pin-head interconnect 302 has a substantially rectangular vertical portion 306.

In the embodiments of Figures 4a and 4b, the head portion 308 and the base portion 402 of the pin-head interconnect 302 have larger lateral dimensions than the pillar portion 306. The head portion 308 and the base portion 402 have a same cross-sectional shape. The pillar portion 306 has a different cross-sectional shape as compared to those of the head portion 308 and the base portion 402.

Figure 4c shows a schematic drawing of a variation of the pin-head interconnect 302 of Figure 4a. Figure 4d shows a schematic drawing of a variation of the pin-head interconnect 302 of Figure 4b. In the embodiments of Figures 4c and 4d, the pin-head interconnect 302 can be considered to include a base portion 402 having same lateral dimensions and cross-sectional shape as the pillar portion 306. The head portion 308 has larger lateral dimensions than the pillar portion 306 and the base portion 402. The head portion 308 has a different cross-sectional shape as compared to those of the pillar portion 306 and the base portion 402.

Figure 4e shows a top sectional view of the pin-head interconnect 302 having a substantially round pillar portion 306 and a substantially round base portion 402 and a substantially round head portion 308. Figures 4f and 4g show top sectional views of the pin-head interconnect 302 with a round pillar portion 306 and a round base portion 402 but different designs of the head portion 308. In Figure 4f, the head portion 308 comprises two semi-circular elements 404. The semi-circular elements 404 are spaced apart and are arranged such that the respective straight edges 406 face each other and are aligned from one end to the other end. In Figure 4g, the head portion 308 is substantially cross shaped. In Figures 4e, 4f and 4g, the pillar portion 306 is disposed substantially in the centre of the head portion 308.

In the embodiments of Figures 4e, 4f and 4g, the pillar portion 306 has the same lateral dimensions and cross-sectional shape as the base portion 402. The head portion 308 has larger lateral dimensions than the pillar portion 306 and the base portion 402. The head portion 308 has a different cross-sectional shape as compared to those of the pillar portion 306 and the base portion 402. As appreciated by a person skilled in the art, the designs of the pillar portions 306, the head portions 308 and the base portions 402 of the pin-head interconnect 302 are not restricted to the examples as described above.

Two example methods, namely photolithography-plating and imprinting-plating, that can be used for manufacturing pin-head interconnects will now be described. Figures 5a to 5j show a process flow for fabricating a pin-head interconnect using photolithography-plating. Figure 5a shows a schematic diagram of a mounting surface in the form of an adhesion and seed layer 502 is deposited on a silicon (Si) chip 504. In this embodiment, the adhesion layer is about 100 to about 1000 angstrom and the seed layer is about 1000 to about 5000 angstrom. Titanium-tungsten (TiW) and copper (Cu) are used for the adhesion and seed layer 502. Depending on the base material of the chip, Ti and Cu or chromium (Cr) and Cu can also be used for the adhesion and seed layer 502 in other embodiments. A first photoresist (PR1) layer 506 is deposited on the adhesion and seed layer 502. A mask with a pattern (not shown) is placed above the PR1 layer 506. After the PR1 layer 506 is exposed to ultraviolet (UV) light through the patterned mask, a patterned opening 508 is formed as shown in Figure 5b. A copper layer 510 is deposited in the opening 508 by e.g. electroplating, which is shown in Figure

5c. In this embodiment, the thickness of the copper layer 510 is about 1.0 to about 10 micron.

The process of forming the copper layer 510 illustrated in Figures 5a to 5c is comparable to a process of forming a conventional chip pad. The copper chip pad 510 forms a base portion of a pin-head interconnect. This advantageously allows the pin-head interconnect to be plated directly on the copper chip pad. This advantageously provides an ease of integration of manufacturing an array of pin-head interconnects at a wafer level.

Figure 5d shows a schematic diagram of a second photoresist (PR2) layer 512 deposited on the PR1 layer 506 with an opening 514 formed. The opening 514 is formed in the PR2 layer 512 with conventional photolithography processes. A copper layer 516 is deposited in the opening 514 by e.g. electroplating, as shown in Figure 5e. The copper layer 516 forms a pillar portion of a pin-head interconnect. The height to diameter aspect ratio of the pillar portion is preferably about 0.5 to about 4.0. A copper layer 518 having a convex surface is deposited in the opening 514 by e.g. electroplating, as shown in Figure 5f. The convex copper layer 518 is formed due to isotropic copper ion deposition on the pillar portion 516 above the PR2 layer 512. The convex copper layer 518 forms a head portion of a pin-head interconnect. Figure 5g shows that a convex pin-head interconnect 520 made of Cu is formed after electroplating. The PR1 layer 506 and PR2 layer 512 are removed. Figure 5h shows that portions of the adhesion and seed layer 502 which extend beyond the copper layer 510 are removed. Figure 5i shows that a dielectric or passivation layer 522 is deposited on the silicon chip 504. Benzocyclobutene (BCB) can be used for the dielectric or passivation layer 522 in this embodiment. The dielectric or passivation layer 522 encapsulates the base portion and part of the pillar portion of the pin-head interconnect 520. Figure 5j shows that portions of the dielectric or passivation layer 522 are removed. The dielectric or passivation layer 522 encapsulating the base portion and part of the pillar portion of the pin-head interconnect 520 can be removed by using conventional photolithography processes if a photoimageable layer 522 is used in this embodiment.

In other embodiments, it is possible to end the process of manufacturing the pin-head interconnect at Figure 5i. The step of removing some portions of the dielectric or passivation layer 522 can produce metal-pad-defined interconnect structures.

Alternatively, after the copper layer 516 is deposited in the gap 514 as shown in Figure 5e, a third photoresist (PR3) layer 602 can be deposited on the PR2 layer 512 (as shown in Figure 6a) or an adhesion and seed layer 702 can be deposited on the PR2 layer 512 (as shown in Figure 7a).

With reference to Figure 6a, a third photoresist (PR3) layer 602 is deposited on the PR2 layer 512, an opening 604 is formed in the PR3 layer 602 with conventional photolithography processes. A copper layer 606 having a convex surface is deposited in the opening 604 by e.g. electroplating, as shown in Figure 6b. The convex surface of the copper layer 606 is formed due to isotropic copper ion deposition. The PR3 layer 602 serves to constrain and define the formation and growth of the convex copper layer 606 according to the patterned opening 604. The copper layer 606 forms a head portion of a pin-head interconnect. The copper layer 606 can be planarized to produce a flat pin-head using chemical, mechanical or chemical-mechanical means before PR3 layer 602 is removed.

Figure 6c shows that a pin-head interconnect 608 made of Cu with a planarized copper layer 606 after planarization. Figure 6d shows that the PR1 layer 506, the PR2 layer 512 and the PR3 layer 602 are removed. Figure 6e shows that portions of the adhesion and seed layer 502 which extend beyond the copper layer 510 are removed. Figure 6f shows a dielectric or passivation layer 610 deposited on the silicon chip 504. In this embodiment, benzocyclobutene (BCB) is used for the dielectric or passivation layer 610. The dielectric or passivation layer 610 encapsulates the base portion and part of the pillar portion of the pin-head interconnect 608. Figure 6g shows that portions of the dielectric or passivation layer 610 encapsulating the base portion and part of the pillar portion of the pin-head interconnect 608 are removed. The dielectric or passivation layer 610 can be removed by using conventional photolithography processes if a photoimageable layer 610 is used in this embodiment.

In other embodiments, it is possible to end the process of manufacturing the pin-head interconnect at Figure 6f. The step of removing some portions of the dielectric or passivation layer 610 can produce metal-pad-defined interconnect structures.

With reference to Figure 7a, where an adhesion and seed layer 702 is deposited on the PR2 layer 512, a third photoresist (PR3) layer 704 is deposited on the layer 702. Titanium-tungsten (TiW) and copper (Cu) are used for the adhesion and seed layer 702. Depending on the base material of the chip, Ti and Cu or chromium (Cr) and Cu can also be used for the adhesion and seed layer 702 in other embodiments. An opening 706 is formed in the PR3 layer 704, as shown in Figure 7b, with conventional photolithography processes. A copper layer 708 having a substantially planar surface is deposited in the opening 706, as shown in Figure 7c. Figure 7d shows that the PR1 layer 506, the PR2 layer 512 and the PR3 layer 704 are removed. The portions of the adhesion and seed layer 702 which extend beyond the copper layer 708 are removed. The adhesion and seed layer 702 and the copper layer 708 form a head portion 710 of a pin-head interconnect. Figure 7e shows that portions of the adhesion and seed layer 502 which extend beyond the copper layer 510 are removed. A pin-head interconnect 712 made of Cu is formed. Figure 7f shows a dielectric or passivation layer 714 deposited on the silicon chip 504. In this embodiment, benzocyclobutene (BCB) is used for the dielectric or passivation layer 714. The dielectric or passivation layer 714 encapsulates the base portion and part of the pillar portion of the pin-head interconnect 712. Figure 7g shows that portions of the dielectric or passivation layer 714 encapsulating the base portion and part of the pillar portion of the pin-head interconnect 712 are removed. The dielectric or passivation layer 714 can be removed by using conventional photolithography processes if a photoimageable layer 714 is used in this embodiment.

In other embodiments, it is possible to end the process of manufacturing the pin-head interconnect at Figure 7f. The step of removing some portions of the dielectric or passivation layer 714 can produce metal-pad-defined interconnect structures.

Figure 8a to 8j shows a process flow for fabrication a pin-head interconnect using low cost imprinting-plating process. Figure 8a shows a schematic diagram of a mounting surface in the form of an adhesion and seed layer 802 deposited on a silicon (Si) chip

804. Titanium-tungsten (TiW) and copper (Cu) are used for the adhesion and seed layer 802. Depending on the base material of the chip, Ti and Cu or chromium (Cr) and Cu can also be used for the adhesion and seed layer 802 in other embodiments. A first photoresist (PR1) layer 806 is deposited on the adhesion and seed layer 804. An opening 808 is formed in the PR1 layer 806, as shown in Figure 8b, with conventional photolithography processes. Alternatively, the PR1 layer 806 can be a non photosensitive polymer resist which is imprinted with a patterned mould and plasma ashed to produce the opening 808. A copper layer 810 is deposited in the opening 808 by e.g. electroplating, which is shown in Figure 8c.

The process of forming the copper layer 810 illustrated in Figures 8a to 8c is comparable to a process of forming a conventional chip pad. The copper chip pad 810 forms a base portion of a pin-head interconnect. This advantageously allows the pin-head interconnect to be plated directly on the copper chip pad. This advantageously provides an ease of integration of the manufacturing an array of pin-head interconnects at a wafer level.

Figure 8d shows a schematic diagram of a second polymer resist (PR2) layer 812 deposited on the PR1 layer 806. An imprinting mould 814 is used to form a cavity 816 in the PR2 layer 812, as shown in Figure 8e. The imprinting mould 814 is made of nickel in this embodiment. Other polymer, composite or metal materials can be used to fabricate the mould 814 in different embodiments. The residues of the PR2 layer 812 at the bottom of the cavity 816 can be removed by plasma ashing followed by wet chemical cleaning. The mould imprinting process enables high aspect ratio openings to be formed on a thick polymer resist. As shown in Figure 8e, a cavity with a complex geometry can be formed in one imprinting step. Copper is deposited into the cavity 816 by e.g. electroplating and the copper layer 818 has a convex pin-head surface, as shown in Figure 8f. The convex surface of the copper layer 818 is formed due to isotropic copper ion deposition. In this embodiment, the copper layer 818 forms a pillar portion and a head portion of a pin-head interconnect. The convex pin-head can be planarized using chemical, mechanical or chemical-mechanical planarizing processes before the removal of the PR2 layer 812 in other embodiments.

Figure 8g shows that a pin-head interconnect 820 made of Cu is formed. The PR1 layer 806 and the PR2 layer 812 are removed. Figure 8h shows that portions of the adhesion and seed layer 802 which extend beyond the copper layer 810 are removed. Figure 8i shows a dielectric or passivation layer 822 deposited on the silicon chip 804. In this embodiment, benzocyclobutene (BCB) is used for the dielectric or passivation layer 822. The dielectric or passivation layer 822 encapsulates the base portion and part of the pillar portion of the pin-head interconnect 820. Figure 8j shows that portions of the dielectric or passivation layer 822 encapsulating the base portion and part of the pillar portion of the pin-head interconnect 820 are removed. The dielectric or passivation layer 822 can be removed by using conventional photolithography processes if a photoimageable layer 822 is used in this embodiment.

In other embodiments, it is possible to end the process of manufacturing the pin-head interconnect at Figure 8i. The step of removing some portions of the dielectric or passivation layer 822 can produce metal-pad-defined interconnect structures.

In the above described photolithography-plating and imprinting-plating processes, the formation of the pin-head interconnect can be viewed as the formation of a modified chip interconnect structure. Further, parts including the base portion, the pillar portion and the head portion of the interconnect structures can be uniformly or selectively treated or coated to enhance their wetting, diffusion and oxidation resistant behaviour. Nickel, for example, is commonly used as a diffusion barrier layer and gold as an oxidation resistant layer. These metals can be deposited on the interconnect structures by sputtering or electroplating processes. The pin-head interconnect structures can be advantageously fabricated at the wafer level. The micro devices can be assembled on a substrate with or without underfill encapsulation.

Further, copper is used to form the base portions and the pillar portions of the pin-head interconnects described above. In other embodiments, nickel or gold can be used for forming the base portion and the pillar portion. In such embodiments, the adhesion and seed layer may comprise nickel or gold.

In the above described photolithography-plating and imprinting-plating processes, the pin-head interconnects are first formed on the silicon chip and substrates are then brought into contact with the pin-head interconnects. In other embodiments, the pin-head interconnects can be first formed on the substrates and the silicon chips are then brought into contact with the pin-head interconnects.

Figure 9a show a schematic drawing of pin-head interconnects 902 connected to a micro device 904. The micro device 904 can be any devices with electronic, optic, fluidic or micro-electro-mechanical functions or a combination of these functions. The pin-head interconnects 902 comprise a base portion 906, a pillar portion 908 and a head portion 910. The base portion 906 and the head portion 910 are disposed at respective ends of the pillar portion 908. A passivation layer 914 of the micro device 904 can be of photoimageable or non-photoimageable material.

In this embodiment, the base portion 906 and the head portion 910 have larger lateral dimensions than the pillar portion 906. The head portion 910 has larger lateral dimensions than the base portion 906. The base portion 906, the pillar portion 908 and the head portion 910 have different cross-sectional areas. The base portion 906 surface is substantially planar and the head portion 910 has a curved surface.

Figure 9b show a schematic drawing of another example of pin-head interconnects 902 of Figure 9a connected to the micro device 904. The head portion 912 of the pin-head interconnects 902 have a substantially planar surface.

Figures 10a, 10b and 10c show schematic drawings of one micro device 904 interconnected to a substrate 10. In Figure 10a, the pin-head interconnects 902 of Figure 9b are connected to metal pads 1002 of a substrate 1004 using methods, e.g. solder, adhesive bonding, indirect bonding or direct bonding. In Figure 10b, the pin-head interconnects 902 of Figure 9b are connected to the metal pads 1002 of the substrate 1004 using solder bumps 1006. The solder bumps 1006 can be preformed on either the pin-head interconnects 902 or the metal pads 1002 before the pin-head interconnects 902 and the substrate 1004 are brought together. In Figure 10c, the pin-head interconnects 902 of Figure 9b are connected to the embedded metal pads 1002 of the

substrate 1004 by solders 1008 or other attachment methods like adhesive bonding, surface activated bonding, compression bonding or diffusion bonding. The embedded metal pads 1002 are formed within the cavities of the substrate 1012. The head portions 912 of the pin-head interconnects 902 are fully encapsulated by solders 1008. Alternatively, the horizontal portions 912 of the pin-head interconnects 902 can be partially encapsulated by the solders 1008.

The pin-head interconnects can be used for joining, interconnecting or supporting micro devices 904 for purposes of packaging and integration. Figures 11a and 11b show schematic drawings of two micro devices 904 interconnected to the substrate 1004. In Figure 11a, the pin-head interconnects 902 are connected to the metal pads 1002 of the substrate 1004 using methods, e.g. solder, adhesive, surface activated, compression or diffusion bonding. In Figure 11b, the pin-head interconnects 902 are connected to the metal pads 1002 of the substrate 1004 using solder bumps 1006. A spacer 1102 is disposed between the micro devices 904 in the embodiments. In other embodiments, more than two micro devices 904 can be interconnected to the substrate 1004.

With the pin-head interconnect design in the example embodiments, the Cu pin-head interconnect can advantageously be plated directly on a Cu metallized chip pad. Hence, UBM is no longer necessary on a chip pad. Designing and optimizing the interconnect reliability on the substrate side is less complex because the concern of thin film materials and active device interaction exist only on the chip side.

High current, coupled with the need to reduce the package size, lead to high heat generation within the package. The ability to design and structure Cu interconnect for specific locations on the same chip can advantageously enhance thermal performance significantly. As a chip size gets smaller and denser, high temperature and current density promote electromigration is a growing concern. Since the melting point of Cu is 1083°C, which is much higher in comparison to the melting point of most leaded or lead-free solder materials, the atomic diffusion of a Cu pin-head interconnect is advantageously much slower than most solder materials. Hence, electromigration is advantageously reduced in the Cu pin-head interconnect.

It will be appreciated by a person skilled in the art that numerous variations and/or modifications may be made to the present invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects to be illustrative and not restrictive.

For example, it will be appreciated that in different embodiments, the base of the pillar structure is formed on a surface of the substrate, for connection of the pillar head to the chip. More generally, the interconnect structure can be applied between mounting surfaces of two components or elements to be interconnected, or between multi component stacks and a substrate, in different embodiments.

Furthermore, the homogenous material for the interconnect structure may comprise any metal or any conducting material suitable for electroplating, in different embodiments.

Furthermore, in other embodiments, the interconnect structure can be formed on any surface that can be subjected to electroplating for formation of the interconnect structure. Also, if the interconnect structure is to be formed on surfaces that cannot be subjected to electroplating, a seed plating layer may be deposited. An additional adhesion layer may be required if the seed layer cannot adhere directly to the base material of the surface.

In various embodiments, the interconnect structure can be fabricated by other electroplated metals like nickel or gold. The adhesion layer can be TiW, Ti or Cr and the seed layer for plating can be nickel or gold if a silicon, glass or ceramic substrate is used. For other materials like epoxy-glass fibre base, the seed or plating layer can be laminated on the base material.

CLAIMS

1. An interconnect structure comprising:
a base portion formed on a mounting surface of a first component;
a pillar portion extending from the base portion and substantially perpendicularly to the mounting surface; and
a head portion formed on the pillar portion and having larger lateral dimensions than the pillar portion;
wherein the base portion and the pillar portion are integrally formed of a homogeneous material.
2. The interconnect structure as claimed in claim 1, wherein the base portion has larger lateral dimensions than the pillar portion.
3. The interconnect structure as claimed in claims 1 or 2, wherein the base portion, the pillar portion and the head portion are integrally formed of the homogeneous material.
4. The interconnect structure as claimed in claims 1 or 2, further comprising an intermediate layer formed between the head portion and the pillar portion, the intermediate layer comprising materials other than the homogenous material.
5. The interconnect structure as claimed in claim 4, wherein the intermediate layer comprises TiW and Cu, Ti and Cu, or Cr and Cu.
6. The interconnect structure as claimed in any one of claims 1 to 5, wherein the base portion is formed on a contact layer formed on the mounting surface of the first component.
7. The interconnect structure as claimed in claim 6, wherein the contact layer comprises TiW and Cu, Ti and Cu, or Cr and Cu.

8. The interconnect structure as claimed in any one of claims 1 to 7, wherein the homogenous material comprises a metal or a conducting material suitable for electroplating.

9. The interconnect structure as claimed in claim 8, wherein the metal comprises one or more of a group consisting of Cu, Ni, and Au.

10. The interconnect structure as claimed in any one of claims 1 to 9, wherein the pillar portion and the head portion have a same cross sectional shape.

11. The interconnect structure as claimed in any one of claims 1 to 9, wherein the pillar portion and the head portion have a different cross sectional shape.

12. The interconnect structure as claimed in any one of claims 1 to 11, wherein the pillar portion and the base portion have a same cross sectional shape.

13. The interconnect structure as claimed in any one of claims 1 to 11, wherein the pillar portion and the base portion have a different cross sectional shape.

14. The interconnect structure as claimed in any one of claims 1 to 13, wherein the head portion and the base portion have a same cross sectional shape.

15. The interconnect structure as claimed in any one of claims 1 to 13, wherein the head portion and the base portion have a different cross sectional shape.

16. The interconnect structure as claimed in any one of claims 1 to 15, wherein the head portion has a surface disposed for facing a second component to which the first component is to be mounted.

17. The interconnect structure as claimed in claim 16, wherein the surface is convex.

18. The interconnect structure as claimed in claim 16, wherein the surface is planar.

19. The interconnect structure as claimed in any one of claims 1 to 18, wherein a dielectric or passivation layer is deposited on the first component and such that the pillar portion and the base portion are either encapsulated or remain exposed.

20. The interconnect structure as claimed in any one of claims 1 to 19, wherein at least one of the base portion, the pillar portion and the head portion are uniformly coated or selectively coated with one or more selected from a group consisting of a wetting layer, a diffusion barrier layer and a oxidation resistant layer.

21. An interconnect structure for interconnecting first and second components, the interconnect structure comprising:

a base portion formed on a mounting surface of the first component;

a pillar portion extending from the base portion and substantially perpendicularly to the mounting surface; and

a head portion formed on the pillar portion and having larger lateral dimensions than the pillar portion;

a contact pad formed on a mounting surface of the second component; and

a connection for connecting the head portion of the interconnect structure to the contact pad;

wherein the base portion and the pillar portion are integrally formed of a homogeneous material.

22. The interconnect structure as claimed in claim 21, wherein the connection for connecting the head portion of the interconnect structure to the contact pad comprises one or more of a group consisting of solder, adhesive bonding, surface activated bonding, compression bonding and diffusion bonding.

23. The interconnect structure as claimed in claim 21, wherein a solder bump is formed between facing surfaces of the head portion and the contact pad respectively.

24. The interconnect structure as claimed in claim 21, wherein the head portion and the contact pad are substantially encapsulated by solder.

25. An interconnect structure for interconnecting a multiple component stack and a substrate, the interconnect structure comprising:

- a first base portion formed on a first mounting surface of a first component of the stack;

- a first pillar portion extending from the first base portion and substantially perpendicularly to the first mounting surface; and

- a second head portion formed on the second pillar portion and having larger lateral dimensions than the second pillar portion;

- a second base portion formed on a second mounting surface of a second component of the stack;

- a second pillar portion extending from the second base portion and substantially perpendicularly to the second mounting surface; and

- a second head portion formed on the second pillar portion and having larger lateral dimensions than the second pillar portion;

- a first and a second contact pad formed on a mounting surface of the substrate; and

- a connection for connecting the head portions to the respective contact pads respectively;

wherein the base portions and the pillar portions are integrally formed of a homogeneous material pillar and the first pillar portion is higher than the second pillar portion.

26. The interconnect structure as claimed in claim 25, further comprising a spacer disposed between the first and second components of the stack.

27. The interconnect structure as claimed in claim 25, wherein the connection for connecting the head portion of the interconnect structure to the contact pad comprises one or more of a group consisting of solder, adhesive bonding, surface activated bonding, compression bonding and diffusion bonding.

28. A method of fabricating an interconnect structure, the method comprising:

- forming a base portion on a mounting surface of a first component;
- forming a pillar portion, the pillar portion extending from the base portion and substantially perpendicularly to the mounting surface; and
- forming a head portion on the pillar portion, the head portion having larger lateral dimensions than the pillar portion; and
- integrally forming the base portion and the pillar portion with a homogeneous material.

29. The method as claimed in claim 28, further comprising forming the pillar portion and the head portion using different masks in a photolithography process.

30. The method as claimed in claim 28, wherein the step of forming the pillar portion and the head portion comprises an imprinting process.

31. The method as claimed in claim 30, wherein a mould for the imprinting process is patterned and comprises polymer, composite or metal materials.

32. The method as claimed in any one of claims 28 to 31, further comprising forming an intermediate layer between the head portion and the pillar portion.