

ABSTRACT**WAFER-LEVEL CHIP MANUFACTURING METHOD**

The present invention discloses a wafer-level chip manufacturing method, comprising:
providing a first wafer; forming a first bonding layer on the first wafer; providing a second
5 wafer and at least four second chips; bonding the second chips onto the second wafer;
continuing to form a first dielectric layer on the second wafer bonded with the second
chips; etching the first dielectric layer to form through-holes, and depositing a conductive
material in the through-holes to form first vertical conductive plugs interconnected with
electrodes of the second chips; forming a horizontal conductive structure interconnected
10 with the first vertical conductive plugs on the first dielectric layer; continuing to form a
second dielectric layer on the first dielectric layer and the horizontal conductive
interconnect structure to form a second reconstituted wafer; bonding the second
reconstituted wafer and the first wafer; removing the second wafer; and etching the first
dielectric layer and the second dielectric layer. This method improves system-in-package
15 integration density and achieves better line width and higher yield.