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High-Voltage Solid-State Switch.

This invention relates to solid-state switches and, in particular, to those capable of blocking high
5 voltages.

In an article entitled "Development of Integrated Semiconductor Crosspoint Switches and a Fully Electronic Switching System" by Michio Tokunaga et al, International Switching Symposium, October 26, 1976, at
10 Kyoto, Japan, Paper 221-4, there is illustrated a dielectrically isolated all solid-state high voltage switch having an n type bulk semiconductor body. A p+ type conductivity anode region is separated from a p+ type conductivity first gate region only by portions of
15 the bulk of the body. The first gate region surrounds and contacts an n+ type conductivity cathode region. A second p+ type conductivity gate region exists in the semiconductor body and is located in a portion of the semiconductor body other than between the anode and
20 first gate regions. The switch is turned on by injecting or extracting current from one of the gate regions. Once current flow between anode and cathode ceases, then the switch reverts to its normally off blocking state. One deficiency of this structure is
25 that it is unable conveniently to interrupt existing substantial current flow between anode and cathode (the output terminals).

28 It is desirable to have an all solid-state

switch much like the one described hereinabove, but in which it is possible readily to interrupt (cut off) existing substantial current flow between the output terminals thereof.

5 According to the present invention there is provided a solid-state switching device comprising: a semiconductor body having a major surface and a bulk portion of a first conductivity type; first, second, and third mutually separated regions of the semiconductor
10 body which each have a portion thereof common with the major surface; a fourth region of the semiconductor body which separates the third region from the bulk portion; the second and third regions being of the first conductivity type and being of lower resistivity than
15 the bulk portion of the semiconductor body; the first and fourth regions being of a second conductivity type which is opposite of the first conductivity type and being of lower resistivity than the bulk portion of the semiconductor body; and the second region being located
20 in between the first and fourth regions.

 An embodiment of the invention will now be described by way of example with reference to the single Figure which illustrates a high voltage switch in accordance with the invention.

25 In the Figure there is illustrated a perspective view of a structure 10 having a planar surface 11 and comprising a polycrystalline semiconductive member 12 supporting a monocrystalline semiconductor body 16 whose bulk is of n type conductivity, and which is separated
30 from support member¹² by a dielectric layer 14.

 A localized anode region 18, which is of p+ type conductivity, is included in body 16 and has a portion which forms a part of surface 11. A localized gate region 20, which is of n+ type conductivity, is also
35 included in body 16 and has a portion which forms a part of surface 11. A localized cathode region 24, which is of n+ type conductivity, is included in body 16 and has
38 a portion which forms a part of surface 11. A region 22,

which is of p type conductivity closely surrounds cathode region 24 and acts as a depletion layer punch-through shield. In addition it acts to inhibit inversion of the portions of body 16 at or near surface 11 between regions 20 and 24. Gate region 20 is located between anode region 18 and region 22 and is separated from both by n- type bulk portions of body 16. The resistivities of regions 18, 20, and 24 are low compared to that of the bulk portions of body 16. The resistivity of region 22 is intermediate between that of cathode region 24 and that of the bulk portions of body 16.

Electrodes 28, 30, and 32 are conductors which make low resistance contact to the surface portions of regions 18, 20, and 24, respectively. An apertured dielectric covers major surface 11 so as to isolate electrodes 28, 30, and 32 from all regions other than those intended to be electrically contacted. An electrode 36 provides a low resistance contact to support 12 by way of a highly doped region 34 which is of the same n type conductivity type as support 12.

The support 12 and the body 16 are each of silicon and the support 12 can alternatively be of p type conductivity in which case the region 34 must also be. As shown, electrodes 28, 30, and 32 overlap the edges of the semiconductor regions to which they make low resistance contact, although separated from the edges by portions of layer 26. Electrode 32 also completely overlaps region 22. This overlapping, which is known as field plating, facilitates high voltage operation because it increases the voltage at which breakdown occurs.

In the illustrative embodiment, support 12 and body 16 and regions 18, 20, 22, 24, and 34 are all silicon and are of n-, n-, p+, n+, p, n+, and n+ type conductivity, respectively, where the "+" designates relatively low resistivity and "-" designates relatively high resistivity. Dielectric layer 14 is silicon dioxide and electrodes 28, 30, 32, and 36 are all aluminum layers.

A plurality of separate bodies 16 can be formed in a common support 12 to provide in one integrated structure a plurality of switches.

Structure 10 is typically operated as a switch 5 which has a low impedance path between anode region 18 and cathode region 24 when in the ON (conducting) state and has a high impedance between these two regions when in the OFF (blocking) state. The potential applied to the gate region 20 determines the state of the switch when 10 appropriate operating voltages are maintained on the other electrodes. Conduction between anode region 18 and cathode region 24 occurs if the potential of anode region 18 is sufficiently greater than that of cathode region 24 and if the potential of gate region 20 is below that of 15 anode region 18. During the ON state holes are injected into body 16 from anode region 18 and electrons are injected into body 16 from cathode region 24. These holes and electrons are in sufficient numbers to form a plasma which conductivity modulates body 16. This effectively 20 lowers the resistance of body 16 such that the resistance between anode region 18 and cathode region 24 is relatively low when structure 10 is operating in the ON state. This type of operation is denoted as dual carrier injection.

25 Region 22 helps limit the punch-through of a depletion layer formed during operation between gate region 20 and cathode region 24 and helps inhibit formation of a surface inversion layer between these two regions. In addition, it facilitates gate region 20 and 30 cathode region 24 being relatively closely spaced apart. This facilitates relatively low resistance between anode region 18 and cathode region 24 during the ON state.

Support 12 is typically held at the most positive potential level available. Conduction between anode 35 region 18 and cathode region 24 is inhibited or cut off if the potential of gate region 20 is sufficiently more positive than that of anode region 18, cathode region 24 38 and region 22. The amount of excess positive potential

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needed to inhibit or cut off conduction depends on the geometry and impurity concentration (doping) levels of structure 10. This positive gate potential causes a portion of body 16 between gate region 20 and the dielectric layer 14 to be more positive in potential than anode region 18, cathode region 24 and/or region 22. This positive potential barrier inhibits the conduction of holes from anode region 18 to cathode region 24. In addition, depletion regions are formed at the junctions of anode region 18 and body 16 and between region 22 and body 16. The electric field within the depletion regions serves to retain holes within anode region 18 and region 22 and thus limits current flow between the anode and cathode regions (18 and 24). Gate region 20 collects electrons emitted at cathode region 24 before they can reach anode region 18.

During the ON state of structure 10, the junction diode comprising anode region 18 and semiconductor body 16 becomes forward-biased. Current limiting means such as a load (not illustrated) are normally included to limit the conduction through the forward-biased diode. While structure 10 is in the ON state the potential of the gate region 20 can be raised above the anode region 18 potential and current flow will continue between anode region 18 and cathode region 24 until the portion of semiconductor body 16 below gate region 20 and down to dielectric layer 14 is more positive in potential than anode region 18, cathode region 24, and region 22.

One typical embodiment has the following design. Support member 12 is an n type silicon substrate, 18 to 22 mils (0.45 to 0.55mm) thick to provide mechanical support, with an impurity concentration of approximately 2×10^{13} impurities/cm³ corresponding to a resistivity greater than 100 ohm-centimetres. The other dimensions are dictated by the size and number of bodies 16 to be included. Dielectric layer 14 is a silicon dioxide layer that is 2 to 4 microns thick. Body 16 is typically 30 to 55 microns thick, approximately 430 microns long, 300

microns wide, and is of n- type conductivity with an impurity concentration in the range of approximately $5-9 \times 10^{13}$ impurities/cm³. Anode region 18 is of p+ type conductivity, is typically 2 to 4 microns thick, 44 microns wide, 52 microns long, and has an impurity concentration of approximately 10^{19} impurities/cm³ or larger. Electrode 28 is typically aluminum, with a thickness of $1\frac{1}{2}$ microns, a width of 84 microns, and a length of 105 microns. Region 20 is of n+ type conductivity and is typically 2 to 20 microns thick, 15 microns wide, 300 microns long, and has an impurity concentration of approximately 10^{19} impurities/cm³ or larger. Electrode 30 is aluminum, $1\frac{1}{2}$ microns thick, 50 microns wide, and 340 microns long. The spacing between adjacent edges of electrodes 28 and 30 and between adjacent edges of electrodes 30 and 32 is typically 40 microns in both cases. Region 22 is p type conductivity and is typically 3-6 microns thick, 64 microns wide, 60 microns long, and has an impurity concentration of approximately 10^{17} to 10^{18} impurities/cm³. Cathode region 24 is n+ type conductivity and is typically 2 microns thick, 48 microns wide, 44 microns long, and has an impurity concentration of approximately 10^{19} impurities/cm³ or larger. Electrode 32 is aluminum, $1\frac{1}{2}$ microns thick, 104 microns wide, and 104 microns long. The spacing between the ends of regions 18 and 22 and the respective ends of body 16 is typically 55 microns. The spacing between anode regions 18 and gate region 20 is typically 74 microns as is the spacing between gate region 20 and region 22. Region 34 is n+ type conductivity and is typically 2 microns thick, 26 microns wide, 26 microns long, and has an impurity concentration of 10^{19} impurities/cm³ or larger. Electrode 36 is aluminum which is $1\frac{1}{2}$ microns thick, 26 microns wide, and 26 microns long.

The embodiment described herein is intended to be illustrative of the general principles of the invention. Various modifications are possible consistent with the invention. For example, support member 12 can
5 alternatively be p type conductivity silicon, gallium arsenide, sapphire, a conductor, or an electrically inactive material. If region 12 is an electrically inactive material, then dielectric layer 14 can be eliminated. Still further, body 16 can be fabricated as
10 an air isolated structure. This allows for the elimination of support member 12. Further, the electrodes can be doped polysilicon, gold, titanium, or other types of conductors. Still further, the impurity concentration levels, spacings between different regions,
15 and other dimensions of the regions can be adjusted to allow significantly different operating voltages and currents than are described. Additionally, other types of dielectric materials, such as silicon nitride, can be substituted for silicon dioxide. Still further, the
20 conductivity type of all regions within the dielectric layer can be reversed provided the voltage polarities are appropriately changed. Still further, an electrical contact can be made to region 22. Dependent on the resistivity of region 22, the electrical contact thereto
25 could be made directly to region 22 or through a more highly doped semiconductor contact region added into a portion of region 22. Region 22 could then be used as a second gate region of structure 10. It is to be appreciated that the use of two of the structures of the
30 present invention with the cathode of one coupled to the anode of the other and the first gates 20 being common provides a bidirectional switch which allows alternating or direct current operation.



CLAIMS

1. A solid-state switching device comprising:
a semiconductor body having a major surface and a bulk
portion of a first conductivity type; first, second, and
5 third mutually separated regions of the semiconductor
body which each have a portion thereof common with the
major surface; a fourth region of the semiconductor body
which separates the third region from the bulk portion;
the second and third regions being of the first
10 conductivity type and being of lower resistivity than the
bulk portion of the semiconductor body; the first and
fourth regions being of a second conductivity type which
is opposite of the first conductivity type and being of
lower resistivity than the bulk portion of the semi-
15 conductor body; and the second region being located in
between the first and fourth regions.

2. A device as claimed in claim 1 wherein the
resistivity of the fourth region is intermediate between
that of the third region and that of the bulk portion of
20 the semiconductor body.

3. A device as claimed in claim 1 or claim 2
including separate electrical contacts to the first,
second and third regions.

4. A device as claimed in any of the preceding
25 claims wherein the semiconductor body is supported by a
semiconductor support member and electrically insulated
therefrom by a dielectric layer.

5. A structure comprising a plurality of devices
as claimed in claim 4 sharing a common semiconductor
30 support member.

6. A device as claimed in claim 4 or a structure
as claimed in claim 5 including a separate electrode
coupled to the semiconductor support member,

7. A solid-state switching device substantially
35 as herein described with reference to the accompanying
drawing.