CLAIMS

What is claimed is:

1. A memory device, comprising:

a first semiconductor structure comprising a memory cell array, wherein the memory cell array comprises a first memory bank and a second memory bank; and

a second semiconductor structure comprising a peripheral circuit, wherein the peripheral circuit comprises a first bank circuit and a second bank circuit arranged along a first direction, wherein the first bank circuit is coupled to the first memory bank and the second bank circuit is coupled to the second memory bank,

wherein the first bank circuit comprises a first driver circuit on a boundary of the first bank circuit, and the second bank circuit comprises a second driver circuit on a boundary of the second bank circuit, and

wherein at least a portion of the first driver circuit is adjacent to and overlaps with at least a portion of the second driver circuit along a second direction perpendicular to the first direction.

2. The memory device of claim 1, wherein the first semiconductor structure and the second semiconductor structure are stacked along a third direction perpendicular to the first direction and the second direction,

wherein the first memory bank overlaps with the first bank circuit in a plan view perpendicular to the third direction, and

wherein the second memory bank overlaps with the second bank circuit in the plan view.

3. The memory device of claim 2, wherein the first bank circuit comprises block circuits arranged in one or more rows, wherein the first driver circuit is comprised in a first block circuit that is closest to the second bank circuit among one row of block circuits of the first bank circuit, and

wherein the second bank circuit comprises block circuits arranged in one or more rows, wherein the second driver circuit is comprised in a second block circuit that is closest to the first bank circuit among one row of block circuits of the second bank circuit.

4. The memory device of claim 3, wherein the first block circuit further comprises first sense amplifiers coupled to bit lines in a memory block of the first memory bank, and

wherein the second bank circuit further comprises second sense amplifiers coupled to bit lines in a memory block of the second memory bank.

5. The memory device of claim 4, wherein positioning of the first driver circuit and the first sense amplifiers in the first block circuit is identical to positioning of the second driver circuit and the second sense amplifiers in the second block circuit.

6. The memory device of claim 3, wherein the first memory bank comprises a first memory block that is coupled to the first block circuit,

wherein the first block circuit further comprises a third driver circuit,

wherein the third driver circuit overlaps with the first memory block in the plan view, and the first driver circuit does not overlap with the first memory block in the plan view.

7. The memory device of claim 6, wherein word lines in the first memory block are numbered in a numerical order,

wherein the first bank circuit further comprises a fourth driver circuit and a fifth driver circuit,

wherein the first driver circuit and the third driver circuit are on a first boundary of the first block circuit and comprise a first set of word line drivers,

wherein the fourth driver circuit and the fifth driver circuit are on a second boundary of the first block circuit opposite to the first boundary, and comprise a second set of word line drivers, and

wherein an even-numbered word line in the first memory block is coupled to a corresponding word line driver of the first set of word line drivers, and an odd-numbered word line in the first memory block is coupled to a corresponding word line driver of the second set of word line drivers.

8. The memory device of claim 1, wherein the peripheral circuit comprises:

a third bank circuit adjacent to the second bank circuit along the first direction, wherein the third bank circuit is coupled to a third memory bank of the memory cell array; and

row decoders between the second bank circuit and the third bank circuit.

9. The memory device of claim 8, wherein the peripheral circuit comprises a fourth bank circuit adjacent to the third bank circuit along the first direction, wherein the fourth bank circuit is coupled to a fourth memory bank of the memory cell array,

wherein the third bank circuit comprises a sixth driver circuit on a boundary of the third bank circuit, and the fourth bank circuit comprises a seventh driver circuit on a boundary of the fourth bank circuit, and

wherein at least a portion of the sixth driver circuit is adjacent to and overlaps with at least a portion of the seventh driver circuit along the second direction.

10. The memory device of claim 1, wherein the memory cell array comprises DRAM memory cells.

11. The memory device of claim 1, wherein the first semiconductor structure and the second semiconductor structure comprise bonding contacts that bond the first semiconductor structure and the second semiconductor structure together, wherein the bonding contacts are isolated by an isolating material.

12. A method of forming a memory device, comprising:

forming a first semiconductor structure comprising a memory cell array, wherein the memory cell array comprises a first memory bank and a second memory bank; and

forming a second semiconductor structure comprising a peripheral circuit, wherein the peripheral circuit comprises a first bank circuit and a second bank circuit arranged along a first direction, wherein the first bank circuit is coupled to the first memory bank and the second bank circuit is coupled to the second memory bank,

wherein the first bank circuit comprises a first driver circuit on a boundary of the first bank circuit, and the second bank circuit comprises a second driver circuit on a boundary of the second bank circuit, and

wherein at least a portion of the first driver circuit is adjacent to and overlaps with at least a portion of the second driver circuit along a second direction perpendicular to the first direction.

13. The method of claim 12, comprising:

stacking the first semiconductor structure and the second semiconductor structure along a third direction perpendicular to the first direction and the second direction,

wherein the first memory bank overlaps with the first bank circuit in a plan view perpendicular to the third direction, and

wherein the second memory bank overlaps with the second bank circuit in the plan view.

14. The method of claim 13, wherein the first bank circuit comprises block circuits arranged in one or more rows, wherein the first driver circuit is comprised in a first block circuit that is closest to the second bank circuit among one row of block circuits of the first bank circuit, and

wherein the second bank circuit comprises block circuits arranged in one or more rows, wherein the second driver circuit is comprised in a second block circuit that is closest to the first bank circuit among one row of block circuits of the second bank circuit.

15. The method of claim 14, comprising:

forming first sense amplifiers in the first bank circuit, wherein the first sense amplifiers are coupled to bit lines in a memory block of the first memory bank; and

forming second sense amplifiers in the second bank circuit, wherein the second sense amplifiers are coupled to bit lines in a memory block of the second memory bank.

16. The method of claim 15, wherein positioning of the first driver circuit and the first sense amplifiers in the first block circuit is identical to positioning of the second driver circuit and the second sense amplifiers in the second block circuit.

17. The method of claim 14, wherein the first memory bank comprises a first memory block that is coupled to the first block circuit,

wherein the first block circuit further comprises a third driver circuit,

wherein the third driver circuit overlaps with the first memory block in the plan view, and the first driver circuit does not overlap with the first memory block in the plan view.

18. The method of claim 17, wherein word lines in the first memory block are numbered in a numerical order,

wherein the first bank circuit further comprises a fourth driver circuit and a fifth driver circuit,

wherein the first driver circuit and the third driver circuit are on a first boundary of the first block circuit and comprise a first set of word line drivers,

wherein the fourth driver circuit and the fifth driver circuit are on a second boundary of the first block circuit opposite to the first boundary, and comprise a second set of word line drivers, and

wherein an even-numbered word line in the first memory block is coupled to a corresponding word line driver of the first set of word line drivers, and an odd-numbered word line in the first memory block is coupled to a corresponding word line driver of the second set of word line drivers.

19. The method of claim 12, wherein forming the second semiconductor structure comprises:

forming a third bank circuit adjacent to the second bank circuit along the first direction, wherein the third bank circuit is coupled to a third memory bank of the memory cell array; and

forming row decoders between the second bank circuit and the third bank circuit.

20. A memory system, comprising:

a memory device comprising:

a first semiconductor structure comprising a memory cell array, wherein the memory cell array comprises a first memory bank and a second memory bank; and

a second semiconductor structure comprising a peripheral circuit, wherein the peripheral circuit comprises a first bank circuit and a second bank circuit arranged along a first direction, wherein the first bank circuit is coupled to the first memory bank and the second bank circuit is coupled to the second memory bank,

wherein the first bank circuit comprises a first driver circuit on a boundary of the first bank circuit, and the second bank circuit comprises a second driver circuit on a boundary of the second bank circuit, and

wherein at least a portion of the first driver circuit is adjacent to and overlaps with at least a portion of the second driver circuit along a second direction perpendicular to the first direction; and

a controller coupled to the memory device and configured to control the memory device.