WET ETCH SUITABLE FOR CREATING SQUARE CUTS IN SI AND RESULTING STRUCTURES

TECHNICAL FIELD

The present invention relates generally to methods for undercutting single crystal silicon using wet etchants. More particularly, the present invention relates to methods for creating square undercuts in single crystal silicon and resulting structures.

BACKGROUND

State of the Art: Higher performance, lower cost, increased miniaturization of semiconductor components, and greater packaging density of integrated circuits are ongoing goals of the computer industry. One way to reduce the overall cost of a semiconductor component is to reduce the manufacturing cost of that component. Lower manufacturing costs can be achieved through faster production as well as in reduction in the amount of materials used in fabricating the semiconductor component. In recent years, the semiconductor industry has greatly expanded its emphasis in development and production of electro-optical components, such as, for example, charge-coupled devices (CCDs) and, more recently, CMOS imagers. As with other semiconductor components, there is a continued drive toward higher performance parameters and greater yields at ever-lower costs.

Micro-electromechanical systems ("MEMS") is another technology receiving a great deal of attention in many industries, including the electronics industry. MEMS integrate microminiature electrical and mechanical components on the same substrate, for example, a silicon substrate, using microfabrication technologies to form extremely small apparatuses. The electrical components may be fabricated using integrated circuit fabrication ("IC") processes, while the mechanical components may be fabricated using micromachining processes that are compatible with the integrated circuit fabrication processes. This combination of approaches makes it possible, in many instances, to fabricate an entire microminiature system on a chip using conventional manufacturing processes. However, there remain many shortcomings in existing fabrication technologies which limit the types and sizes of MEMS components and assemblies which may be fabricated.

Conventional IC processing for DRAM, microprocessors, etc. are currently performed on (100) silicon. Potassium hydroxide and TMAH may be used to create vertical etches in (110) silicon by using (110) substrate wafers or causing the recrystallization of the surface of a substrate wafer to have a (110) crystal orientation. However, the resultant structures are not always desirable and may introduce costly, additional processing steps and procedures to the fabrication process and create a low performance device.

Various conventional chemistries have been used to etch silicon. For example, both single crystal and polycrystalline silicon are typically wet etched in mixtures of nitric acid (HNO_3) and hydrofluoric acid (HF). With use of such etchants, the etching is generally isotropic. The reaction is initiated by the HNO_3, which forms a layer of silicon dioxide on the silicon, and the HF dissolves the silicon oxide away. In some cases, water is used to dilute the etchant, with acetic acid (CH_3COOH) being a preferred buffering agent.

In some applications, it is useful to etch silicon more rapidly along one or more crystal planes relative to others. For example, in the diamond lattice of silicon, generally the (111) plane is more densely packed than the (100) plane, and thus the etch rates of (111) orientated surfaces are expected to be lower than those with (100) orientations. Bonding orientation of the different planes also contributes to etchant selectivity to exposed planes. One etchant that exhibits such orientation-dependent etching properties consists of a mixture of KOH and isopropyl alcohol. For example, such a mixture may etch about one hundred (100) times faster along (100) planes than along (111) planes.

Hydroxide etchants and TMAH may be used to create a vertical undercut in (100) silicon. FIGs. 1 and 2 show a silicon etch performed with different etchant solutions in both the standard silicon orientation (FIG. 1A and FIG. 2A) and 45° rotation (FIG. 1B and FIG. 2B). In the standard orientation, a mask is aligned along the <110> directions. The {111} planes define the sidewalls which are sloped from (100) surface plane. With the 45° rotation, the mask is aligned along the <100> direction. In FIG. 1, the etchant was dilute NH_4OH applied at 26° C and in FIG. 2, the etchant was dilute TMAH applied at 26° C. While the two etchants display different selectivity, both undercut the silicon 10 and create beveled edges or chamfers 12. The beveled edges may be undesirable for some applications and may limit the spacing of components on the integrated circuit.

Accordingly, it would be desirable to create square undercuts in (100) silicon without beveled edges, or chamfers and/or to manipulate the shape of the undercut. Further, it would be desirable to create a lateral shelf in (100) silicon using wet etch chemistry.

BRIEF DESCRIPTION OF DRAWINGS

In the drawings, which illustrate what is currently considered to be the best mode for carrying out the invention:

FIG. 1A is a cross-sectional view of single crystal silicon masked along the <110> direction and undercut with NH_4OH applied at 26° C. FIG. 1B shows of single crystal silicon masked along the <100> direction and undercut with NH_4OH applied at 26° C.

FIG. 2A is a cross-sectional view of single crystal silicon masked along the <110> direction and undercut with dilute TMAH applied at 26° C. FIG. 1B shows of single crystal silicon masked along the <100> direction and undercut with dilute TMAH applied at 26° C.

FIG. 3A is a cross-sectional view of single crystal silicon masked along the <110> direction and undercut with a buffered fluoride etch solution of the present invention applied at 23° C. FIG. 3B shows single crystal silicon masked along the <100> direction and undercut with a buffered fluoride etch solution of the present invention applied at 23° C.

FIGs. 4-11 show a single crystal silicon wafer at various stages in a fabrication process according to one embodiment of the present invention. FIG. 4A is a plan view of single crystal silicon wafer according to an embodiment of the present invention. FIG. 4B is a cross-sectional view of the same single crystal silicon wafer taken along line –4B – of FIG. 4A.

FIG. 5A is a plan view of single crystal silicon wafer according to an embodiment of the present invention. FIG. 5B is a cross-sectional view of the same single crystal silicon wafer taken along line –5B – of FIG. 5A.

FIG. 6A is a plan view of single crystal silicon wafer according to an embodiment of the present invention. FIG. 6B is a cross-sectional view of the same single crystal silicon wafer taken along line –6B – of FIG. 6A.

FIG. 7A is a plan view of single crystal silicon wafer according to an embodiment of the present invention. FIG. 7B is a cross-sectional view of the same single crystal silicon wafer taken along line –7B – of FIG. 7A.

FIG. 8A is a plan view of single crystal silicon wafer according to an embodiment of the present invention. FIG. 8B is a cross-sectional view of the same single crystal silicon wafer taken along line –8B – of FIG. 8A.

FIG. 9A is a plan view of single crystal silicon wafer according to an embodiment of the present invention. FIG. 9B is a cross-sectional view of the same single crystal silicon wafer taken along line –9B– of FIG. 9A.

FIG. 10A is a plan view of single crystal silicon wafer according to an embodiment of the present invention. FIG. 10B is a cross-sectional view of the same single crystal silicon wafer taken along line –10B– of FIG. 10A. FIG. 10C is a cross-sectional view of the single crystal silicon wafer of FIG. 10A taken along line –10C– of FIG. 10A.

FIG. 11A is a plan view of single crystal silicon wafer according to an embodiment of the present invention. FIG. 11B is a cross-sectional view of the same single crystal silicon wafer taken along line –11B– of FIG. 11A. FIG. 11C is a cross-sectional view of the single crystal silicon wafer of FIG. 11A taken along line –11C– of FIG. 11A. FIG. 11D is a cross-sectional view of the single crystal silicon wafer of FIG. 11A taken along line –11D– of FIG. 11A.

FIGs. 12A-E show a progressive undercut etch of single crystal silicon using a buffered fluoride etch solution of the present invention. The trenches are in the <100> direction on (100) silicon.

FIGs. 13A-D show a progressive undercut etch of single crystal silicon using a buffered fluoride etch solution of the present invention after exposure to NH_4OH. The trenches are in the <100> direction on (100) silicon.

FIGs. 14A-B show transmission electron micrographs (TEMs) of an integrated PSOI DRAM access structure.

MODES FOR CARRYING OUT THE INVENTION

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the

drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention.

The terms "wafer" and "substrate" as used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to those of ordinary skill in the art. The term "conductor" is understood to include semiconductors, and the term "insulator" is defined to include any material that is less electrically conductive than the materials referred to as conductors. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as "on," "side" (as in "sidewall"), "higher," "lower," "over" and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate.

There is a need in the industry, as recognized by the inventors herein, to undercut (100) silicon using wet etch chemistry. A buffered fluoride etch solution may be used to create square corners and lateral shelves in (100) silicon without the typical bevel experienced with hydroxide etches when the initial pattern is oriented along the <100> direction. The wet etch chemistry of the present invention may be used to fabricate devices that have previously been prohibitively expensive, complicated and/or poor yielding.

An embodiment of the present invention further includes methods employing etchant solutions to manipulate the cavity shape of a trench underlying single crystal silicon. Etch chemistry is highly selective to crystal orientation, when using (100) crystal plane orientation and patterning in a <100> direction, a cavity shape lacking beveled corners and including a lateral shelf may be achieved.

An embodiment of the present invention includes a method of etching the (100) crystal silicon plane 2-3 times slower than the (110) and (111) silicon planes. The etch rate of (100) silicon may be approximately 5-10,000Å/min and preferably 10-500Å/min in dilute etchants at low temperatures. The method may include exposing the silicon to a buffered fluoride etch solution of the present invention. The method may further include a simultaneous slower etch on an oxide and/or nitride relative to the (100) silicon.

In an embodiment of the present invention, a square undercut in single crystal silicon may be created by providing single crystal silicon including at least one trench therein, patterning the single crystal silicon in the <100> direction and exposing the single crystal silicon to a solution including a fluoride component, an oxidizing agent and an inorganic acid.

In an embodiment of the present invention, a lateral shelf may be created by exposing single crystal silicon to an anisotropic etchant followed by a buffered fluoride etch solution. Alternatively, a lateral shelf may be created by exposing single crystal silicon to a first isotropic etchant to create a trench. An anisotropic etchant may be applied to undercut the silicon and a buffered fluoride etch solution may be applied to square the corners of the undercut cavity. It will be understood that the buffered fluoride etch solution, which etches silicon at different rates in different exposed planes, may be used in the trench without a first anisotropic etchant.

An embodiment of the present invention includes a semiconductor device including single crystal silicon having a square undercut feature. The undercut feature includes smooth surfaces. An embodiment of the present invention includes a semiconductor device including single crystal silicon having a lateral shelf.

Etch compositions for oxidizing silicon and etching silicon dioxide to create desired structures according to the present invention shall be generally described below. With the description as provided below, it will be readily apparent to one skilled in the art that the buffered fluoride etch compositions described herein may be used in various applications. In other words, the buffered fluoride etch compositions may be used

whenever silicon etch is being performed and wherein square undercuts or lateral shelves are desired. For example, the present invention may be used in the formation of isolation structures for use in the fabrication of integrated circuits. Further, for example, the present invention may be beneficial in the fabrication of transistor structures, such as pseudo-silicon-on-insulator devices (including DRAM, SRAM, Flash, imagers, PCRAM, MRAM, CAM, etc.), FinFets, surround gate transistors, as well as micro electronic mechanical systems ("MEMS") and electro-optical components.

In one embodiment, a buffered fluoride etch composition for use in undercutting single crystal silicon to form lateral shelves generally includes a fluoride component, an inorganic acid and an oxidizing agent. The fluoride component may be, without limitation, HF, HF_2^-, NH_4F, or tetramethylammonium fluoride (TMAF). The ammonium fluoride may be formed with a mixture of ammonium hydroxide and HF. The fluoride component or solution is such that when the reaction of the etch composition with silicon forms silicon dioxide, the fluoride component or solution dissolves away the silicon dioxide formed thereby. The fluoride component may be present in the amount of 0.5-50% by weight.

The oxidizing agent of the buffered fluoride etch composition may be any oxidizing agent such as, for example, hydrogen peroxide or ozone. One currently preferred oxidizing agent is hydrogen peroxide.

The inorganic acid component may include at least one acid selected from hydrofluoric acid (HF), phosphoric acid (H_3PO_4), sulfuric acid (H_2SO_4), nitric acid (HNO_3), hydrochloric acid (HCl), carbonic acid (H_2CO_3), or any other suitable inorganic acid. It is currently preferred that the inorganic acid be H_3PO_4 or H_2CO_3. Inorganic acids are commercially available as concentrated solutions (X) which then typically are diluted to a desired concentration (H_2O:X). For example, commercially available concentrated acids are available as follows: HCl is 37% by weight in deionized water; HNO_3 is 70% by weight in deionized water; H_2SO_4 is 96% by weight in deionized water, and H_3PO_4 is 85% by weight in deionized water. Concentrations of etch compositions described herein are given based on commercially available solutions. For example, if the etch composition has a concentration of 30% HCl, then the solution includes 30% by weight of the commercially available HCl solution. Hydrogen peroxide (H_2O_2) is also commercially available as a concentrated solution of approximately 29% by weight in

deionized water. Further, ammonium fluoride is also commercially available as a concentrated solution, approximately 40% by weight in deionized water. Further, one will recognize that multiple components of the solution may be provided from commercially available solutions. For example, QEII available from Olin Microelectronics Materials (Newalk, Conn.) provides both NH_4F (~39.4 w%)and an inorganic acid (i.e., H_3PO_4 ~0.6 w %) that may be used to adjust the pH of the solution.

Other exemplary suitable etchants are disclosed in U.S. Patent No. 7,166,539 and U.S. Patent No. 6,391,793. The buffered fluoride etch solution preferably has a pH in the range of about 5.0 to about 9.0. More preferably, the buffered fluoride etch composition has a pH of about 7.8. Preferably, the buffered fluoride etch composition includes a fluoride component in a range of about 0.5 percent to about 50 percent by weight of the buffered fluoride etch composition, an oxidizing agent in the range of about 0.5 percent to about 30 percent by weight of the buffered fluoride etch composition; and an inorganic acid in the range of about 0.1-2% by weight. For example, the buffered fluoride etch composition may preferably include a volumetric ratio of NH_4F:QEII:H_2O_2 of about 4:2:3.

Further, preferably, the ionic strength of the buffered fluoride etch composition is greater than one; more preferably, the ionic strength is in the range of about 5 to about 20. As used herein, ionic strength refers to a measure of the average electrostatic interaction among ions in the composition which is equal to one-half the sum of the terms obtained by multiplying the molality of each ion by its valence squared. Yet further, preferably, the redox potential of the etch composition is in the range of about -0.5 to about +0.7 or higher (vs. Standard Hydrogen Electrode (SHE)). As used herein, the redox potential is a measure of the effectiveness of the etch composition as an oxidizing agent, *i.e.*, the ability of the etch composition to oxidize silicon for removal by the HF component of the etch composition.

The above ranges for the buffered fluoride etch solution are particularly applicable to the use of ammonium fluoride and hydrogen peroxide but appear to be equally applicable to buffered fluoride etch compositions having other combinations of components as described above, such as when ammonium fluoride is provided by ammonium hydroxide and hydrofluoric acid. In other words, suitable amounts of ammonium hydroxide and hydrofluoric acid may be mixed to provide an adequate amount

of ammonium fluoride. When ozone is used as the oxidizing agent, ozone is preferably present in a range of about 1 parts per million (ppm) to about 50 ppm.

The buffered fluoride etch solution may exhibit an etch rate of silicon that is greater than 3 times the etch rate of an oxide being exposed to the same etch composition, *i.e.*, the selectivity between silicon and oxide is greater than 3. More preferably, the selectivity between silicon and oxide using the etch composition is greater than 6 compared to <100> silicon etch rate.

Further, to achieve desired throughput of wafers, the etch rate for silicon using the etch composition is preferably greater than about 5 Å/min. More preferably, the etch rate for silicon is greater than 18 Å /min. Even more preferably, the etch rate for silicon is greater than 30-50Å per minute.

Preferably, the etch composition is such that after removal of silicon using the etch composition the silicon surface has a desired surface roughness adequate for later processing. Preferably, the roughness of the silicon surface following the etch is within the range of about 1.25 Å RMS to about 1.30 Å RMS. The silicon surface may desirably fall within such a range for roughness after more than 180 Å of silicon is removed. Generally, for example, roughness may be determined by Atomic Force Microscopy (AFM) which scans a surface area of about 1 μm^2 and gives an average peak-to-valley measurement across this 1 μm^2 surface area, rms.

Preferably, the high selectivity to oxide as described above is a high selectivity to thermal oxide. For example, such thermal oxide may be formed by thermal oxidation such as with use of a wet or dry furnace oxidation. However, such selectivity is also applicable to oxides formed by chemical vapor deposition (CVD), such as high density plasma oxide typically used in isolation processes, such as shallow trench isolation.

Generally, any known method may be used to expose the silicon to the buffered fluoride etch solution. For example, the silicon may be immersed into a tank of the buffered fluoride etch solution. The solution may also be sprayed onto the wafers being etched or may be introduced for contact with the wafer in any other manner, *e.g.*, drip, spraying, vapor, etc. The etching process may be performed at a temperature in the range of about 10° C. to about 90° C. Preferably, the etching process occurs at a temperature between 21° C. to about 30° C and, more preferably, between about 22° C and 25° C.

As previously described herein, FIGs. 1 and 2 show that when NH_4OH or TMAH is used to undercut silicon, virtually no lateral shelf is formed. When performed at a 45° rotation (i.e., patterned along the <100> direction) the corners of the undercut structure have chamfers 12. (FIG. 1B and FIG. 2B). These resulting structures are undesirable for many manufacturing processes. Referring to FIG. 3 a silicon 10 undercut was performed in both the standard silicon orientation (i.e., patterned along the <110> direction) and 45° rotation in (100) silicon using a buffered fluoride etch solution (10L NH_4F + 5L QEII + 7.5L H_2O_2) at 26° C according to the present invention. The buffered fluoride etch solution used in FIG. 3 demonstrates that the (100) silicon planes is the slow etching planes which allows the creation of square undercuts if the pattern is aligned along the <100> direction. In a typical hydroxide-based etch, the (111) plane is a slow etch; thus, it was surprising to discover a wet etch with a slow plane etch in (100) silicon.

The buffered fluoride etch solution provides very useful selectivity, smooth surfaces and controllable etching of (100) silicon. Referring to FIG. 3B, the lateral shelf 14 and lack of beveled corners enables the easy creation thereon of electrical devices such as FinFETs, Pseudo-SOI or RAD bowls in standard CMOS wafers which are manufactured on (100) silicon. The use of the buffered fluoride etch solution also creates concave square corners without a lateral spacer which is desirable for electronic properties in silicon fingers of sheets which have very different properties from the adjacent material having no material etched. The concave square corners depicted in FIG. 3B are also useful for a discrete change in device mechanical and optical properties when fabricating MEMS. The concave corner in (100) silicon also allows simple integration in CMOS devices and enables MEMS mechanical and optical structures to be integrated with CMOS processing more easily.

The etch rate and selectivity of the buffered fluoride etch solution depends on two competing mechanisms – the oxidation of silicon and the etch rate of oxide. This may be depicted in the following simplified reactions:

$$Si + 2\,H_2O_2 = H_2SiO_3 + H_2O = SiO_2 + 2\,H_2O \qquad (1)$$

Half-cell reduction/oxidation reactions:

$$H_2O_2 + 2\,H^+ + 2e^- \leftrightarrow 2\,H_2O \qquad E^{0'} = +1.77\ V \qquad (2)$$

$$Si_s + 2\,OH^- \leftrightarrow = Si(OH)_2 + 2e^- \qquad (3)$$

$$H_2SiO_3 + 6\,HF \leftrightarrow H_2SiF_6 + 3\,H_2O \quad (4)$$

The typical selectivity between (100) silicon crystal orientation and thermal oxide is approximately 6. The (110) directional etch is approximately two and one half times higher than (100) silicon etch.

Although the buffered fluoride etch solution may be used in various applications, FIGs. 4-11 depict a partial process for creating a pseudo-SOI structure according to a method of the present invention. In each of FIGs. 4-11, part A shows a plan view of the structure and part B shows a cross-sectional view of the corresponding structure taken along -- B --. FIG. 4A and B depict a single crystal silicon substrate 100. A silicon nitride liner 112 is formed thereover. A masking layer 128, for example, photoresist, is formed over the silicon nitride liner 112 as known in the art. The masking layer 128 may be patterned to form at least one trench mask opening 132. Conventional photolithography or other lithographic or non-lithographic methods, regardless of the presence of the masking layer 128, are also contemplated.

Referring to FIGs. 5A and 5B, the silicon nitride liner 112 and single crystal silicon substrate 100 are etched through the mask opening 132 to form at least one trench 116 within the single crystal silicon substrate 100. The etch may be conducted utilizing a dry anisotropic etching chemistry, with or without plasma, for example comprising ammonia and at least one fluorocarbon. Masking layer 128 may remain or may be removed when etching into the single crystal silicon substrate 100. While a specific method of forming trench 116 has been disclosed, it will be understood by one of skill in the art that any method of forming trench 116 may be utilized.

Referring to FIGs. 6A and 6B, a nitride layer may be deposited over the silicon nitride liner 112 and trench 116 followed by an etch which removes the nitride from the bottom 126 of the trench 116, but creates nitride spacers 118 on the sidewalls 130 of trench 116. Creation of the Si_3N_4 liner may be performed by conventional techniques.

The buffered fluoride etch solution of the present invention may then be applied to undercut the single crystal silicon substrate 10. Preferably, the buffered fluoride etch solution may be applied at approximately 23° C for approximately 5 minutes, depending on the desired size of the lateral shelf 114. As shown in FIGs. 7A and 7B, the buffered fluoride etch solution etches faster in a direction parallel to the single crystal silicon

substrate 100 as compared with the vertical etch through the bottom 126 of the trench 116. A lateral shelf 114 having a thickness of approximately 450 Å to 550 Å may be created as shown in FIG. 7 B.

If desired, a nitride liner 120 may be deposited on the bottom 126 and sidewalls 130 of the trench 116 and then the trench 116 may be filled with an oxide material 122, for example, a spin-on-dielectric (SOD) as shown in FIGs. 8A and B.

A mask 124 is deposited and patterned over the silicon nitride liner 112 and oxide material 122. A conventional silicon etch having some selectivity to oxide may be performed as shown in FIGs. 9A, B and 10A, B, C.

An optional nitride liner 136 may be deposited and an SOD fill may be performed as shown in FIGs. 11A, B, C and D. After the SOD fill depicted in FIG. 11, the structure 150 may be subjected to further processing to form, for example, transistors, capacitors and digit lines thereover to complete the pseudo-SOI structure. The structure 150 includes a lateral shelf 114 having a thickness of about 500Å (+/- 10%).

The resulting structure, including any transistors, such as array transistors or access transistors, overlying structure 150, has significantly lower leakage due to the presence of oxide material 122 underlying the silicon. (*see*, e.g., FIG. 11B). It will be understood that structure 150 is not limited to being an intermediate pseudo-SOI structure. Any number of additional fabrication steps may be performed in conjunction with the present invention to create any desired device.

FIGs. 12A-E depict silicon oxidation and etching using a solution of NH_4F, QEII and H_2O_2 (provided in a ratio of 4:2:3). The substrate was immersed in a stagnant bath of the NH_4F, QEII and H_2O_2 solution at 23° C. FIG. 12A depicts a trench 310 in single crystal silicon 300 with a nitride liner 320 prior to addition of the buffered fluoride etch solution of the present invention. The top surface 312 of the single crystal silicon represents the (100) plane. The trench 310 is <110> on the (100) plane. After 16 minutes of exposure to the buffered fluoride etch solution at approximately 23° C, an undercut profile is visible having a lateral shelf 314. (FIG. 12B) The etch is progressing faster perpendicular to the (100) direction (i.e., perpendicular to the STI sidewall), than in the (100) direction (i.e., perpendicular to the wafer surface) as shown in FIGs. 12C, D and E after 22 min, 25 min and 28 min exposure, respectively. As seen in FIGs. 12A-E, the

width of the underlying silicon leg, or pillar, 350, decreases with increased exposure to the buffered fluoride etch solution.

The buffered fluoride etch solution may be combined with other components in combination with pattern angles to manufacture vertical walls in various ways. FIG. 13A-D depicts the etch progression of single crystal silicon 400 at 0 min (FIG. 13A), 3 min (FIG. 13B), 6 min (FIG. 13C) and 9 min (FIG. 13D) exposure to the NH_4F, QEII and H_2O_2 solution (the buffered fluoride etch solution) after a five minute anisotropic NH_4OH etch at 23° C. Exposure occurred using a stagnant bath. The top surface 412 of the single crystal silicon represents the (100) plane. The trench 410 is <110> on the (100) plane. Increasing the time of the buffered fluoride etch solution etch forms a shelf undercut of the silicon active area without significantly increasing the trench depth. Further, it can be seen that the silicon legs, or pillars, 450 under the single crystal silicon 400 becomes increasingly narrow as the etch progresses. Thus, it will be understood that using appropriate pattern angles in combination with etchant solutions of the present invention, devices may be manufactured having various characteristics. By manipulating the etch time and etchant combination, different undercut profiles may be achieved. For example, the buffered fluoride etch solution may be combined with hydroxides, NH_4OH, NH_4F, TMAH or combinations thereof.

The invention may further be understood by the following non-limiting examples.

EXAMPLE 1

FIGs. 14A and B depict two TEMs of an integrated PSOI DRAM access structure. The profile was created by the combination of a TMAH (100:1) etch of 4 minutes 36 seconds at 25° C. A second etch using the buffered fluoride etch solution (NH_4F, QEII and H_2O_2 (provided in a ratio of 4:2:3) was run at 25° C for 6 minutes. A conventional oxide spacer was used for the two wet etches and removed after the cavity creation. The image is shown in the <100> direction after the access transistors and bit line were integrated along with poly-silicon plugs between the transistor gates.

All documents cited herein are incorporated in their entirety as if each were incorporated separately. This invention has been described with reference to illustrative embodiments and is not meant to be construed in a limiting sense. As described previously, one skilled in the art will recognize that various other illustrative applications may utilize the etch compositions described herein. Various modifications of the

illustrative embodiments, as well as additional embodiments of the invention, will be apparent to persons skilled in the art upon reference to this description. While the preferred embodiments of the present invention have been described herein, the invention defined by the claims herein is not limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A method of creating a square undercut in single crystal silicon, the method comprising:

patterning a single crystal silicon having at least one trench therein in the <100> direction; and

introducing the single crystal silicon to a solution including a fluoride component, an oxidizing agent and an inorganic acid.

2. The method of claim 1, further comprising selecting the fluoride component to be ammonium fluoride formed from ammonium and hydrofluoric acid.

3. The method of claim 1, further comprising introducing the single crystal silicon to the solution at a temperature of about 10° C. to about 90° C.

4. The method of claim 1, further comprising introducing the single crystal silicon to a solution including a fluoride component, an oxidizing agent and an inorganic acid, wherein the solution includes a pH of about 5.8 to about 9.8.

5. The method of claim 1, wherein patterning single crystal silicon having at least one trench therein comprises exposing the single crystal silicon to an anisotropic etchant to form at least one trench therein.

6. The method of claim 5, further comprising selecting the anisotropic etchant from the group consisting of tetramethylammonium fluoride, ammonium fluoride, and ammonium hydroxide.

7. The method of claim 1, further comprising selecting the fluoride component from the group consisting of hydrogen fluoride, ammonium fluoride and tetramethylammonium fluoride.

8. The method of claim 1, further comprising selecting the inorganic acid from the group consisting of hydrofluoric acid, phosphoric acid, sulfuric acid, nitric acid, hydrochloric acid and carbonic acid.

9. The method of claim 1, further comprising selecting the oxidizing agent from the group consisting of hydrogen peroxide, ozone and ammonium perfluorate.

10. The method of claim 1, wherein introducing comprises immersing the single crystal silicon in bath including NH_4F, H_2O_2 and QEII in a volumetric ratio of about 4:2:3.

11. The method of claim 1, wherein introducing comprises immersing the single crystal silicon in bath including approximately 10-35 w% NH_4F, approximately 3-20 w% $_2O_2$, approximately 0.1-2 w% H_3PO_4 or other acid, and approximately 43 - 86.9 w% deionized water.

12. The method of claim 1, wherein introducing the single crystal silicon to a solution comprises etching the (100) plane of the single crystal silicon more slowly than either the (110) or the (111) planes of the single crystal silicon.

13. A semiconductor device structure comprising single crystal silicon including a square undercut feature.

14. The semiconductor device structure of claim 13, further comprising a nitride spacer on at least a portion of a top surface of the single crystal silicon substrate and at least partially extending into the square undercut feature.

15. The semiconductor device structure of claim 13, wherein the single crystal silicon comprises a lateral shelf.

16. The semiconductor device structure of claim 13, wherein the single crystal silicon has a top surface comprising (100) silicon.

17. The semiconductor device structure of claim 13, wherein the square undercut feature comprises at least one undercut trench formed in the single crystal silicon substrate and including a first trench wall substantially perpendicular to a surface of the single crystal silicon substrate and a second trench wall substantially parallel to the surface of the single crystal silicon substrate.