

ELIMINATION OF SOI PARASITIC BIPOLAR EFFECT

ABSTRACT

There is disclosed a circuit (300) implemented in SOI (silicon on insulator) CMOS, which includes a first node precharged to an activated level, a first transistor (325) coupled between the first node (312) and the second node, a second transistor (326) coupled between the second node (313) and a ground potential, and a third transistor (327) coupled to the second node and operable for preventing the second node from rising to the activated level. The third transistor prevents the parasitic bipolar effect from raising this second node to the activated level. Essentially, the third transistor maintains the second node substantially at a ground level.

Fig.3