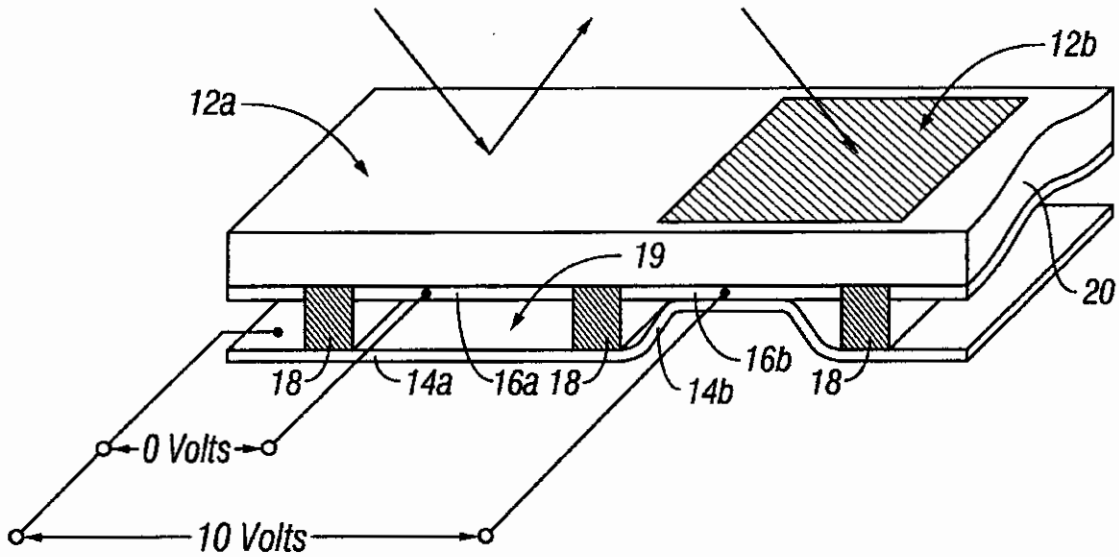


FIG. 1

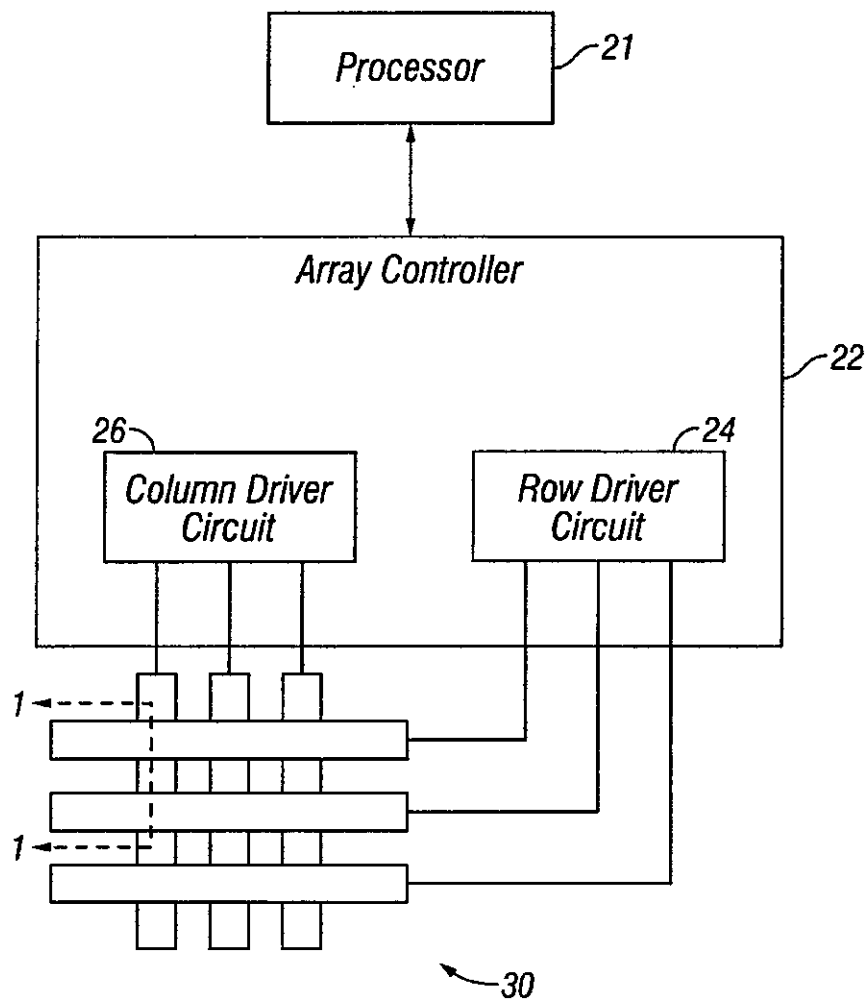

Processor
21
Array Controller
22
26
Column Driver Circuit
24
Row Driver Circuit
1
1
30

FIG. 2

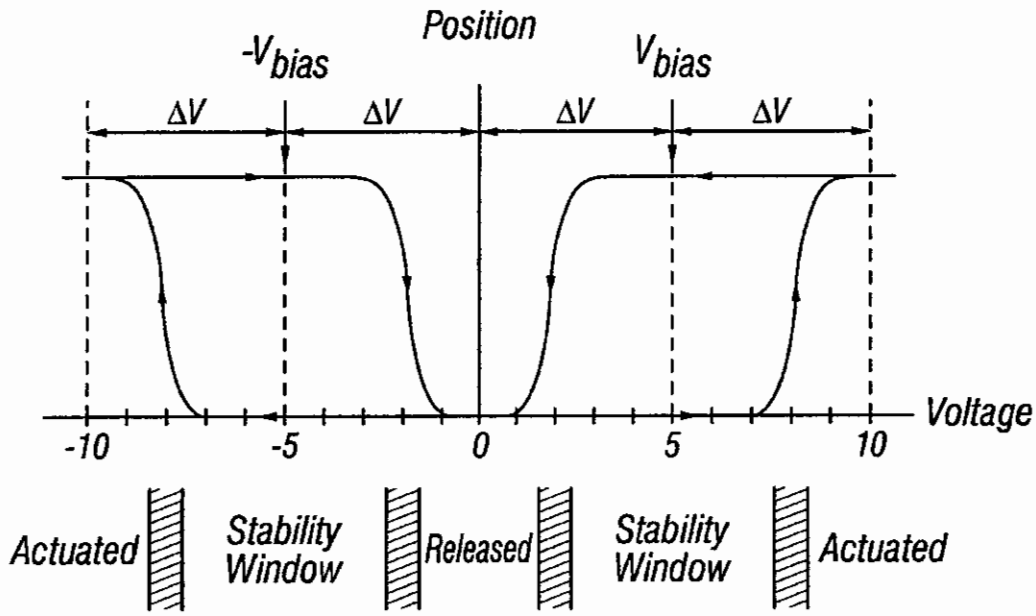


FIG. 3

Row Output Signals	Column Output Signals: $+V_{bias}$	Column Output Signals: $-V_{bias}$
0	Stable	Stable
$+\Delta V$	Release	Actuate
$-\Delta V$	Actuate	Release

FIG. 4

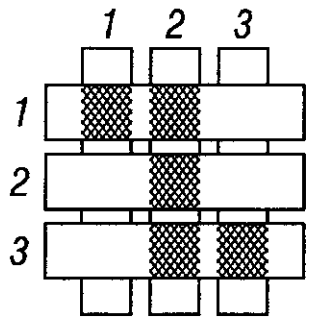

1
2
3
1
2
3

FIG. 5A

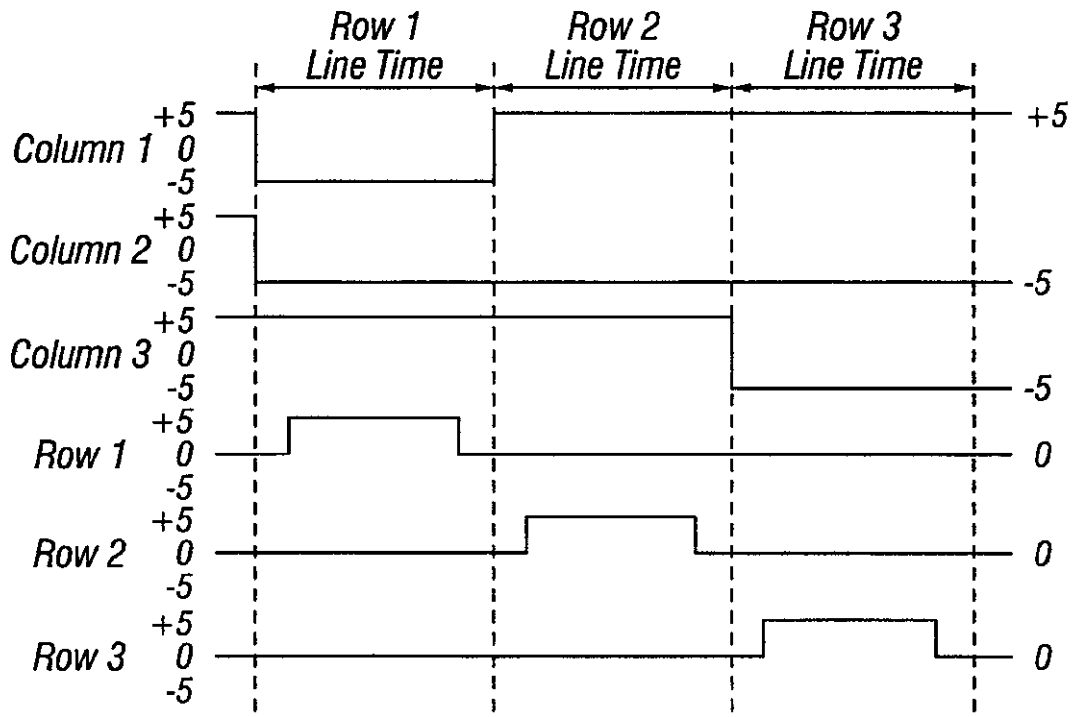

Row 1
Line Time
Row 2
Line Time
Row 3
Line Time
Column 1
Column 2
Column 3
Row 1
Row 2
Row 3
+5
0
-5
+5
-5
-5
0
0
0

FIG. 5B

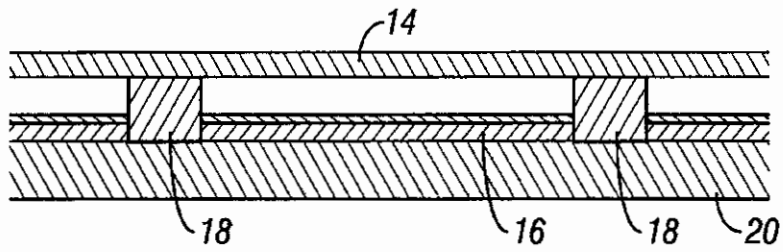


FIG. 6A

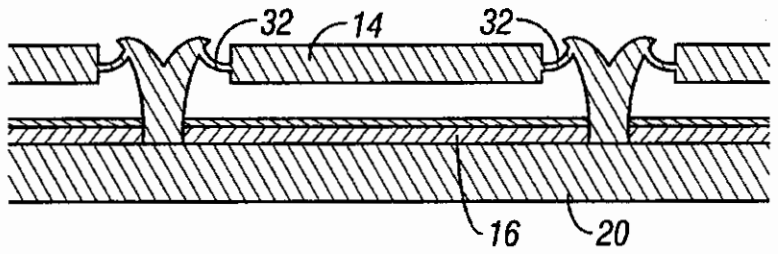


FIG. 6B

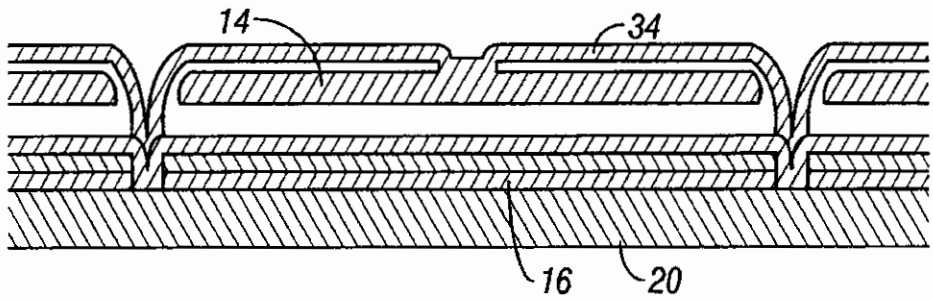


FIG. 6C

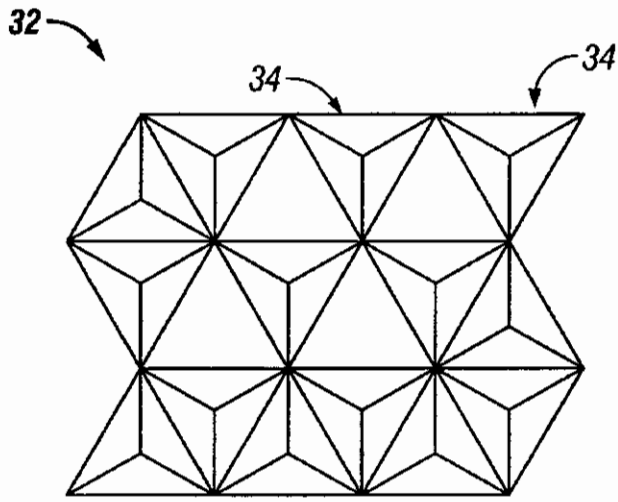


FIG. 7

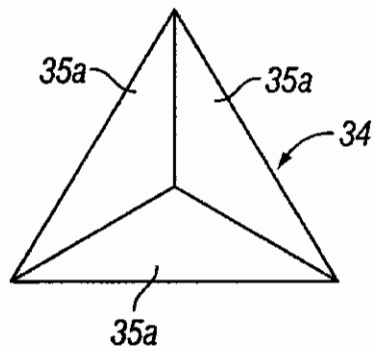


FIG. 7A

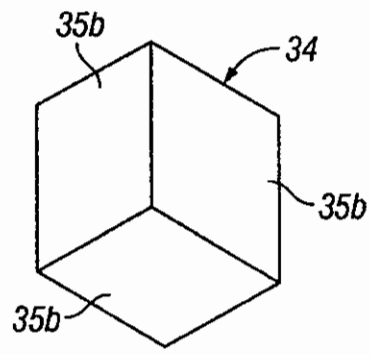


FIG. 7B

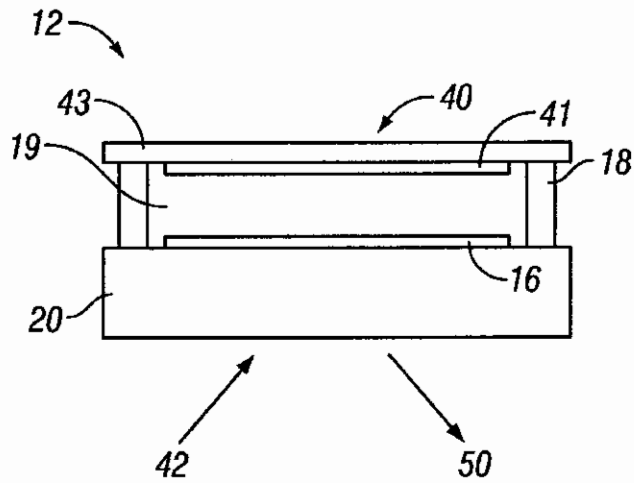


FIG. 8A

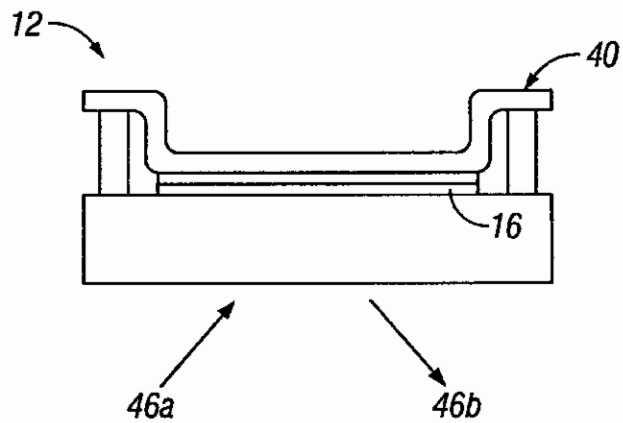


FIG. 8B

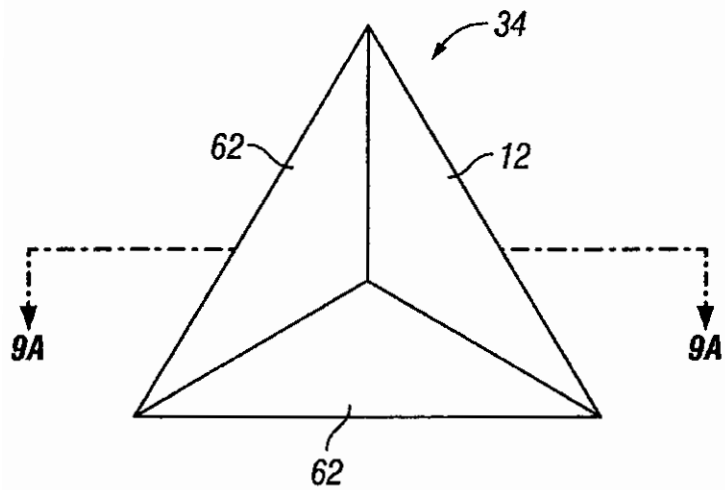


FIG. 9

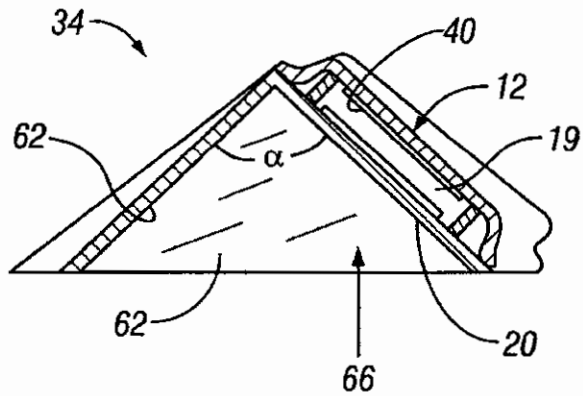


FIG. 9A

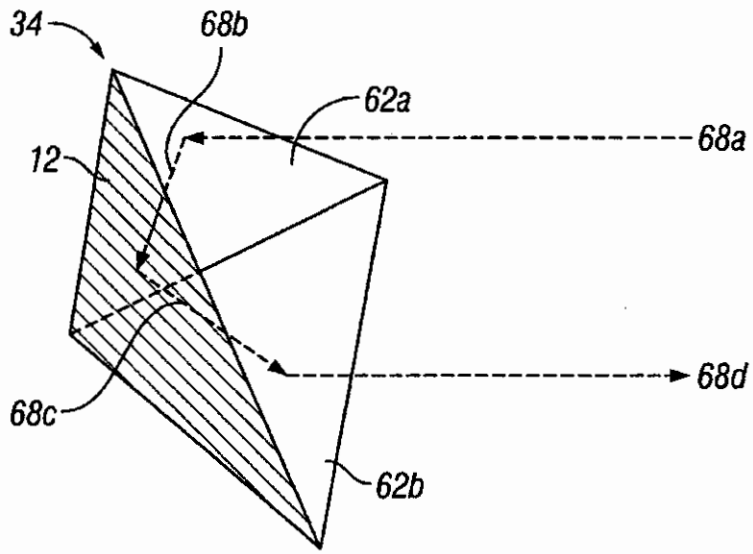

34
68b
62a
68a
12
68d
68c
62b

FIG. 9B

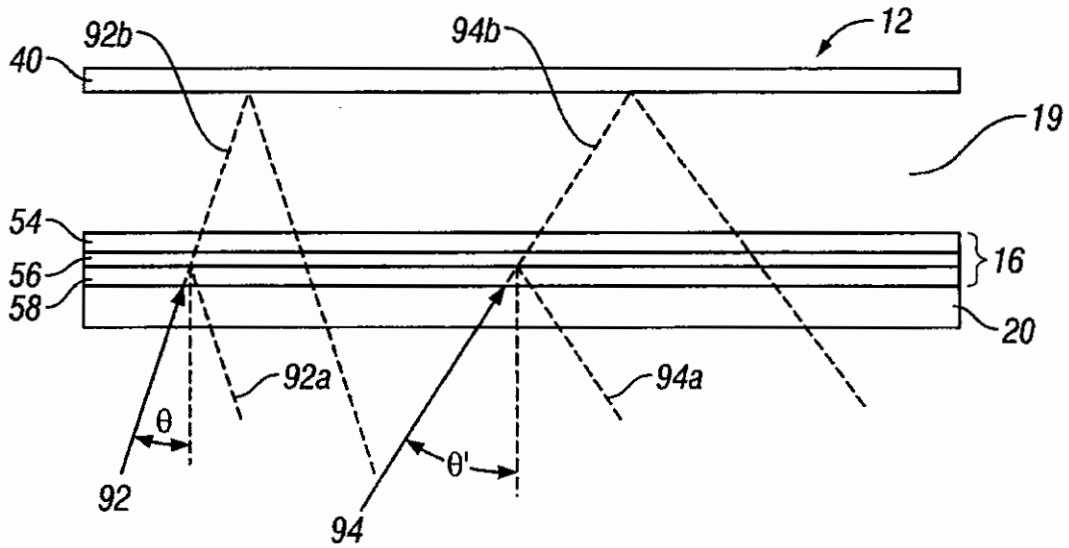

92b
94b
12
40
19
54
56
58
16
20
92a
94a
θ
θ'
92
94

FIG. 10

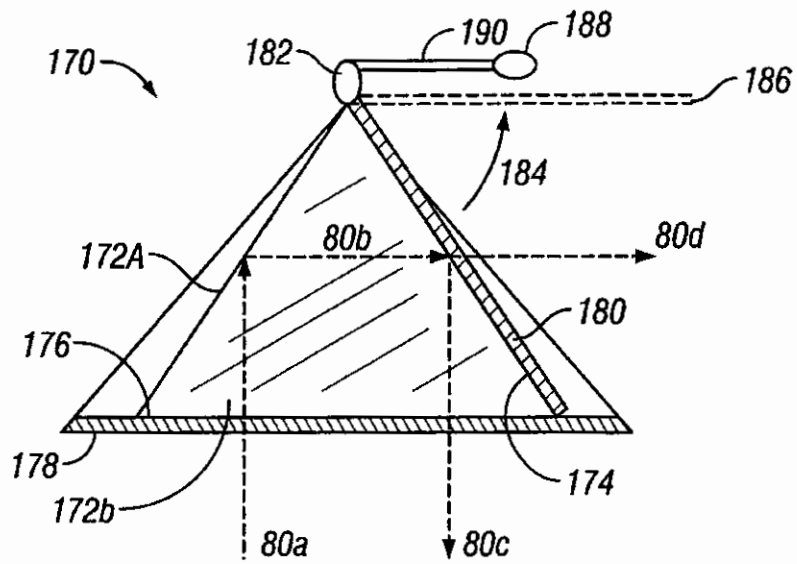

170
182
190
188
186
184
80b
80d
172A
180
176
178
172b
174
80a
80c

FIG. 11

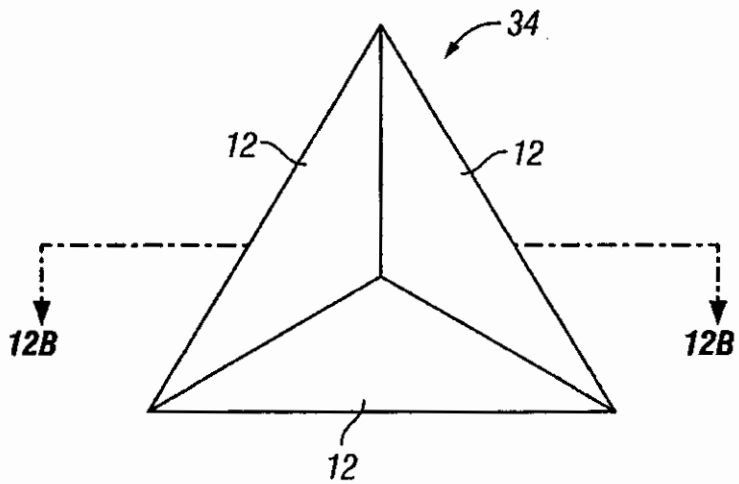

34
12
12
12B
12B
12

FIG. 12

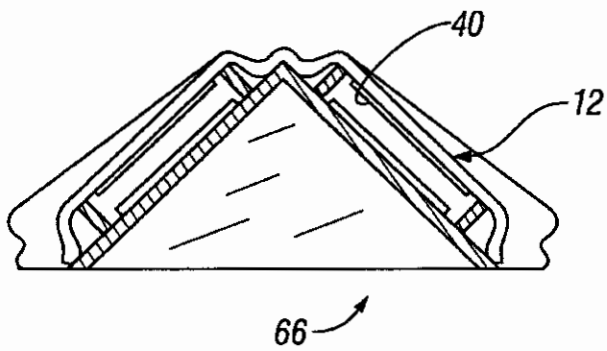


FIG. 12A

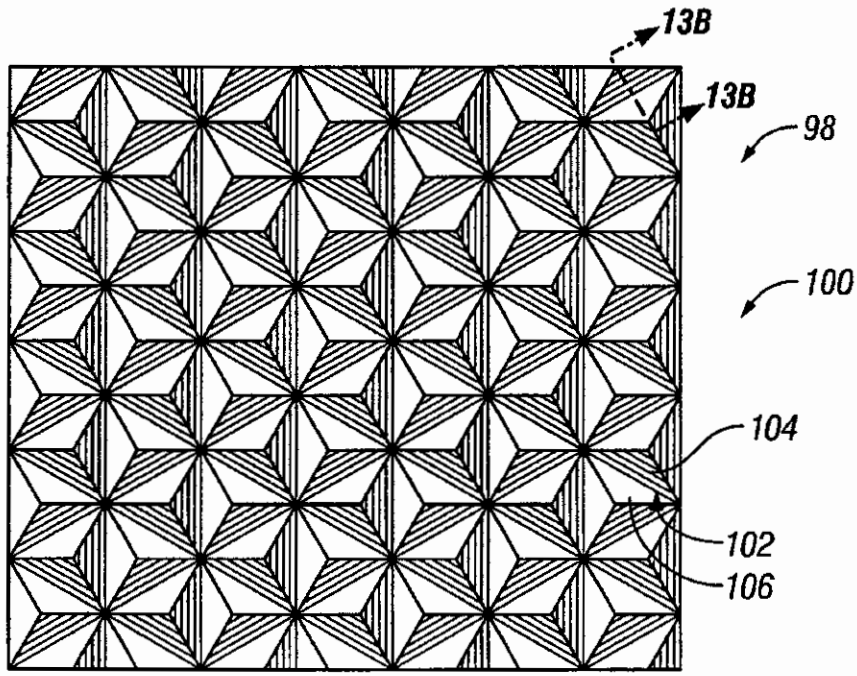


FIG. 13A

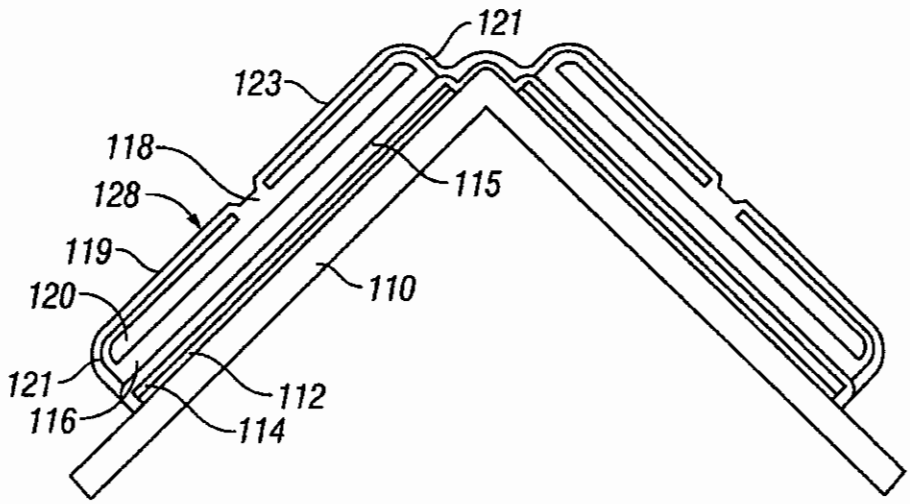


FIG. 13B

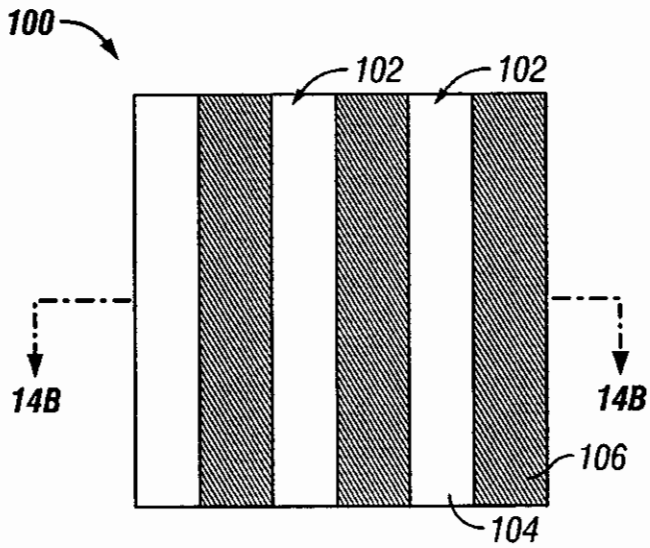


FIG. 14A

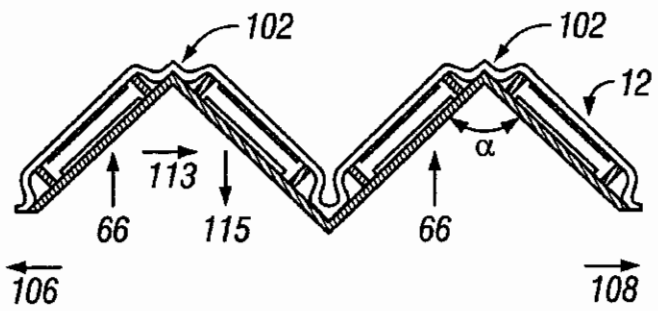


FIG. 14B

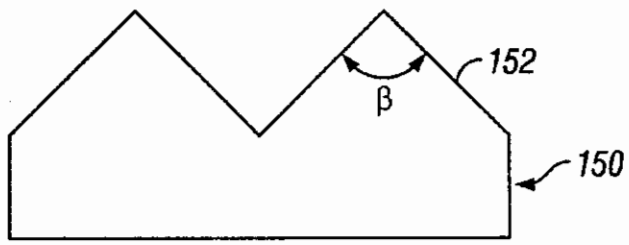


FIG. 15A

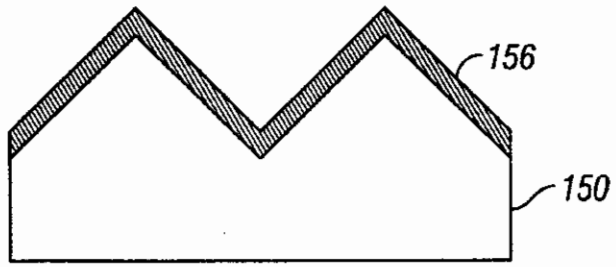


FIG. 15B

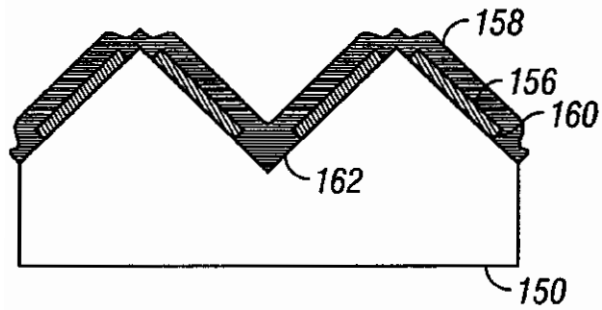


FIG. 15C

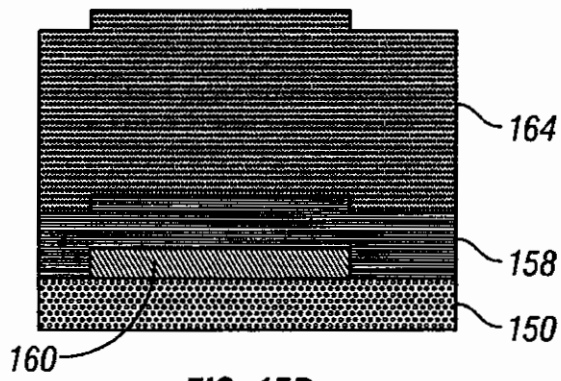


FIG. 15D

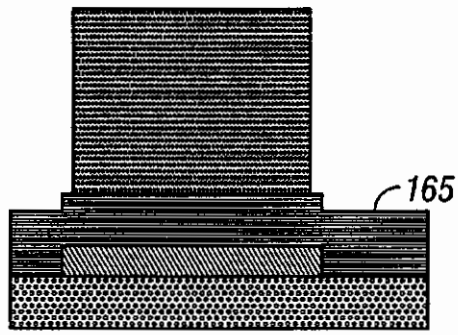


FIG. 15E

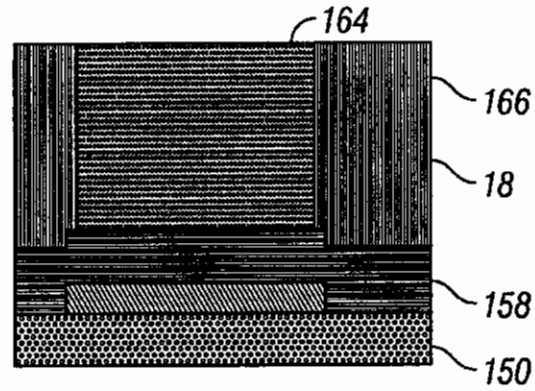


FIG. 15F

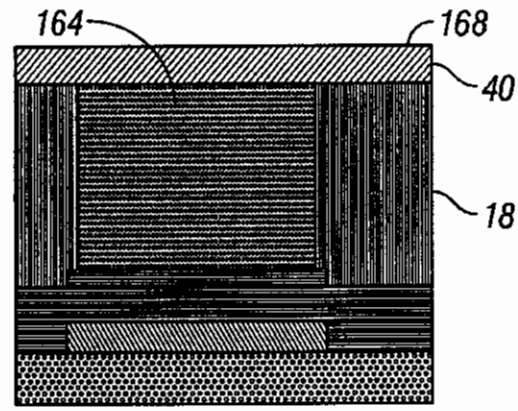


FIG. 15G

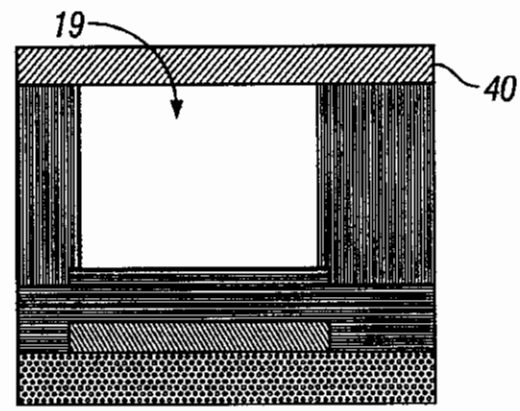


FIG. 15H

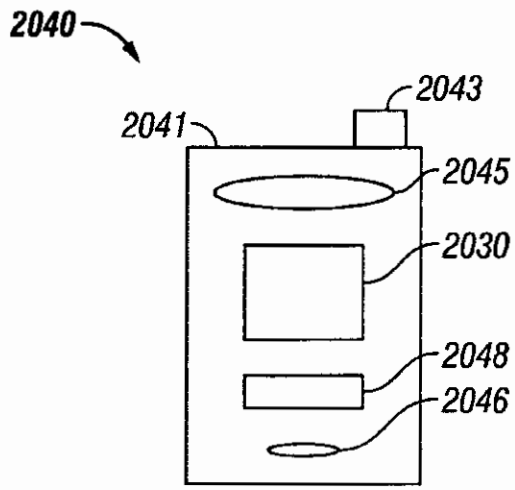


FIG. 16A

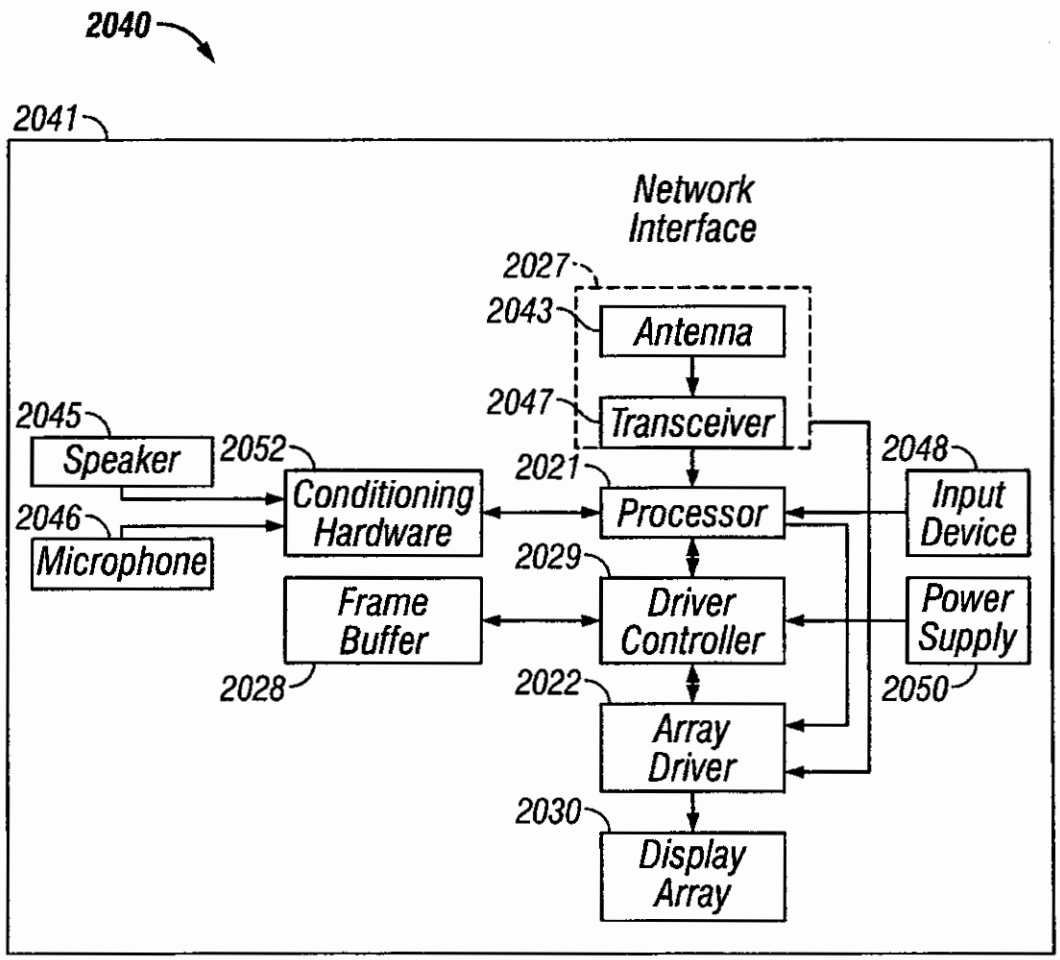


FIG. 16B