

PRE-BONDING AUTOMATIC OPTICAL INSPECTION DEFECT CLASSIFICATION

FIELD

[0001] Embodiments of the present principles generally relate to detecting and quantifying chipping defects in diced wafers and in particular to the automatic optical inspection of diced wafers to automatically detect and quantify chipping defects on wafers caused by, for example, a dicing process.

BACKGROUND

[0002] In the context of manufacturing integrated circuits, wafer dicing is the process by which dies are separated from a wafer of semiconductor following the processing of the wafer. The dicing process can involve scribing and breaking, mechanical sawing and other forms of cutting. However, in some instances, during the dicing process, chipping can occur on the wafer. That is, the cutting/removal of wafer material via abrasive force can cause chipping to occur at the groove edges of the wafer because wafer material is typically brittle.

[0003] There currently exist manual processes for detecting and measuring the chipping defects of a wafer. For example, in some instances a process engineer can implement an image capture device, such as an optical profiler tool, which can focus on an area of a diced wafer (i.e., a quadrant of the diced wafer) with great precision. Using the optical tool, the process engineer can draw a line of measurement to evaluate any chipping deviations across each section of the quadrant of the wafer. Such manual measurement of the chipping deviations, however, is a cumbersome process and is error prone due to human perspective, i.e., the measurement line is drawn from the engineer's point of view.

[0004] What is needed is a process for the automatic optical inspection of diced wafers to automatically detect and quantify chipping defects on wafers.

SUMMARY

[0005] Methods, apparatuses and systems for the automatic detection and measurement of chipping defects on diced wafers are provided herein.

[0006] In some embodiments a method for the automatic detection and measurement of chipping defects on diced wafers includes receiving an image of at least a portion of a diced wafer, aligning the received image of the at least the portion of the diced wafer, determining edges of the at least the portion of the diced wafer depicted in the aligned, received image, automatically determining at least one baseline from which to measure chipping defects on the at least the portion of the diced wafer from the determined edges, and measuring chipping defects on the at least the portion of the diced wafer using at least one determined, respective baseline.

[0007] In some embodiments the method can further include aligning the received image along a vertical axis. In some embodiments, the method can further include aligning the received image along a horizontal axis.

[0008] In some embodiments, the method can further include determining a reference axis line, and aligning the received image along the determined, reference axis line.

[0009] In some embodiments, the method can further include measuring chipping defects as a distance from the determined respective baseline to an end of a chipping defect.

[0010] In some embodiments, the method can further include applying a machine learning model to measured chipping defects to determine if a critical failure exists on the diced wafer. In some embodiments, the machine learning model is trained to recognize measured chipping defects that result in a critical failure of the diced wafer.

[0011] In some embodiments, an apparatus for the automatic detection and measurement of chipping defects on diced wafers includes a processor and a memory coupled to the processor. In some embodiments, the memory has stored therein at least one of programs or instructions executable by the processor to configure the

apparatus to receive an image of at least a portion of a diced wafer, align the received image of the at least the portion of the diced wafer, determine edges of the at least the portion of the diced wafer depicted in the aligned, received image, automatically determine at least one baseline from which to measure chipping defects on the at least the portion of the diced wafer from the determined edges, and measure chipping defects on the at least the portion of the diced wafer using the at least one determined baseline.

[0012] In some embodiments, the apparatus is configured to align the received image along at least one of a vertical axis or a horizontal axis.

[0013] In some embodiments, the apparatus is further configured to determine a reference axis line, and align the received image along the determined, reference axis line.

[0014] In some embodiments, the apparatus is configured to measure chipping defects as a distance from the determined respective baseline to an end of a chipping defect.

[0015] In some embodiments, the apparatus is further configured to apply a machine learning model to measured chipping defects to determine if a critical failure exists on the diced wafer. In such embodiments, the machine learning model is trained to recognize measured chipping defects that result in a critical failure of the diced wafer.

[0016] In some embodiments, a system for the automatic detection and measurement of chipping defects on diced wafers includes an image capture device for capturing images of at least a portion of a diced wafer, and an apparatus including a processor and a memory. In some embodiments, the memory has stored therein at least one program, the at least one program including instructions which, when executed by the processor, cause the system to perform a method including capturing an image of at least a portion of a diced wafer using the image capture device, and aligning the captured image of the at least the portion of the diced wafer, determining edges of the at least the portion of the diced wafer depicted in the aligned, received image, automatically determining at least one baseline from which to measure

chipping defects on the at least the portion of the diced wafer from the determined edges, and measuring chipping defects on the at least the portion of the diced wafer using at least one determined, respective baseline, using the apparatus.

[0017] In some embodiments, the method performed by the system further includes aligning captured images along at least one of a vertical axis or a horizontal axis.

[0018] In some embodiments, the method performed by the system further includes determining a reference axis line, and aligning the captured images along the determined, reference axis line.

[0019] In some embodiments, the method performed by the system further includes measuring chipping defects as a distance from the determined respective baseline to an end of a chipping defect.

[0020] In some embodiments, the method performed by the system further includes applying a machine learning model to measured chipping defects to determine if a critical failure exists on the diced wafer. In such embodiments, the machine learning model is trained to recognize measured chipping defects that result in a critical failure of the diced wafer

[0021] Other and further embodiments of the present disclosure are described below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] Embodiments of the present disclosure, briefly summarized above and discussed in greater detail below, can be understood by reference to the illustrative embodiments of the disclosure depicted in the appended drawings. However, the appended drawings illustrate only typical embodiments of the disclosure and are therefore not to be considered limiting of scope, for the disclosure may admit to other equally effective embodiments.

[0023] Figure 1 depicts a high-level block diagram of a wafer chipping inspection system in accordance with an embodiment of the present principles.

[0024] Figure 2 depicts two images of a quadrant of a diced wafer on which an embodiment of wafer chipping inspection system of the present principles can be applied in accordance with an embodiment of the present principles.

[0025] Figure 3 depicts an embodiment of an edge detection process of an edge detection module of the present principles in accordance with an embodiment of the present principles.

[0026] Figure 4 depicts a pictorial representation of chipping measurements made on quadrants of a diced wafer by a measurement module of the present principles in accordance with an embodiment of the present principles.

[0027] Figure 5 depicts a flow diagram of a method for the automatic detection and measurement of chipping defects on diced wafers in accordance with an embodiment of the present principles.

[0028] Figure 6 depicts a high-level block diagram of a computing device suitable for use with embodiments of a wafer chipping inspection system in accordance with the present principles.

[0029] Figure 7 depicts a high-level block diagram of a network in which embodiments of a wafer chipping inspection system of the present principles can be applied in accordance with an embodiment of the present principles.

[0030] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. The figures are not drawn to scale and may be simplified for clarity. Elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0031] The following detailed description describes techniques (e.g., methods, apparatuses, and systems) for the automatic detection and measurement of chipping defects on diced wafers. While the concepts of the present principles are susceptible to various modifications and alternative forms, specific embodiments thereof are

shown by way of example in the drawings and are described in detail below. It should be understood that there is no intent to limit the concepts of the present principles to the particular forms disclosed. On the contrary, the intent is to cover all modifications, equivalents, and alternatives consistent with the present principles and the appended claims. For example, although embodiments of the present principles are described herein with respect to automatically detecting and measuring specific wafer chipping defects caused by the slicing of wafers, embodiments of the present principles can be applied to automatically detect and measure substantially any wafer defects caused by any means.

[0032] Throughout this disclosure the terms machine learning (ML) model, machine learning model/algorithm and the like, are used interchangeably to describe an ML process that can be trained to identify chipping defects in a diced wafer(s)/wafer portions that can lead to critical failures of the diced wafer(s)/wafer portions.

[0033] Embodiments of the present principles enable the automatic detection and measurement of chipping defects introduced, for example, introduced during a dicing process applied to wafers, with consistency, repeatability and efficiency. In accordance with embodiments of the present principles, a process/algorithm of the present principles is able to prepare the wafer for measurement and enable assisted measurements to quantify and qualify chipping defects on wafers. For example, in some embodiments, in a first step, the algorithm aligns an image of a diced wafers, in a second step the algorithm performs edge detection and in a third step, the algorithm performs defect measurements of the image of the wafers.

[0034] Figure 1 depicts a high-level block diagram of a wafer chipping inspection system 100 in accordance with an embodiment of the present principles. In the embodiment of Figure 1, the wafer chipping inspection system 100 illustratively includes an alignment module 110, an edge detection module 115, and a chipping measurement module 120. In the embodiment of the wafer chipping inspection system 100 of Figure 1, the chipping measurement module 120 includes an optional machine learning model/algorithm. Although in the embodiment of the wafer chipping

inspection system 100 Figure 1 the alignment module 110, the edge detection module 115, and the chipping measurement module 120 are depicted as three (3) separate modules for ease of description, in alternate embodiments of the present principles, the alignment module 110, the edge detection module 115, and the chipping measurement module 120 can comprise a single or at least one module. The wafer defect detection and classification system 100 of Figure 1 further illustratively includes an optional storage device 130.

[0035] As depicted in Figure 1, embodiments of a wafer chipping inspection system of the present principles, such as the wafer chipping inspection system 100 of Figure 1, can be implemented via a computing device 600 (described in greater detail below) in accordance with the present principles. Although in the embodiment of the wafer chipping inspection system 100 of Figure 1 (and with reference to Figure 6), the computing device 600 is depicted as a general-purpose computer, in some embodiments of the present principles a computing device of the present principles can be part of an optical tool (e.g., an optical profiler tool) capable of capturing images of a diced wafer(s).

[0036] In the wafer chipping inspection system 100 of Figure 1, the alignment module 110 can receive data including images of a wafer(s) having been diced, which include images of at least the edges of the diced wafer(s). In some embodiments, such image data can be received from/retrieved from the optional storage device 130. Alternatively or in addition, a wafer chipping inspection system of the present principles, such as the wafer chipping inspection system 100 of Figure 1, can be part of an optical tool (e.g., an optical profiler tool) capable of capturing images of a diced wafer(s), and can receive data related to the captured images, or the images of such a diced wafer(s) from the optical tool (not shown). Even further, alternatively or in addition, a wafer chipping inspection system of the present principles can receive data including images of a wafer(s) having been diced, from a user of a wafer chipping inspection system of the present principles via, for example, an input device of the computing device 600.

[0037] The received image(s) of the diced wafer is/are aligned by the alignment module 110. For example, Figure 2 depicts two images of a quadrant of a diced wafer on which an embodiment of wafer chipping inspection system of the present principles can be applied in accordance with an embodiment of the present principles. In Figure 2, the first image 202 depicts a pre-aligned image of a quadrant of the diced wafer. The second image 204 of Figure 2 depicts the image of the quadrant of the diced wafer having been vertically aligned by the alignment module 110. In the embodiment of Figure 2, the image 204 of the quadrant of the diced wafer was aligned in the vertical direction/axis by the alignment module 110 by rotating the image 204.

[0038] Although in the embodiment of Figure 2, the images 202, 204 represent images of a quadrant of the diced wafer, in alternate embodiments, images received by the alignment module 110 can represent images of a vertically diced wafer portion. In such embodiments, an alignment module of the present principles can align the images of the vertically diced wafer portion in the vertical direction/axis. In some embodiments, images received by the alignment module 110 can represent images of a horizontally diced wafer portion. In such embodiments, an alignment module of the present principles can align the images of the horizontally diced wafer portion in the horizontal direction/axis. In some embodiments and as depicted in the embodiment of Figure 2, images received by the alignment module 110 can represent images of a quadrant of a wafer portion having been diced vertically and horizontally. In such embodiments, an alignment module of the present principles can align the images of the horizontally diced wafer portion in the horizontal direction/axis or in the vertical direction/axis or in a combination of both, the vertical and the horizontal direction/axis. For example, in some embodiments an image rotation alignment process can be used by an alignment module of the present principles to align the images. In such embodiments, an average can be determined along a horizontal and/or vertical edge of diced wafer portions to determine a reference axis line, which can be used to rotate an image such that the reference axis line is parallel to the horizontal axis or vertical axis. In such a manner, the rotated image can be corrected along a relevant axis for further measurement processes.

[0039] Data of the aligned image(s) from the alignment module 110 are communicated to the edge detection module 120. The edge detection module 115 processes the data from the alignment module 110 to determine the edges of the portions of the diced wafer. For example, Figure 3 depicts an embodiment of an edge detection process of an edge detection module of the present principles, such as the edge detection module 115 of the wafer chipping inspection system 100 of Figure 1 in accordance with an embodiment of the present principles. In the embodiment of Figure 3, edges are determined for the quadrant portions of the diced wafer depicted in Figure 2 as quadrant pairs, and specifically in Figure 3, a horizontal edge is determined for the two left quadrants of the diced wafer of Figure 2. As depicted in the first image 302 of Figure 3, in some embodiments of the present principles, the edges are determined pairwise for each quadrant of a diced wafer. For example, in the embodiment of Figure 3 and as depicted in the second image 304, a central reference line between two quadrant images of a diced wafer can be determined by analyzing adjacent quadrants. In the embodiment of Figure 3 an edge detection process can be used to detect image edges, such as in, for example, the third image 306. For example, embodiments of the present principles can use relevant edge detection gradient image processing operations, such as Canny Edge which depicts the luminosity variation due to chipping, to extract the gradients in an image. Such techniques assist in detecting image borders/edges using existing chipping.

[0040] The edge detection process of an edge detection module of the present principles can continue until the edges of all diced wafer portions depicted in an image are determined. For example and in the embodiment of Figure 3, the edge detection process of the edge detection module 115 can continue until the horizontal edge is determined for the two right quadrants of the diced wafer of Figure 2, and the vertical edges are determined for the two top quadrants of the diced wafer and for the two bottom quadrants of the diced wafer of the example of Figure 2.

[0041] The edge information determined by an edge detection module of the present principles, such as the edge detection module 115 of the wafer chipping inspection

system 100 of Figure 1, is communicated to a chipping measurement module of the present principles, such the chipping measurement module 120 of the wafer chipping inspection system 100 of Figure 1. The chipping measurement module 120 uses the edge information to establish a measurement baseline for the diced wafer sections for which the edge(s) was/were determined. That is, once a baseline is determined from the determined edge information for each portion of the diced wafer (i.e., each quadrant of the diced wafer), the measurement module 120 can measure a distance between the baseline and an end of any chipping at several locations in a diced wafer portion to determine chipping information for that portion of the diced wafer, such as a mean chipping value, an average chipping value, a maximum chipping value, and the like.

[0042] For example, Figure 4 depicts a pictorial representation of chipping measurements made on quadrants of a diced wafer by a measurement module of the present principles, such as the measurement module 120 of the wafer chipping inspection system 100 of Figure 1, in accordance with an embodiment of the present principles. As depicted in the embodiment of Figure 4, the measurement module measured a distance between a determined, respective baseline 402₁-402₈ and the end of several chips 407₁-407₇ at several locations in each of the quadrants 404₁-404₄ of the diced wafer.

[0043] In some embodiments of the present principles, the chipping measurement information determined by a measurement module of the present principles can be used to determine if a wafer contains a critical failure. Such information can be used by a wafer chipping inspection system of the present principles, such as the wafer chipping inspection system 100 of Figure 1 to determine if a wafer should be scrapped or if the wafer should be allowed to continue in a wafer processing system.

[0044] For example, as depicted in the wafer chipping inspection system 100 of Figure 1, in some embodiments the measurement module 120 can include an optional machine learning model 122. In accordance with the present principles, the machine learning model 122 can be trained to identify chipping measurements, alone or in any

combinations of chipping measurements, that can lead to critical failures of a diced wafer. For example, in some embodiments, historical data regarding chipping measurements, alone or in combination, that lead to critical failures for diced wafers of all types can be used to train the machine learning module 122 to identify chipping measurements on diced wafers that can lead to critical failures of a diced wafer.

[0045] In some embodiments, a model/algorithm of the present principles, such as the machine learning model/algorithm 122, can include a multi-layer neural network comprising nodes that are trained to have specific weights and biases. In some embodiments, the machine learning model/algorithm 122 employs artificial intelligence techniques or machine learning techniques to analyze received data images including wafer defects. In some embodiments in accordance with the present principles, suitable machine learning techniques can be applied to learn commonalities in sequential application programs and for determining from the machine learning techniques at what level sequential application programs can be canonicalized. In some embodiments, machine learning techniques that can be applied to learn commonalities in sequential application programs can include, but are not limited to, regression methods, ensemble methods, or neural networks and deep learning such as 'Se2oSeq' Recurrent Neural Network (RNNs)/Long Short-Term Memory (LSTM) networks, Convolution Neural Networks (CNNs), graph neural networks applied to the abstract syntax trees corresponding to the sequential program application, and the like. In some embodiments a supervised machine learning (ML) classifier/algorithm could be used such as, but not limited to, Multilayer Perceptron, Random Forest, Naive Bayes, Support Vector Machine, Logistic Regression and the like. In addition, in some embodiments, the ML classifier/algorithm of the present principles can implement at least one of a sliding window or sequence-based techniques to analyze data.

[0046] The machine learning model/algorithm 122 can be trained using a plurality (e.g., hundreds, thousands, etc.) of instances of diced wafer critical failure data in which the training data comprises data related to critical failures of diced wafers

caused by chipping defects on the diced wafer portions to train a machine learning model/algorithm of the present principles to recognize/detect and distinguish between various types of chipping defects on diced wafers that lead to critical failures.

[0047] Figure 5 depicts a flow diagram of a method 500 for the automatic detection and measurement of chipping defects on diced wafers in accordance with an embodiment of the present principles. The method can begin at 502 during which an image of at least a portion of a diced wafer is received. The method 500 can proceed to 504.

[0048] At 504, the received image of at least the portion of the diced wafer is aligned. The method 500 can proceed to 506.

[0049] At 506, the edges of the at least the portion of the diced wafer depicted in the received image are determined. The method can proceed to 508.

[0050] At 508, at least one baseline from which to measure chipping defects on the at least the portion of the diced wafer is automatically determined from the determined edges. The method can proceed to 510.

[0051] At 510, chipping defects on the at least the portion of the diced wafer are measured using determined, respective baselines. The method 500 can be exited.

[0052] In some embodiments of the present principles, the method 500 can further include applying a machine learning model to the determined chipping measurements to determine if the diced wafer contains a critical failure.

[0053] As depicted in Figure 1, embodiments of a wafer chipping inspection system of the present principles, such as the wafer chipping inspection system 100 of Figure 1, can be implemented in a computing device 600 in accordance with the present principles. That is, in some embodiments, wafer image data and the like can be communicated to a wafer chipping inspection system of the present principles using the computing device 600 via, for example, any input/output means associated with the computing device 600. Chipping measurement data associated with a wafer chipping inspection system of the present principles can be presented to a user using

an output device of the computing device 600, such as a display, a printer or any other form of output device.

[0054] For example, Figure 6 depicts a high-level block diagram of a computing device 600 suitable for use with embodiments of a wafer chipping inspection system in accordance with the present principles, such as the wafer chipping inspection system 100 of Figure 1. In some embodiments, the computing device 600 can be configured to implement methods of the present principles as processor-executable executable program instructions 622 (e.g., program instructions executable by processor(s) 610) in various embodiments.

[0055] In the embodiment of Figure 6, the computing device 600 includes one or more processors 610a-610n coupled to a system memory 620 via an input/output (I/O) interface 630. The computing device 600 further includes a network interface 640 coupled to I/O interface 630, and one or more input/output devices 650, such as cursor control device 660, keyboard 670, and display(s) 680. In various embodiments, a user interface can be generated and displayed on display 680. In some cases, it is contemplated that embodiments can be implemented using a single instance of computing device 600, while in other embodiments multiple such systems, or multiple nodes making up the computing device 600, can be configured to host different portions or instances of various embodiments. For example, in one embodiment some elements can be implemented via one or more nodes of the computing device 600 that are distinct from those nodes implementing other elements. In another example, multiple nodes may implement the computing device 600 in a distributed manner.

[0056] In different embodiments, the computing device 600 can be any of various types of devices, including, but not limited to, a personal computer system, desktop computer, laptop, notebook, tablet or netbook computer, mainframe computer system, handheld computer, workstation, network computer, a camera, a set top box, a mobile device, a consumer device, video game console, handheld video game device, application server, storage device, a peripheral device such as a switch, modem, router, or in general any type of computing or electronic device.

[0057] In various embodiments, the computing device 600 can be a uniprocessor system including one processor 610, or a multiprocessor system including several processors 610 (e.g., two, four, eight, or another suitable number). Processors 610 can be any suitable processor capable of executing instructions. For example, in various embodiments processors 610 may be general-purpose or embedded processors implementing any of a variety of instruction set architectures (ISAs). In multiprocessor systems, each of processors 610 may commonly, but not necessarily, implement the same ISA.

[0058] System memory 620 can be configured to store program instructions 622 and/or data 632 accessible by processor 610. In various embodiments, system memory 620 can be implemented using any suitable memory technology, such as static random-access memory (SRAM), synchronous dynamic RAM (SDRAM), nonvolatile/Flash-type memory, or any other type of memory. In the illustrated embodiment, program instructions and data implementing any of the elements of the embodiments described above can be stored within system memory 620. In other embodiments, program instructions and/or data can be received, sent or stored upon different types of computer-accessible media or on similar media separate from system memory 620 or computing device 600.

[0059] In one embodiment, I/O interface 630 can be configured to coordinate I/O traffic between processor 610, system memory 620, and any peripheral devices in the device, including network interface 640 or other peripheral interfaces, such as input/output devices 650. In some embodiments, I/O interface 630 can perform any necessary protocol, timing or other data transformations to convert data signals from one component (e.g., system memory 620) into a format suitable for use by another component (e.g., processor 610). In some embodiments, I/O interface 630 can include support for devices attached through various types of peripheral buses, such as a variant of the Peripheral Component Interconnect (PCI) bus standard or the Universal Serial Bus (USB) standard, for example. In some embodiments, the function of I/O interface 630 can be split into two or more separate components, such as a north

bridge and a south bridge, for example. Also, in some embodiments some or all of the functionality of I/O interface 630, such as an interface to system memory 620, can be incorporated directly into processor 610.

[0060] Network interface 640 can be configured to allow data to be exchanged between the computing device 600 and other devices attached to a network (e.g., network 690), such as one or more external systems or between nodes of the computing device 600. In various embodiments, network 690 can include one or more networks including but not limited to Local Area Networks (LANs) (e.g., an Ethernet or corporate network), Wide Area Networks (WANs) (e.g., the Internet), wireless data networks, some other electronic data network, or some combination thereof. In various embodiments, network interface 640 can support communication via wired or wireless general data networks, such as any suitable type of Ethernet network, for example; via digital fiber communications networks; via storage area networks such as Fiber Channel SANs, or via any other suitable type of network and/or protocol.

[0061] Input/output devices 650 can, in some embodiments, include one or more display terminals, keyboards, keypads, touchpads, scanning devices, voice or optical recognition devices, or any other devices suitable for entering or accessing data by one or more computer systems. Multiple input/output devices 650 can be present in computer system or can be distributed on various nodes of the computing device 600. In some embodiments, similar input/output devices can be separate from the computing device 600 and can interact with one or more nodes of the computing device 600 through a wired or wireless connection, such as over network interface 640.

[0062] Those skilled in the art will appreciate that the computing device 600 is merely illustrative and is not intended to limit the scope of embodiments. In particular, the computer system and devices can include any combination of hardware or software that can perform the indicated functions of various embodiments, including computers, network devices, Internet appliances, PDAs, wireless phones, pagers, and the like. The computing device 600 can also be connected to other devices that are not

illustrated, or instead can operate as a stand-alone system. In addition, the functionality provided by the illustrated components can in some embodiments be combined in fewer components or distributed in additional components. Similarly, in some embodiments, the functionality of some of the illustrated components may not be provided and/or other additional functionality can be available.

[0063] The computing device 600 can communicate with other computing devices based on various computer communication protocols such as Wi-Fi, Bluetooth, RTM, (and/or other standards for exchanging data over short distances includes protocols using short-wavelength radio transmissions), USB, Ethernet, cellular, an ultrasonic local area communication protocol, etc. The computing device 600 can further include a web browser.

[0064] Although the computing device 600 is depicted as a general-purpose computer, the computing device 600 is programmed to perform various specialized control functions and is configured to act as a specialized, specific computer in accordance with the present principles, and embodiments can be implemented in hardware, for example, as an application specified integrated circuit (ASIC). As such, the process steps described herein are intended to be broadly interpreted as being equivalently performed by software, hardware, or a combination thereof.

[0065] Figure 7 depicts a high-level block diagram of a network in which embodiments of a wafer chipping inspection system of the present principles, such as the wafer chipping inspection system 100 of Figure 1, can be applied. The network environment 700 of Figure 7 illustratively comprises a user domain 702 including a user domain server/computing device 704. The network environment 700 of Figure 7 further comprises computer networks 706, and a cloud environment 710 including a cloud server/computing device 712.

[0066] In the network environment 700 of Figure 7, a wafer chipping inspection system in accordance with the present principles, such as wafer chipping inspection system of Figure. 1, can be included in at least one of the user domain server/computing device 704, the computer networks 706, and the cloud

server/computing device 712. That is, in some embodiments, a user can use a local server/computing device (e.g., the user domain server/computing device 704) to detect and measure chipping defects in diced wafers in accordance with the present principles.

[0067] In some embodiments, a user can implement a system for detecting and measuring chipping defects in diced wafers in the computer networks 706 in accordance with the present principles. Alternatively or in addition, in some embodiments, a user can implement a system for detecting and measuring chipping defects in diced wafers in the cloud server/computing device 712 of the cloud environment 710 to provide container forensics in accordance with the present principles. For example, in some embodiments it can be advantageous to perform processing functions of the present principles in the cloud environment 710 to take advantage of the processing capabilities and storage capabilities of the cloud environment 710. In some embodiments in accordance with the present principles, a system for detecting and measuring chipping defects in diced wafers can be located in a single and/or multiple locations/servers/computers to perform all or portions of the herein described functionalities of a system in accordance with the present principles. For example, a wafer chipping inspection system of the present principles can be located in one or more than one of the user domain 702, the computer network environment 706, and the cloud environment 710 for detecting and measuring chipping defects in diced wafers in accordance with the present principles.

[0068] Those skilled in the art will appreciate that, while various items are illustrated as being stored in memory or on storage while being used, these items or portions of them can be transferred between memory and other storage devices for purposes of memory management and data integrity. Alternatively, in other embodiments some or all of the software components can execute in memory on another device and communicate with the illustrated computer system via inter-computer communication. Some or all of the system components or data structures can also be stored (e.g., as instructions or structured data) on a computer-accessible medium or a portable article

to be read by an appropriate drive, various examples of which are described above. In some embodiments, instructions stored on a computer-accessible medium separate from the computing device 600 can be transmitted to the computing device 600 via transmission media or signals such as electrical, electromagnetic, or digital signals, conveyed via a communication medium such as a network and/or a wireless link. Various embodiments can further include receiving, sending or storing instructions and/or data implemented in accordance with the foregoing description upon a computer-accessible medium or via a communication medium. In general, a computer-accessible medium can include a storage medium or memory medium such as magnetic or optical media, e.g., disk or DVD/CD-ROM, volatile or non-volatile media such as RAM (e.g., SDRAM, DDR, RDRAM, SRAM, and the like), ROM, and the like.

[0069] The methods and processes described herein may be implemented in software, hardware, or a combination thereof, in different embodiments. In addition, the order of methods can be changed, and various elements can be added, reordered, combined, omitted or otherwise modified. All examples described herein are presented in a non-limiting manner. Various modifications and changes can be made as would be obvious to a person skilled in the art having benefit of this disclosure. Realizations in accordance with embodiments have been described in the context of particular embodiments. These embodiments are meant to be illustrative and not limiting. Many variations, modifications, additions, and improvements are possible. Accordingly, plural instances can be provided for components described herein as a single instance. Boundaries between various components, operations and data stores are somewhat arbitrary, and particular operations are illustrated in the context of specific illustrative configurations. Other allocations of functionality are envisioned and can fall within the scope of claims that follow. Structures and functionality presented as discrete components in the example configurations can be implemented as a combined structure or component. These and other variations, modifications, additions, and improvements can fall within the scope of embodiments as defined in the claims that follow.

[0070] In the foregoing description, numerous specific details, examples, and scenarios are set forth in order to provide a more thorough understanding of the present disclosure. It will be appreciated, however, that embodiments of the disclosure can be practiced without such specific details. Further, such examples and scenarios are provided for illustration, and are not intended to limit the disclosure in any way. Those of ordinary skill in the art, with the included descriptions, should be able to implement appropriate functionality without undue experimentation.

[0071] References in the specification to “an embodiment,” etc., indicate that the embodiment described can include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Such phrases are not necessarily referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is believed to be within the knowledge of one skilled in the art to affect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly indicated.

[0072] Embodiments in accordance with the disclosure can be implemented in hardware, firmware, software, or any combination thereof. Embodiments can also be implemented as instructions stored using one or more machine-readable media, which may be read and executed by one or more processors. A machine-readable medium can include any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computing device or a “virtual machine” running on one or more computing devices). For example, a machine-readable medium can include any suitable form of volatile or non-volatile memory.

[0073] Modules, data structures, and the like defined herein are defined as such for ease of discussion and are not intended to imply that any specific implementation details are required. For example, any of the described modules and/or data structures can be combined or divided into sub-modules, sub-processes or other units of computer code or data as can be required by a particular design or implementation.

[0074] In the drawings, specific arrangements or orderings of schematic elements can be shown for ease of description. However, the specific ordering or arrangement of such elements is not meant to imply that a particular order or sequence of processing, or separation of processes, is required in all embodiments. In general, schematic elements used to represent instruction blocks or modules can be implemented using any suitable form of machine-readable instruction, and each such instruction can be implemented using any suitable programming language, library, application-programming interface (API), and/or other software development tools or frameworks. Similarly, schematic elements used to represent data or information can be implemented using any suitable electronic arrangement or data structure. Further, some connections, relationships or associations between elements can be simplified or not shown in the drawings so as not to obscure the disclosure.

[0075] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof.

Claims:

1. A method for the automatic detection and measurement of chipping defects on diced wafers, comprising:
 - receiving an image of at least a portion of a diced wafer;
 - aligning the received image of the at least the portion of the diced wafer;
 - determining edges of the at least the portion of the diced wafer depicted in the aligned, received image;
 - automatically determining at least one baseline from which to measure chipping defects on the at least the portion of the diced wafer from the determined edges; and
 - measuring chipping defects on the at least the portion of the diced wafer using at least one determined, respective baseline.
2. The method according to claim 1, further comprising:
 - aligning the received image along a vertical axis.
3. The method according to claim 1, further comprising:
 - aligning the received image along a horizontal axis.
4. The method according to any of claims 1 to 3, further comprising:
 - determining a reference axis line; and
 - aligning the received image along the determined, reference axis line.
5. The method according to any of claims 1 to 4, further comprising:
 - measuring chipping defects as a distance from the determined respective baseline to an end of a chipping defect.
6. The method according to any of claims 1 to 5, further comprising:

applying a machine learning model to measured chipping defects to determine if a critical failure exists on the diced wafer.

7. The method according to claim 6 wherein the machine learning model is trained to recognize measured chipping defects that result in a critical failure of the diced wafer.

8. An apparatus for the automatic detection and measurement of chipping defects on diced wafers, comprising:

a processor; and

a memory coupled to the processor, the memory having stored therein at least one of programs or instructions executable by the processor to configure the apparatus to:

receive an image of at least a portion of a diced wafer;

align the received image of the at least the portion of the diced wafer;

determine edges of the at least the portion of the diced wafer depicted in the aligned, received image;

automatically determine at least one baseline from which to measure chipping defects on the at least the portion of the diced wafer from the determined edges; and

measure chipping defects on the at least the portion of the diced wafer using the at least one determined baseline.

9. The apparatus according to claim 8, wherein the received image is aligned along a vertical axis.

10. The apparatus according to claim 8 wherein the received image is aligned along a horizontal axis.

11. The apparatus according to any of claims 8 to 10, wherein the apparatus is further configured to:

determine a reference axis line; and
align the received image along the determined, reference axis line.

12. The apparatus according to any of claims 8 to 11, wherein chipping defects are measured as a distance from the determined respective baseline to an end of a chipping defect.

13. The apparatus according to any of claims 8 to 12, wherein the apparatus is further configured to:

apply a machine learning model to measured chipping defects to determine if a critical failure exists on the diced wafer.

14. The apparatus of claim 13, wherein the machine learning model is trained to recognize measured chipping defects that result in a critical failure of the diced wafer.

15. A system for the automatic detection and measurement of chipping defects on diced wafers, comprising:

an image capture device for capturing images of at least a portion of a diced wafer; and

an apparatus comprising:

a processor; and

a memory having stored therein at least one program, the at least one program including instructions which, when executed by the processor, cause the system to perform a method, comprising;

capturing an image of at least a portion of a diced wafer;

aligning the captured image of the at least the portion of the diced wafer;

determining edges of the at least the portion of the diced wafer depicted in the aligned, received image;

automatically determining at least one baseline from which to measure chipping defects on the at least the portion of the diced wafer from the determined edges; and

measuring chipping defects on the at least the portion of the diced wafer using at least one determined, respective baseline.

16. The system of claim 15, wherein the method further comprises:
aligning captured images along at least one of a vertical axis or a horizontal axis.
17. The system according claim 15, wherein the method further comprises:
determining a reference axis line; and
aligning the captured images along the determined, reference axis line.
18. The system according to any of claims 15 to 17, wherein the method further comprises:
measuring chipping defects as a distance from the determined respective baseline to an end of a chipping defect.
19. The system according to any of claims 15 to 18, wherein the method further comprises:
applying a machine learning model to measured chipping defects to determine if a critical failure exists on the diced wafer.
20. The system of claim 19, wherein the machine learning model is trained to recognize measured chipping defects that result in a critical failure of the diced wafer.