

BUMPLESS FLIP CHIP ASSEMBLY WITH STRIPS-IN-VIA AND PLATING

BACKGROUND OF THE INVENTION

5

1. Field of the Invention

This invention relates generally to semiconductor device assembly, and in particular, to a chip assembly which includes a single or multi-layered
10 substrate of which circuitry are connected to the input/output terminal pads of the IC chip through deposition of conductive material onto pre-formed leads and IC pads.

2. Related Art

15

Recent developments in semiconductor packaging suggest an increasingly critical role of the technology. New demands are coming from requirements for more leads per chip (and hence smaller input/output terminal pitch), shrinking die and package footprint, and higher operational
20 frequency that generate more heat (thus requiring advanced heat dissipation designs). All of these considerations must be met and, as usual, are placed in addition to the cost that packaging adds to the semiconductor-manufacturing food chain.

Conventionally, there are three predominant chip-level connection
25 technologies in use for integrated circuits, namely wire bonding, tape

automated bonding (TAB) and flip chip (FC), to electrically or mechanically connect integrated circuits to leadframe or substrate circuitry. Wire bonding has been by far the most broadly applied technique in the semiconductor industry because of its maturity and cost effectiveness. However, this process can be performed only one at a time between the semiconductor chip's bonding pads and the appropriate interconnect points. Furthermore, because of the ever-increasing operational frequency of the device, the length of the interconnects needs to be shorter to minimize inductive noise in power and ground, and also to limit the crosstalk between the signal leads. An example of such a method is disclosed in U.S. Pat. No. 5,397,921 to Karnezos et al.

Flip chip technology is generally defined as mounting of an unpackaged semiconductor chip with the active side facing down to a interconnect substrate through some kind of contact anchors such as solder, gold or organic conductive adhesive bumps. The major advantage of the flip chip technology is the short interconnects which can, therefore, handle high speed or high frequency signals. There are essentially no parasitic elements, such as inductance. Not only is the signal propagation delay slashed, but much of the waveform distortion is also eliminated. Flip Chip also allows an array interconnecting layout that provides more I/O than a perimeter interconnect with the same die size. Furthermore, it requires minimal mounting area and weight, thus effecting overall cost savings since no extra packaging and less circuit board space is used. An example of such a method is disclosed in U.S. Pat. No. 5,261,593 to Casson et al.

While flip chip technology shows tremendous advantage over wire bonding, its cost and technical limitations are significant. First of all, prior art flip chip technology must confront the challenges of forming protruded contact anchors or bumps to serve as electrical connections between integrated circuit chip and substrate circuitry. Examples of such an approach are disclosed in U.S. Pat. No. 5,803,340 to Yeh, al. et. al.; U.S. Pat. No. 5,736,456 to Akram. These typically include a very costly vacuum process to deposit intermediate under-bump layer that serves as adhesive and diffusion barrier. This barrier layer is typically composed of a film stack that can be in the structure of chromium/copper/gold. Bumping materials such as solder are subsequently deposited onto this intermediate layer through evaporation, sputtering, electroplating, solder jetting or paste printing methods followed by a reflow step to form the solder contacts. Although evaporation and sputtering techniques can potentially offer high density bumps, these processes need very tight controls and normally result in poor yield. In addition, from the mechanical structural viewpoint, the coefficient of thermal expansion (CTE) of silicon and substrate may be quite different, and the stress between these two parts after attachment will build up and be fully loaded onto these bumps. This will then cause severe joint cracking and disconnection problems during normal operation conditions. As a result, a conventional flip chip assembly is not only very costly but also suffers from a very serious reliability problems and high fatality ratio.

Techniques for fabricating the intermediate under-bump barrier layer as well as bump material utilizing electroless plating methods are also

known in the prior art. An example of such a method is described in the U.S. Pat. No. 5,583,073 to Lin et al. Although electroless technique provides an economical, simple and effective method for under bump barrier layer, contacting material such as solder or adhesive is still required for assembling. Solder dipping or screen printing of solder paste onto these bumps have been explored but have been met with very limited success due to lack of solder bridging control and non-uniform deposition of solder on the metal bump. This process can be very troublesome and suffers from poor process control as input/output terminal pad space is getting smaller and smaller. Additional problems have been encountered with the tin/lead solder systems due to its increase in electrical resistance over time, and this solder contacts are easily fatigued in thermo-mechanical stressing.

In view of the limitations of currently available integrated circuits assembling methods, a high performance, reliable and economical method that can effectively interconnect integrated circuits to the external circuitry would be greatly desirable.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a flip chip assembly to address high density, low cost and high performance requirements of semiconductor packaging. It involves the bonding of substrate circuitry to semiconductor device through connection of pre-formed leads to the IC terminal pads inside the via holes without the need

for conventional bump, bonding wire, or other media. These unique joining approaches are capable of providing both electrical and mechanical connection between IC chip and circuitry of the substrate.

To achieve the foregoing, the assembly includes a rigid or flexible
5 dielectric substrate having a plurality of electrically conductive circuitry and a plurality of via holes formed in the dielectric substrate. These conductive traces on the surface of the substrate are extended into each specific via holes through the leads that are fabricated by conventional circuitry patterning process, cutting or punching methods.

10 The orientation of the contact ensures that at least one of the via holes in the dielectric substrate are aligned to the pads of the IC chip so that these pads can be totally or partially exposed through the opposite side of the substrate. After alignment, the IC chip is attached to the dielectric substrate through adhesive film or paste, or mechanical techniques to form a
15 chip assembly. Electrically conductive material is subsequently deposited onto the leads and the input/output pads of the IC chip to complete the connection of the IC chip and the substrate circuitry.

In one embodiment of the invention, the connection method may take the form of electrolytic plating. In this method, the assembly is
20 connected to an external power source and serves as one of the electrode for electrochemical plating. Electrolytic plating of metals and alloys, are common and are well known in the industry, and so further elaboration is not necessary. The metallic leads as well as other conductive parts of the assembly that are connected to the external power and exposed to the

plating solution will generate cathodic reaction on the surfaces and continuously deposit metal or alloys thereon. This deposition of metal or alloys will result in a longer and wider lead as electroplating reaction proceeds. In the initial stage, the terminal pads of the IC chip that are also
5 immersed in the plating solution, will not receive any deposition due to lack of connection to the external power source. However, as the plating process continues, the leads which are bent toward inside the via holes, will lengthen out and finally reach the surface of the terminal pads which located at the bottom of the via holes. These metallic contacts will then provide
10 electrical power to the IC terminal pads and subsequently initiate electroplating reaction thereon. This simultaneously electroplating of leads and terminal pads will then form an integral part of a joint thus providing an effective means for electrical and mechanical connections between IC chip and the dielectric circuitry. This is important in that it not only assures a very
15 desired inter-metallic structure but also assures a pre-defined, very reliable connection between substrate and IC chip due to the flexibility of the leads. In some of the embodiments, in order to provide a good contact and prevent oxidation or dissolution of the IC terminal pads before the plating starts, these pads are commonly pre-treated or coated with a protective layer such
20 as a stack of thin film thereon before assembly.

In another embodiment of the invention, the connection is achieved by electroless (chemical) plating. In this method, the electroless plating can be initiated on the catalyzed leads and continuously deposit metal or alloys thereon. In contrast to the electrolytic plating, there is no external power

necessary to sustain the plating reaction and the metal deposition can be achieved by a chemical reaction controlled by at least one reducing agent (catalyst) such as hypophosphite. Since electroless plating is a common practice and well known in the industry, no further explanation is necessary.

- 5 Under certain pre-defined bath conditions (e.g., temperature and chemical composition), the catalyzed leads that are immersed in the plating bath will be readily initiated and will continuously deposit metal or alloys thereon. Similarly, this deposition of metal or alloys will result in a longer and wider lead as plating reaction proceeds. The terminal pads of the IC chip that are
10 immersed in the plating solution may also receive deposition simultaneously depending on their surface energy and chemical potential.

- According to another embodiment of the invention, the connection method may take the form of soldering. In this method, the connecting leads inside the via holes are pre-coated with the soldering materials and brought
15 near to or in contact with the IC terminal pads after the IC attachment. Heat, which serves to activate the flux and bring the solder to its melting point to effect the metallurgical bonding, is then applied to the assembly. This re-flow process will results in a solder joint which will electrically and physically connect the pre-coated lead and IC pad for permanent contact thereafter.
20 This is considered important in that it not only assures a very low cost and simple process but also provides a compliant joint with significant stress release, which results in a very reliable connection between the substrate circuitry and IC chip.

Various techniques including electroplating, wave soldering, meniscus solder coating, solder paste printing and dispensing techniques can accomplish the pre-coating of solder materials onto the leads.

5 The via holes of the substrate circuitry can be formed by various techniques including mechanical drilling, punching, plasma etching or laser drilling. They are formed in the substrate at the locations where the electrical circuitry on one side of the substrate can be connected to the opposite side of the surface on which the semiconductor chip or chips are mounted and their input/output terminal pads can be exposed through these holes.

10 Using extended leads and conductive material directly deposited in via hole can effectively connect IC chip and dielectric substrate circuitry without external bumps or wires. This approach allows a reliable, low profile, high performance and low cost assembly to be achieved. In particular, a small via hole, which can be formed by laser or other techniques, allows
15 very fine pitch terminal pad to be interconnected, and can significantly enhance the capability of packaging future high I/O semiconductor chips.

BRIEF DESCRIPTION OF THE DRAWINGS

20 FIG. 1 is an isometric view of a substrate showing via hole and traces of the substrate circuitry.

FIG. 2A to 2E are diagrammatic cross-sectional views showing steps involved in the manufacturing of an integrated circuits assembly by electroless plating according to the present invention.

FIG. 3A to 3E are diagrammatic cross-sectional views showing steps involved in the manufacturing of an integrated circuit assembly by electrolytic plating according to another embodiment of the invention.

FIG. 4A to 4F are diagrammatic cross-sectional views showing steps involved in the manufacturing of an integrated circuit assembly by pre-deposited solder and re-flowing process according to another embodiment of the invention.

10

DETAILED DESCRIPTION OF THE INVENTION

According to the invention, a flip chip assembly is provided to address high density, low cost and high performance requirements of semiconductor packaging. It involves the bonding of substrate circuitry to semiconductor device through connection of pre-formed leads to the IC terminal pads inside the via holes without the need for conventional bump, bonding wire, or other media. These unique joining approaches are capable of providing both electrical and mechanical connection between IC chip and circuitry of the substrate.

20

To achieve the foregoing, the assembly includes a rigid or flexible dielectric substrate having a plurality of electrically conductive circuitry and a plurality of via holes formed in the dielectric substrate. These conductive traces on the surface of the substrate are extended into each specific via holes through the leads that are fabricated by conventional circuitry

patterning process, cutting or punching methods. FIG. 1 is an isometric view of a section of such a substrate 101 on which vias 102 are normally formed by laser or mechanical drilling. These via holes 102 are to serve as the interconnecting channels between circuitry traces 103 and IC terminal pads through the pre-formed leads 104 hanging inside the vias. Circuitry traces 103, which extend from vias 102 along an outer surface of the substrate, will lead to another pad connection for next level assembly.

The orientation of the contact ensures that at least one of the via holes in the dielectric substrate are aligned to the pads of the IC chip so that these pads can be totally or partially exposed through the opposite side of the substrate. After alignment, the IC chip is attached to the dielectric substrate through adhesive film or paste, or mechanical techniques to form a chip assembly. Electrically conductive material is subsequently deposited onto the leads and the input/output pads of the IC chip to complete the connection of the IC chip and the substrate circuitry.

As defined herein, the preferred embodiment is particularly directed to the bonding of an integrated circuit (IC) chip to a flexible circuitized substrate, or to a more rigid, circuitized substrate, a particular example of the later being a printed circuit board. It is to be understood, however, that the invention is not limited to attachment to printed circuit boards, in that other circuitized substrates, including known flexible substrate tapes or ceramic substrates, may be employed. Typically, organic-type substrate is preferable for the purpose of lower cost, superior dielectric property whereas inorganic-type of substrate is preferable when high thermal dissipation and matched

coefficient of expansion are desired. The term "substrate" as used herein is meant as at least one layer of dielectric material having at least one conductive layer thereon. Printed circuit boards of similar type are well known in the electronic industry, as well as the processes for making same, and, therefore, further definition is not believed to be necessary. Such structures may include many more electrically conductive layers than those depicted in FIGS. 1 through 4, depending on the desired operational characteristics. As is known, such electrically conductive layers may function as signal, power, and/or ground layers.

10 In one embodiment of the invention, the connection method may take the form of electrolytic plating. In this method, the assembly is connected to an external power source and serves as one of the electrode for electrochemical plating. Electrolytic plating of metals and alloys, are common and are well known in the industry, and so further elaboration is not
15 necessary. The metallic leads as well as other conductive parts of the assembly that are connected to the external power and exposed to the plating solution will generate cathodic reaction on the surfaces and continuously deposit metal or alloys thereon. This deposition of metal or alloys will result in a longer and wider lead as electroplating reaction
20 proceeds. In the initial stage, the terminal pads of the IC chip that are also immersed in the plating solution, will not receive any deposition due to lack of connection to the external power source. However, as the plating process continues, the leads which are bent toward inside the via holes, will lengthen out and finally reach the surface of the terminal pads which located

at the bottom of the via holes. These metallic contacts will then provide electrical power to the IC terminal pads and subsequently initiate electroplating reaction thereon. This simultaneously electroplating of leads and terminal pads will then form an integral part of a joint thus providing an effective means for electrical and mechanical connections between IC chip and the dielectric circuitry. This is important in that it not only assures a very desired inter-metallic structure but also assures a pre-defined, very reliable connection between substrate and IC chip due to the flexibility of the leads. In some of the embodiments, in order to provide a good contact and prevent oxidation or dissolution of the IC terminal pads before the plating starts, these pads are commonly pre-treated or coated with a protective layer such as a stack of thin film thereon before assembly.

In another embodiment of the invention, the connection is achieved by electroless (chemical) plating. In this method, the electroless plating can be initiated on the catalyzed leads and continuously deposit metal or alloys thereon. In contrast to the electrolytic plating, there is no external power necessary to sustain the plating reaction and the metal deposition can be achieved by a chemical reaction controlled by at least one reducing agent (catalyst) such as hypophosphite. Since electroless plating is a common practice and well known in the industry, no further explanation is necessary. Under certain pre-defined bath conditions (e.g., temperature and chemical composition), the catalyzed leads that are immersed in the plating bath will be readily initiated and will continuously deposit metal or alloys thereon. Similarly, this deposition of metal or alloys will result in a longer and wider

lead as plating reaction proceeds. The terminal pads of the IC chip that are immersed in the plating solution may also receive deposition simultaneously depending on their surface energy and chemical potential.

For example, a catalyzed or oxide-free nickel which is pre-coated on the aluminum surface will enable the plating reaction to proceed on the IC pads as well. As the plating process continues, the leads which are bent toward inside the via holes, will lengthen out and finally touch the terminal pads located at the bottom of the via holes. Likewise, the simultaneously plated-up parts of leads and terminal pads will join together providing an effective means for electrical and mechanical connections between IC chip and dielectric circuitry. This is important in that it not only assures a very flexible design in the substrate circuitry since no external contact is necessary, but also assures a very reliable metallic interface between substrate and chip.

According to another embodiment of the invention, the connection method may take the form of soldering. In this method, the connecting leads inside the via holes are pre-coated with the soldering materials and brought near to or in contact with the IC terminal pads after the IC attachment. Heat, which serves to activate the flux and bring the solder to its melting point to effect the metallurgical bonding, is then applied to the assembly. This re-flow process will results in a solder joint which will electrically and physically connect the pre-coated lead and IC pad for permanent contact thereafter. This is considered important in that it not only assures a very low cost and simple process but also provides a compliant joint with significant stress

release, which results in a very reliable connection between the substrate circuitry and IC chip.

Various techniques including electroplating, wave soldering, meniscus solder coating, solder paste printing and dispensing techniques
5 can accomplish the pre-coating of solder materials onto the leads. It is understood from the teaching herein that the particular solder material and methods of dispensing techniques depicted here are not meant to limit the invention, in that it is also possible to directly place solder particles onto the leads and re-flow them prior to the IC mounting. In the case of solder paste
10 application, flux is normally incorporated and the considerations are the same as described for conventional printed circuit board assembly. Since the soldering material on the leads may take the form of paste, or plated-up deposition, heat transfer techniques such as conduction, convection, radiation, or a combination of these is normally needed to re-flow them in
15 order to wet the IC pad surface. A preferred application of such heat is achieved by using laser. Alternatively, the attached assembly may be positioned within a suitable oven to effect solder reflow and bonding to the IC terminals which are in the vicinity of the via holes. One example of such an approach is an infrared (IR) continuous belt reflow oven. In the
20 alternative, hot nitrogen gas may be directed onto the solder members of the assembly. It is understood from the teaching herein that the particular re-flow techniques depicted above are not meant to limit the invention, in that it is also possible to reflow the solder by vapor phase reflow or other similar techniques.

A barrier layer over-coated on the aluminum pad is preferred as it provides good solder wetting and protects the aluminum surface against leaching, oxidation or degradation resulting from heat and soldering contact. This coating can be accomplished by sputtering a stake of thin film thereon
5 or by wet chemical direct plating technique such as electroless nickel and immersion gold. For copper terminal pads, the pre-treatment may not be necessary as long as its surface is free of oxide and contamination.

The contacting leads that located inside of the via holes may take the form of strips with various shapes. A preferred fabrication process is
10 conventional photolithographic patterning and etching. Alternately, they can be fabricated by micro-machining or laser cutting. After these leads are formed, they are bent toward inside the via holes in order to provide an effective connection path between IC pads and the circuitry. The bending of the leads can be achieved by a variety of methods such as vacuum suction,
15 air blowing or mechanical pushing.

The via holes of the substrate circuitry can be formed by various techniques including mechanical drilling, punching, plasma etching or laser drilling. They are formed in the substrate at the locations where the electrical circuitry on one side of the substrate can be connected to the opposite side
20 of the surface on which the semiconductor chip or chips are mounted and their input/output terminal pads can be exposed through these holes.

If the finished product is, for instance, a ball grid array package, solder balls will normally be placed on the specific pads on the surface of the dielectric substrate. This finished package can be connected to a printed

circuit board by reflowing the solder balls to form an attachment to the traces of the printed circuit board.

Using extended leads and conductive material directly deposited in via hole can effectively connect IC chip and dielectric substrate circuitry without external bumps or wires. This approach allows a reliable, low profile, high performance and low cost assembly to be achieved. In particular, a small via hole, which can be formed by laser or other techniques, allows very fine pitch terminal pad to be interconnected, and can significantly enhance the capability of packaging future high I/O semiconductor chips. The present invention will be illustrated further by the following examples. These examples are meant to illustrate and not to limit the invention, the scope of which is defined solely by the appended claims.

EXAMPLE 1

FIG 2A shows an integrated circuit chip 201 with various types of transistor, wiring and the like were (not shown) having a plurality of exposed input/output terminal pads 202 (only one shown). These pads 202 were firstly cleaned by dipping the integrated circuitry chip 201 in a phosphoric acid solution at room temperature with an immersion time of 10 minutes to remove the surface oxide film. This chip was next dipped in a diluted catalytic solution Enthone "Alumon EN" (trademark) at 25 degree C for 20 seconds to form an thin zinc film (not shown) on the surface of aluminum alloy terminals 202. Following steps include a thorough distilled water

rinse and electroless plating using Shipley "NIPOSIT 468" (trademark) at 85 degree Celcius. The electroless plating will continuously deposit a thin layer of nickel film 203 containing phosphorous (to be referred to as a nickel film hereafter) on the input/output terminal pads 202 of the integrated circuits
5 chips 201

FIG. 2B shows a substrate 204 having a plurality of electrically conductive circuitry traces 205 partially covered by the solder mask 206. The traces 205 on the substrate extend to the via holes 207 and split into a plurality of leads 208 which are bent toward inside of the via hole. The holes
10 207 are arranged in such a manner that the terminal pads 202 of the integrated circuit chip 201 can be totally or partially exposed when integrated circuit chip 201 is mounted on the substrate 204. The bent leads 208 are to serve as the electrically connecting channels for the respective traces 205 of the substrate 204 with respective terminal pads 202 of the
15 integrated circuit chips 201. These leads were activated by immersing them in a palladium chloride solution (0.05 M) for electroless (chemical) plating before attachment.

As shown in FIG. 2C, the IC chip is securely attached to the substrate circuitry by adhesive paste ABLESTIK "ABLEBOND 961-2" (trademark) 209 and this assembly is immersed in the electroless plating
20 solution Shipley "NIPOSIT 468" (trademark) at 65 degree C. The electroless plating will initiate and continuously deposit nickel 210 on the leads 208 as well as on the pre-deposited nickel film 203 on the input/output terminal pads 202 of the integrated circuits chips 201.

As FIG. 2D shows, the bent leads and input/output terminals finally contact and join together to become an integrated part. These simultaneously-plated joints will then provide an effective means for electrical and mechanical connections between the input/output terminals and the traces of the dielectric circuitry.

As shown in FIG. 2E, the solder ball 211 is attached to the substrate at the opening site of the solder mask to provide the finished assembly for the next level connection.

Though only one integrated circuit chip 201 is shown in the figure, it is to be understood that additional integrated circuit chips, as well as passive components such as resistors or capacitors, can also be mounted on the substrate 204.

EXAMPLE 2

15

Referring now to FIG 3A, an integrated circuit chip 301 similar to that in example 1 was cleaned in an alkaline solution containing 0.05M phosphoric acid at room temperature (25 degree C) with immersion time of 1 minute. The chip was then thoroughly rinsed in distilled water to ensure there is no residue on the surface of IC chip. A stake of thin film 303 in the structure of chromium (500 Angstroms)/copper (700Angstroms)/gold (1000 Angstroms) was deposited and patterned on the terminal pads 302 to serve as the barrier and adhesive layer.

FIG. 3B shows a dielectric substrate 304 having a plurality of electrically conductive circuitry traces 305 partially covered by the solder mask 306. These traces 305 on the substrate extend into via holes 307 and split into a plurality of leads 308 which are bent toward inside of the via holes 307. The holes 307 are arranged in such a manner that the terminal pads 302 of the integrated circuit chip 301 can be totally or partially exposed when integrated circuit chip 301 is mounted on the substrate 304. The bent leads 308 are to serve as the electrically connecting channels for the respective traces 305 of the substrate 304 with respective terminal pads 302 of the integrated circuit chips 301.

As shown in FIG. 3C, the IC chip is securely attached to the substrate circuitry by adhesive film ABLESTIK "ABLEFILM 561K" (trademark) 309 and the assembly is immersed in the copper plating solution Sel-Rex "CUBATH M " (trademark) at 25 degree Celcius. The electrical power source is connected to the circuitry of the dielectric substrate. Electroplating reaction initiates and continuously deposits copper 310 on the bent leads 307. As the plating process proceeds, the length and width of the leads will continuously increase.

FIG. 3D shows that the plated copper has reached gold surface 303 of the terminal pads 302 to provide electrical contact with the terminal pads and to initiate copper plating thereon. These electroplated joints 310 will then provide an effective means for electrical and mechanical connections between the input/output terminals and the top surface of the dielectric circuitry.

As shown in FIG. 3E, the solder ball 311 is attached to the substrate at the opening site of the solder mask to provide the finished assembly for the next level connection.

5 EXAMPLE 4

FIG 4A shows an integrated circuit chip 401 with various types of transistor, wiring and the like (not shown) having a plurality of exposed input/output terminal pads 402 (only one shown). These pads 402 were
10 firstly cleaned by dipping the integrated circuitry chip 401 in a phosphoric acid solution at room temperature with an immersion time of 10 minutes to remove the surface oxide film. This chip was next dipped in a diluted catalytic solution Enthone "Alumon EN" (trademark) at 25 degree C for 20 seconds to form a thin zinc film (not shown) on the surface of aluminum alloy
15 terminals 402. Following steps include a thorough distilled water rinse and electroless plating using Shipley "NIPOSIT 468" (trademark) at 65 degree C. The electroless plating will continuously deposit a thin layer of nickel film 403 containing phosphorous (to be referred to as a nickel film hereafter) on the input/output terminal pads 402 of the integrated circuits
20 chips 401.

FIG. 4B shows a dielectric substrate 404 having a plurality of electrically conductive circuitry traces 405 partially covered by the solder mask 406. The traces 405 on the substrate extend to via holes 407 and split into a plurality of leads 408 which are bent toward inside of the via hole. The

holes 407 are arranged in such a manner that the terminal pads 402 of the integrated circuit chip 401 can be totally or partially exposed when integrated circuit chip 401 is mounted on the substrate 404. The bent leads 408 are to serve as electrically connecting channels for respective traces 405 of the substrate 404 with respective terminal pads 402 of the integrated circuit chips 401.

As shown in FIG. 4C, the substrate 404 is brought in contact with molten solder bath (Sn-Pb) from the surface where there is no circuitry thereon. Solder 409 is readily deposited onto the leads 407 the moment they are in contact with the molten solder bath.

As shown in FIG. 4D, the IC chip is next securely attached to the substrate circuitry by adhesive paste ABLESTIK "ABLEBOND 961-2" (trademark) 410.

FIG 4E shows the solder 409 wet on the IC terminal pad after the assembly is re-flowed under a conventional re-flow oven, and form an integrated part of a solder joint.

FIG. 4F shows the solder ball 411 is attached to the substrate at the opening site of the solder mask to provide the finished assembly for the next level connection.

Though only one solder system is shown in the figure, it is to be understood that many solder systems including lead-free ones, can also be applied and serve the connection purpose.

The present invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The

presently disclosed embodiments are, therefore, to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are, therefore, to be
5 embraced therein.

I claim:

1. A flip chip assembly, comprising:

(a) a dielectric substrate having a plurality of via holes;

5 (b) the said dielectric substrate having a first and second
opposite surfaces and a plurality of electrically conductive traces
being formed on the first surface of the said dielectric substrate, each
one of the said traces are extended into the specific said via holes
through at least one lead but preferable a plurality of leads which
10 fabricated on the top of and bent into the said via holes;

(c) a semiconductor device having a first surface and a plurality of
input/output terminal pads with a stack of metal film formed thereon;

(d) the said substrate is attached on the said semiconductor device
from the second surface and the via holes of the said substrate are
15 aligned on the top of the said terminal pads so that at least one of the
said terminal pads can be totally or partially exposed through the said
via holes from the said first surface of the said substrate;

(e) the electrical continuity of the said substrate to the said
semiconductor device is achieved by depositing conductive material
20 on the said bent leads of the substrate as well as to the said terminal
pads of the said semiconductor device therefore jointly form an
integral part in the said assembly.

2. The dielectric material of the said substrate according to claim 1(a), is
made of plastics.



3. The dielectric material of the said substrate according to claim 1(a), is the flexible film.
4. The dielectric material of the said substrate according to claim 1(a), is made of ceramics.
- 5 5. The via holes of the said substrate according to claim 1(b), are fabricated by at least one method from the group of laser drilling, mechanical punching, plasma etching or chemical etching.
6. The bent leads on the said substrate according to claim 1(b) are fabricated by photolithographic patterning and etching.
- 10 7. The bent leads on the said substrate according to claim 1(b) are fabricated by laser cutting.
8. The said a stack of metal film according to claim 1(c), is deposited by sputtering process.
9. The said a stack of metal film according to claim 1(c), is deposited by
- 15 evaporation process.
10. The said a stack of metal film according to claim 1(c), is deposited by electroless plating.
11. The attachment of the said semiconductor device to the said dielectric substrate according to claim 1(d), is adhesive film.
- 20 12. The attachment of the said semiconductor device to the said dielectric substrate according to claim 1(d), is adhesive paste.
13. The attachment of the said semiconductor device to the said dielectric substrate according to claim 1(d) is by mechanical clamping.



14.The deposition technique according to claim 1(e), is electrolytic plating.

15.The deposition technique according to claim 1(e), is electroless (chemical) plating.

5 16.A flip chip assembly, comprising:

(a) a dielectric substrate having a plurality of via holes;

(b) the said dielectric substrate having a first and second opposite surfaces and a plurality of electrically conductive traces being formed on the first surface of the said dielectric substrate, each one of the said traces are extended into the specific said via hole through at least one lead but preferable a plurality of leads which fabricated on the top of and bent into the said via holes;

10

(c) the said bent lead or leads extended from the said circuitry traces have at least one soldering material deposited thereon;

(d) a semiconductor device having a first surface and a plurality of input/output terminal pads with a stack of metal film deposited thereon;

15

(d) the said substrate is attached on the said semiconductor device from the second surface and the via holes of the said substrate are aligned on the top of the said terminal pads so that at least one of the said terminal pads can be totally or partially exposed through the said via holes from the said first surface of the said substrate;

20

(e) the electrical continuity of the said substrate to the said semiconductor device is achieved by solder re-flowing process so



that the pre-coated solder on the said bent leads contact and wet the said terminal pads of the said IC chip thus providing electrical connection between the said semiconductor device and at least one of the traces on the said substrate.

- 5 17.The integrated circuit assembly according to claim 15(c), wherein said soldering material on the leads is deposited by electroplating.
- 18.The integrated circuit assembly according to claim 15(c), wherein said soldering material on the leads is deposited by electroless plating.
- 10 19.The integrated circuit assembly according to claim 15(c), wherein said soldering material on the leads is deposited by wave soldering.
- 20.The integrated circuit assembly according to claim 15(c), wherein said soldering material on the leads is deposited by solder paste printing.
- 15 21.The integrated circuit assembly according to claim 15(c), wherein said soldering material on the leads is deposited by meniscus coating.



BUMPLESS FLIP CHIP ASSEMBLY WITH STRIPS-IN-VIA AND PLATING

ABSTRACT

5

A flip chip assembly, and methods of forming the same, including a single or multi-layer substrate having a plurality of via holes of which the pre-formed strips or wires inside the via holes serve as the connections between semiconductor device and substrate circuitry is described. The assembling steps comprise of attaching an integrated circuit (IC) chip or chips to a rigid or flexible substrate circuitry having a plurality of pre-formed strips extended from the patterned circuitry and hanging inside a plurality of through holes. These through holes are aligned and placed on top of the terminal pads so that the respective traces on substrate can be connected with the respective input/output terminal pads of the IC chip through the leads inside the via holes. After attachment, electrically conductive material is subsequently connect these leads to the IC terminal pads through electrolytic plating, electroless (chemical) plating or solder re-flow processes. The joining material can provide mechanical support as well as electrical continuity between IC chip and the circuitry of the substrate.

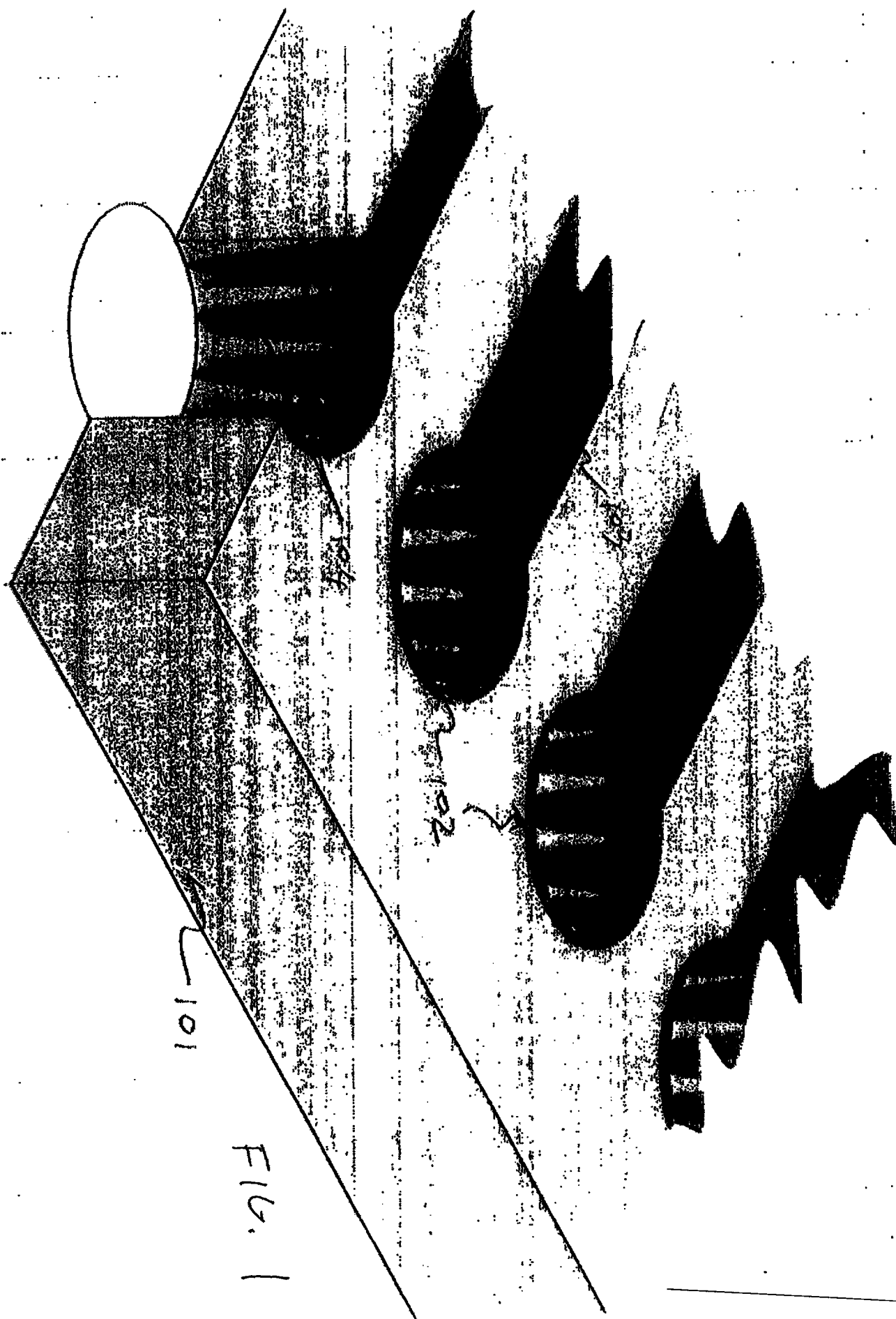
10

15

20

FIG. 2E

1/17



This Sheet Has Been Replaced



2/17

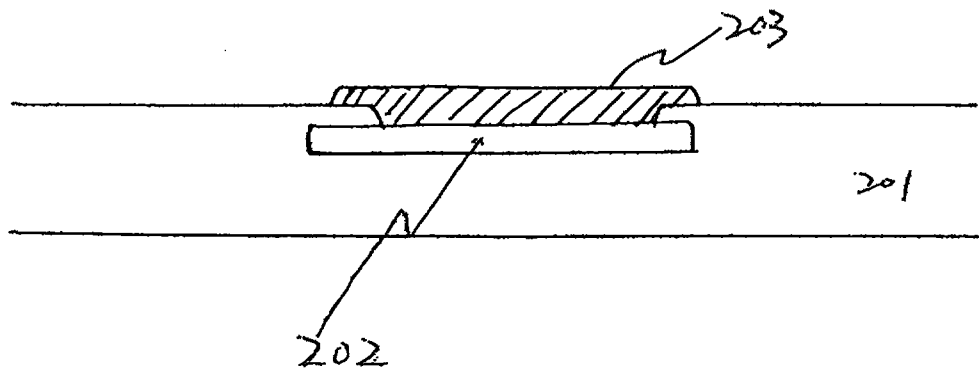


FIG. 2(A)

This Sheet Has Been Replaced



3/17

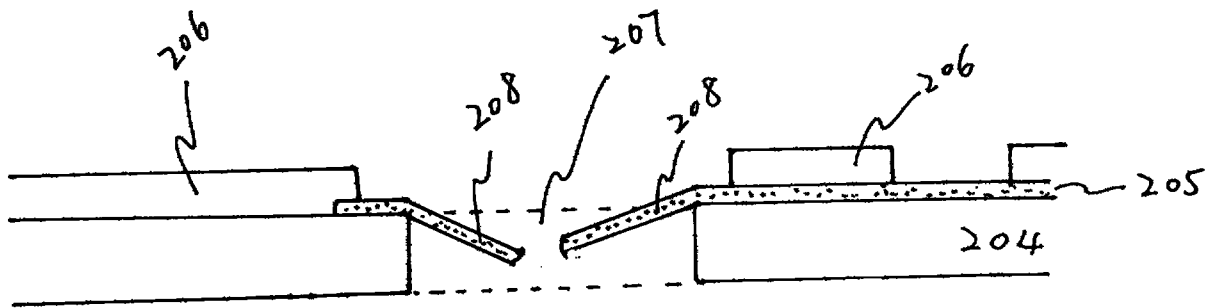


FIG 2B

This Sheet Has Been Replaced



4/17

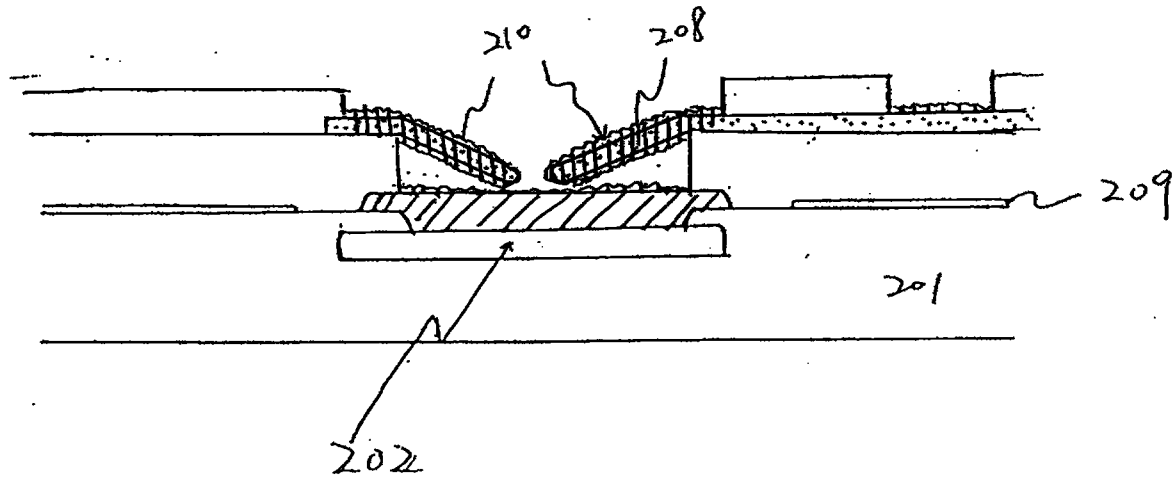


FIG. 2C

This Sheet Has Been Replaced



5/17

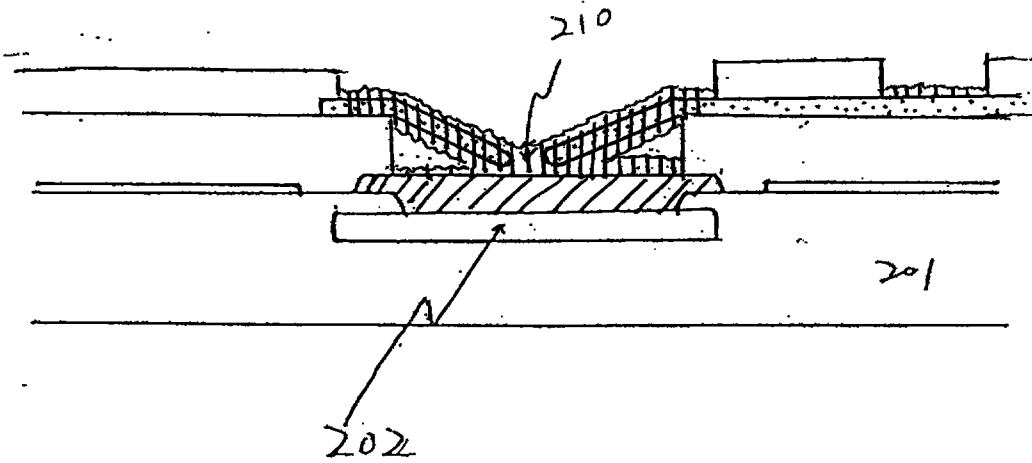


FIG. 2D

This Sheet Has Been Replaced



6/17

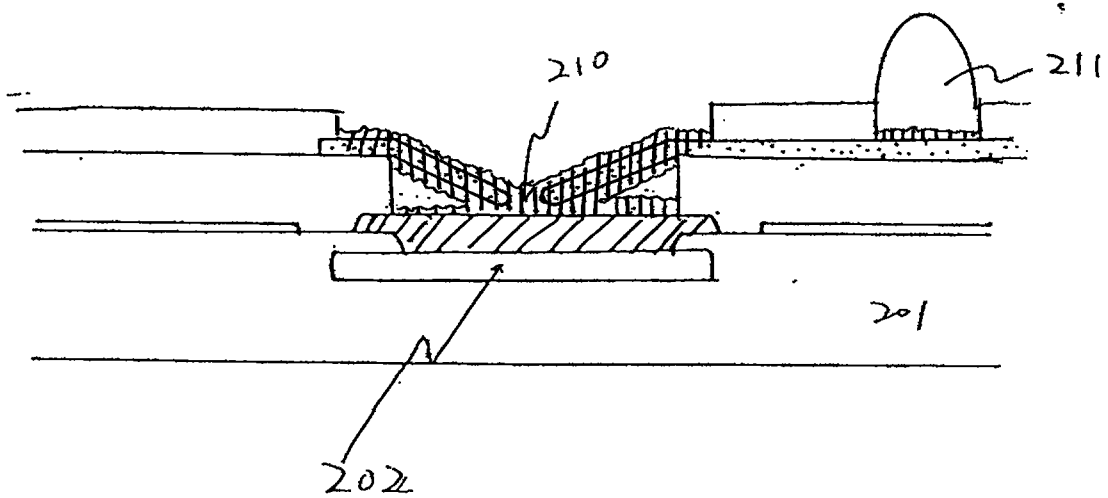


FIG. 2(E)

This Sheet Has Been Replaced

7/17

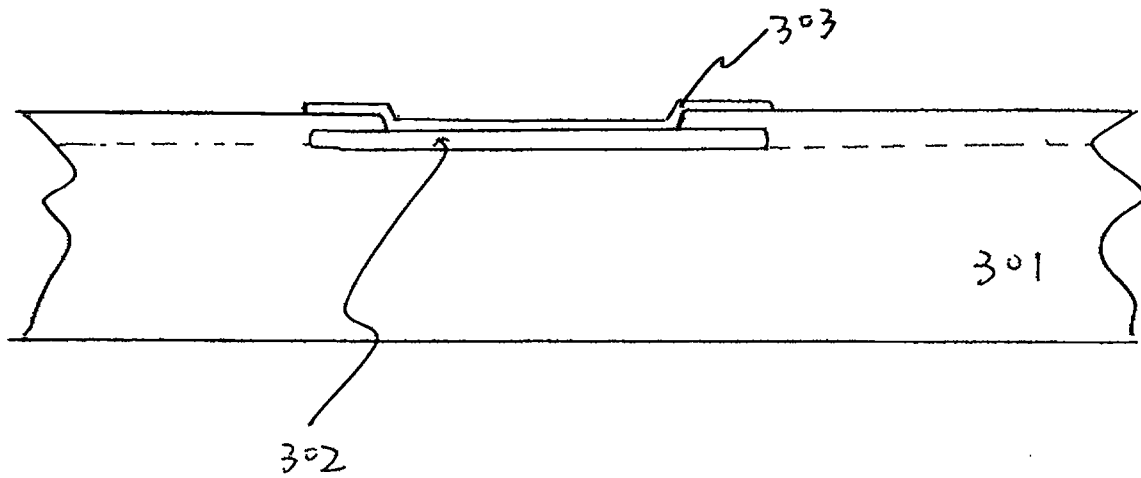


FIG. 3A

This Sheet Has Been Replaced



8/17

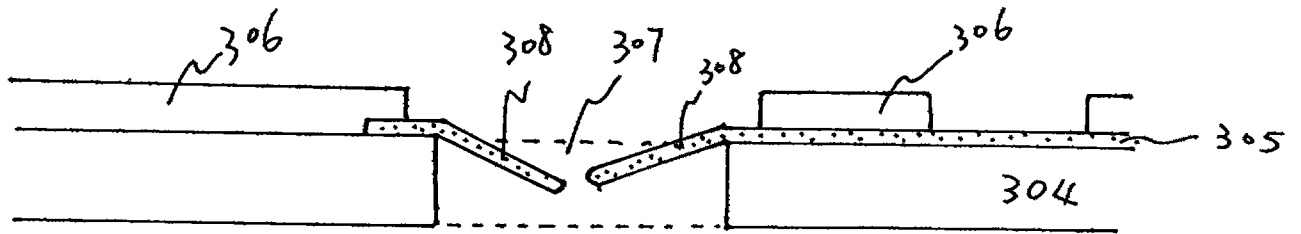


FIG. 3B

This Sheet Has Been Replaced



9/17

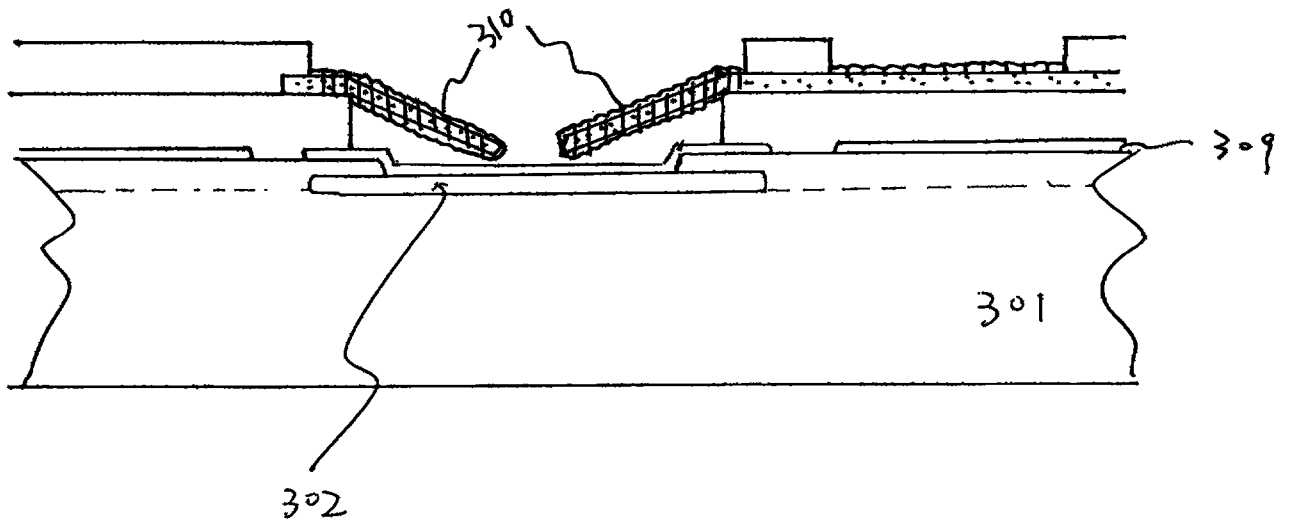


FIG. 3(c)

This Sheet Has Been Replaced



10/17

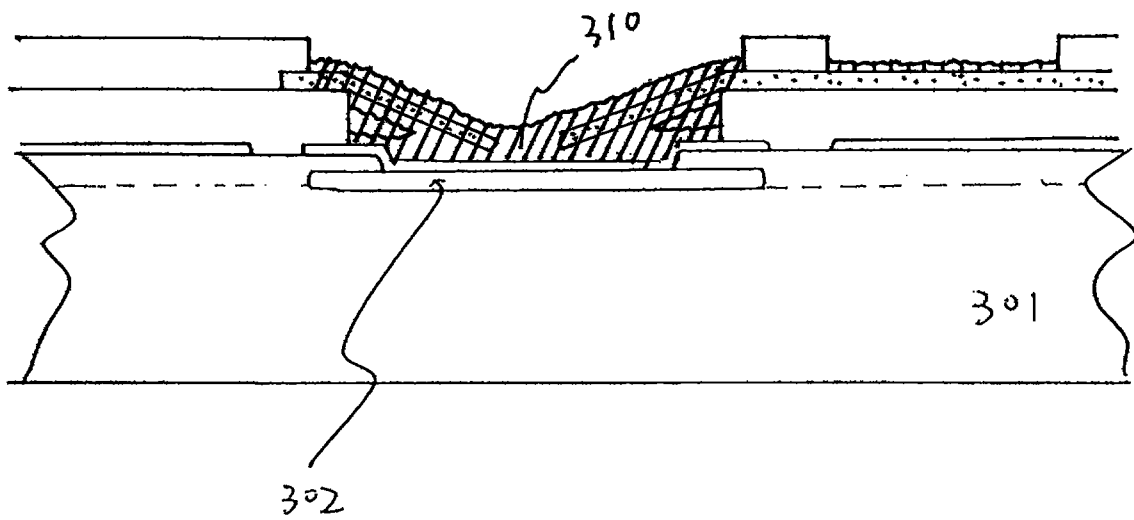


FIG. 3D

This Sheet Has Been Replaced



11/17

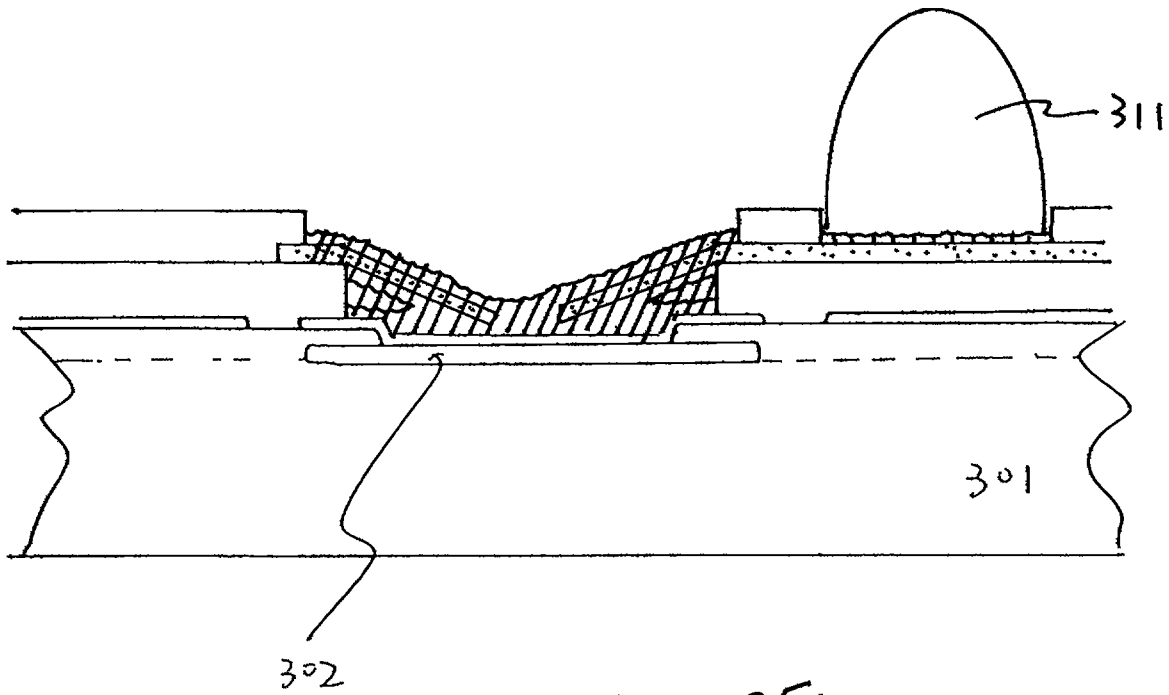


FIG. 3E

This Sheet Has Been Replaced



12/17

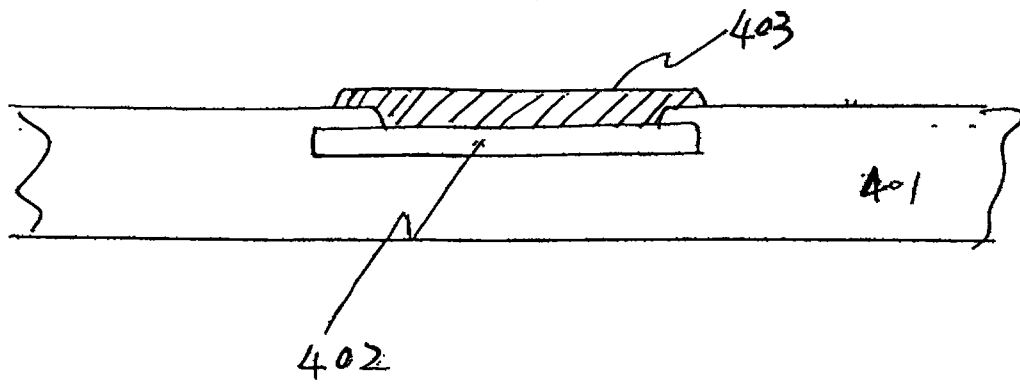


FIG. 4A

This Sheet Has Been Replaced



13/17

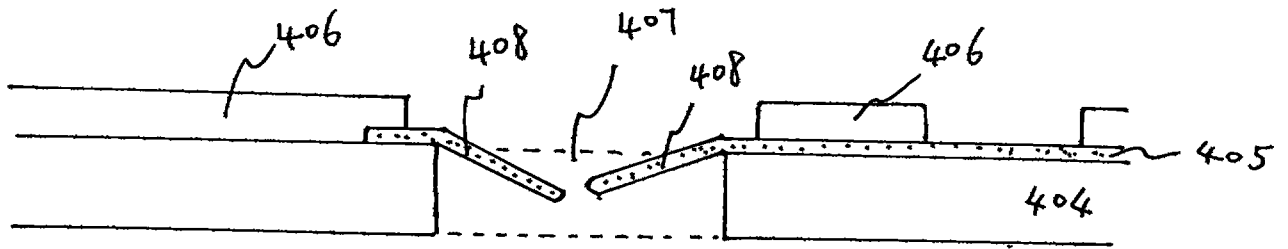


FIG. 4B

This Sheet Has Been Replaced



14/17

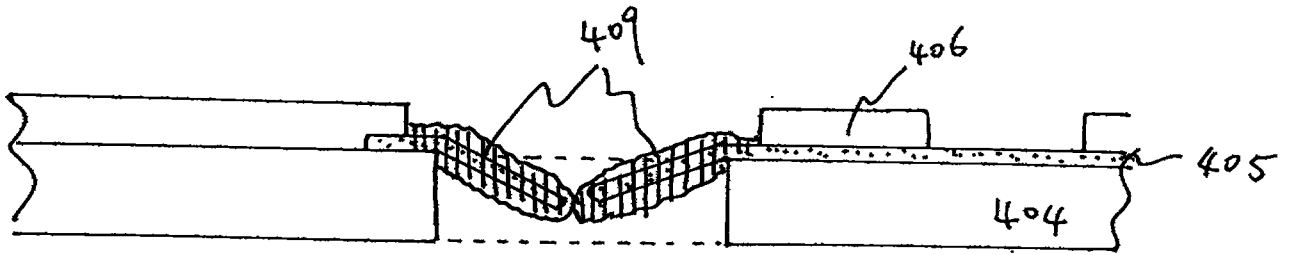


FIG. 4C



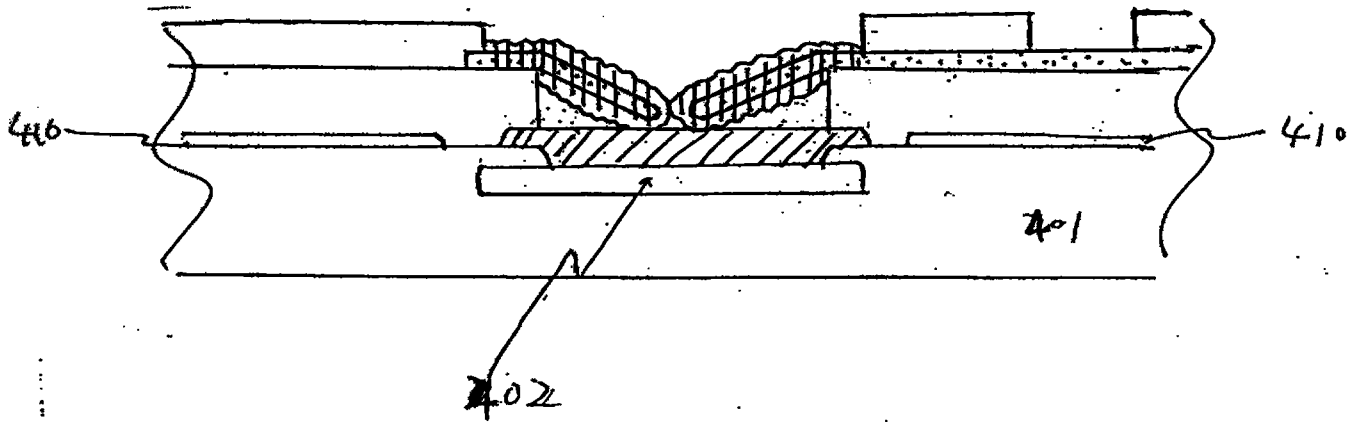
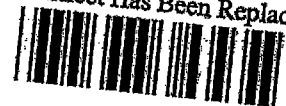


FIG. 4D



16/17

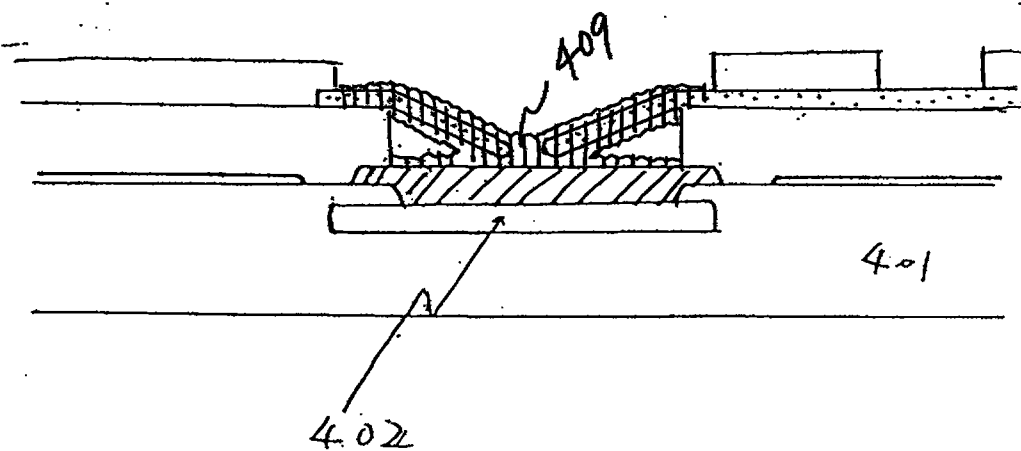


FIG. 4E

This Sheet Has Been Replaced



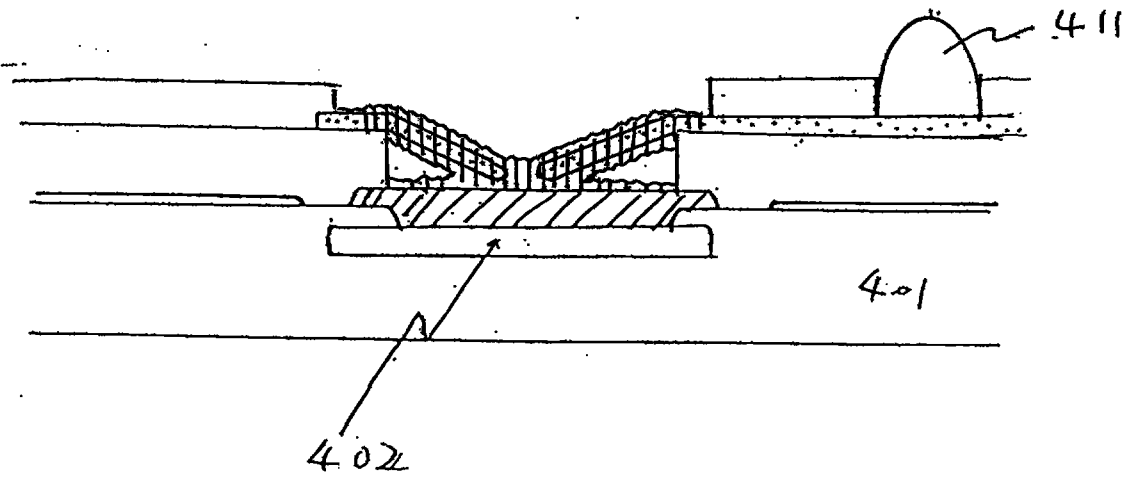


FIG. 4F



23 APR 1999

1/9

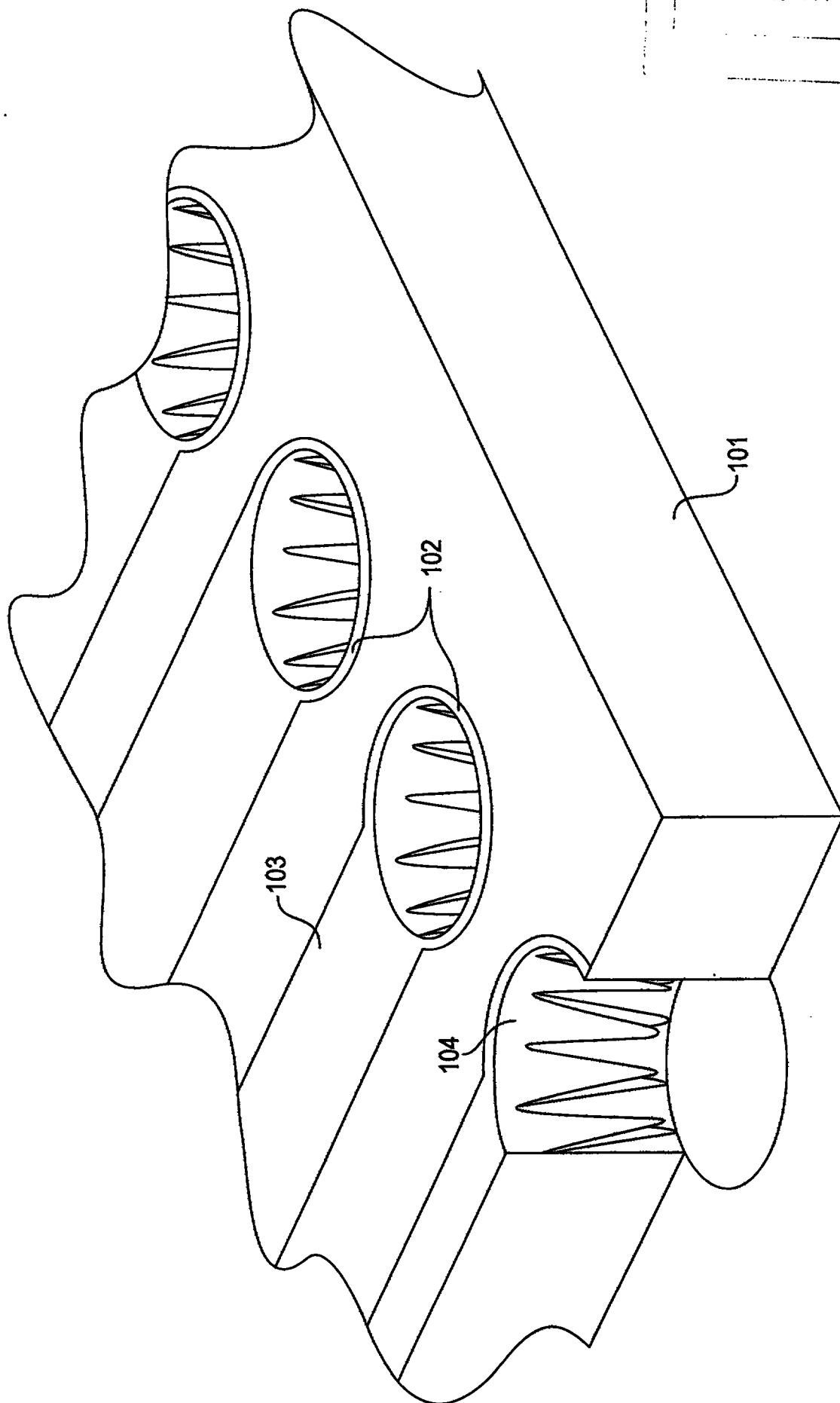


FIG. 1

23 APR 1999

2/9

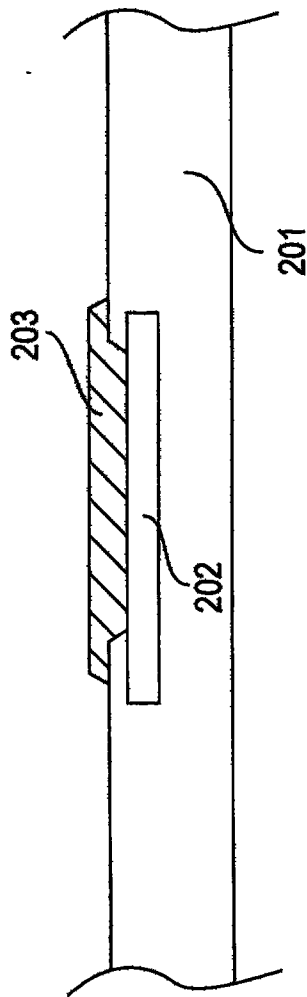


FIG. 2A

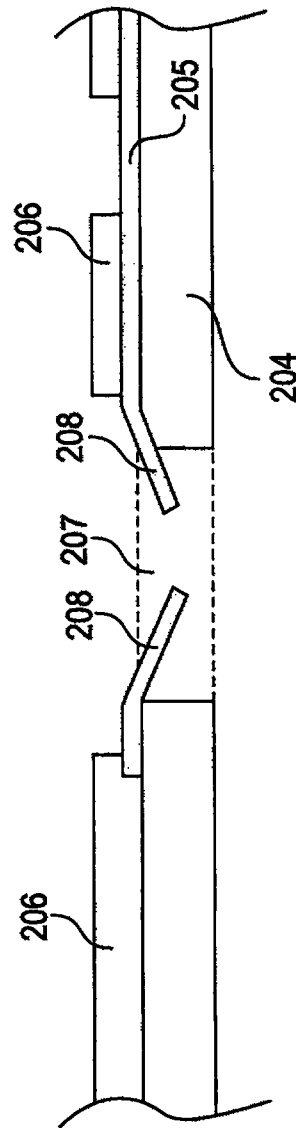


FIG. 2B

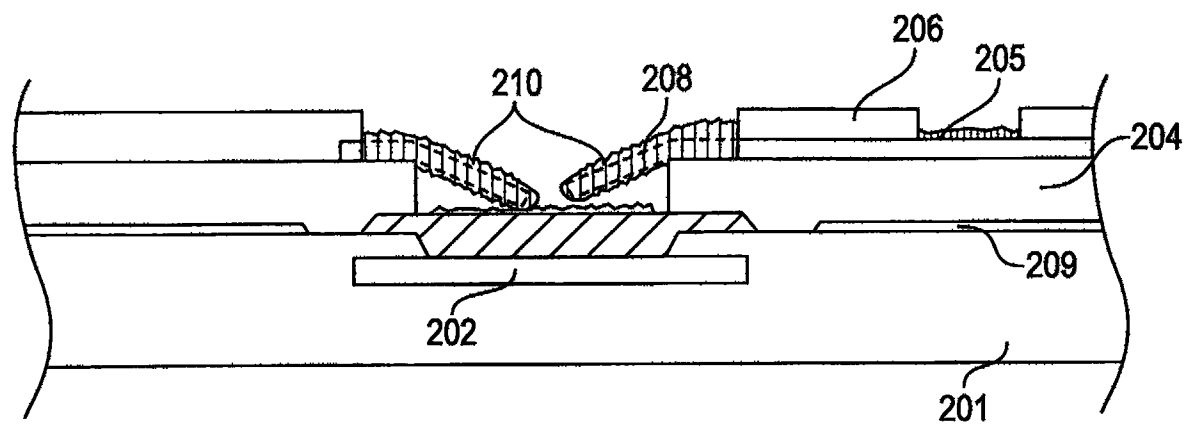


FIG. 2C

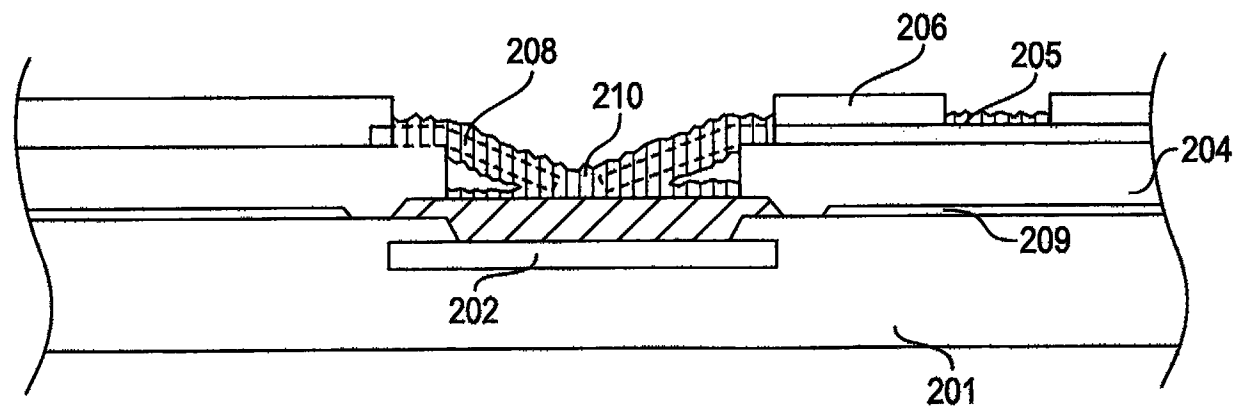


FIG. 2D

23 APR 1999

4/9

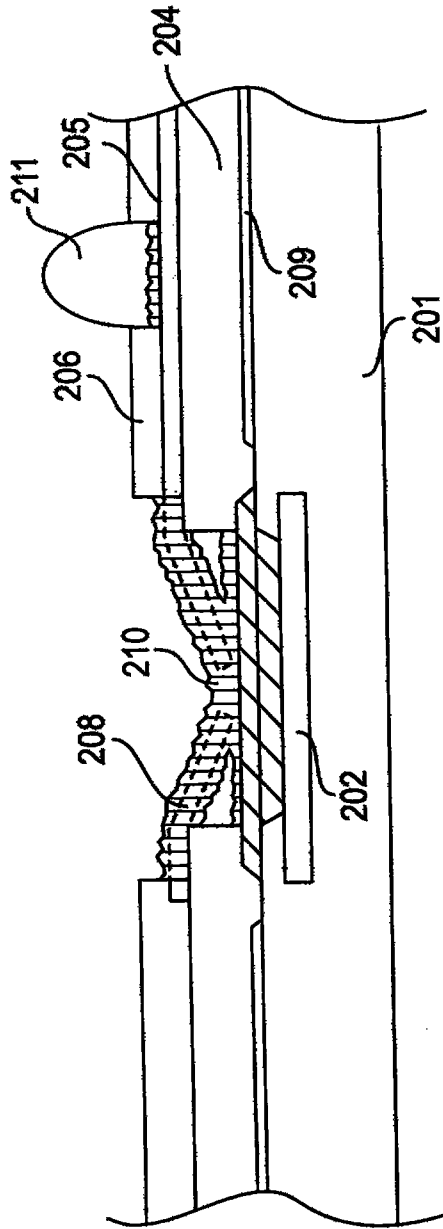


FIG. 2E

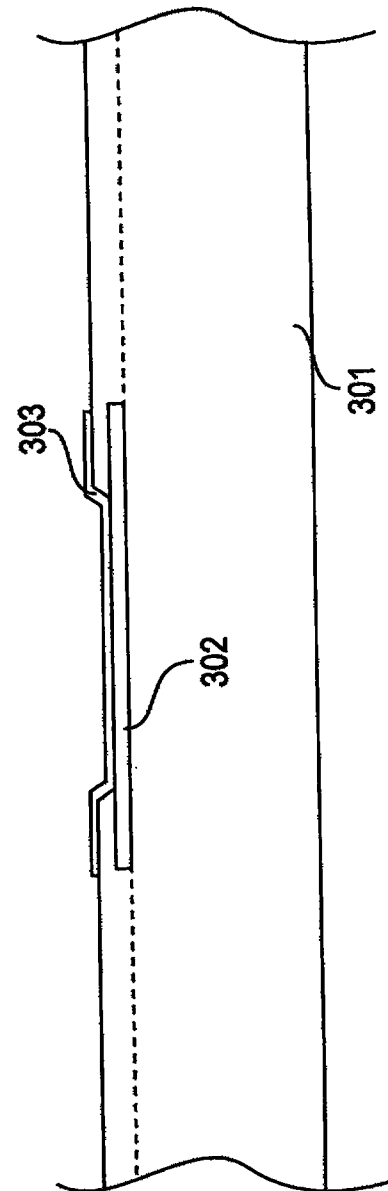


FIG. 3A

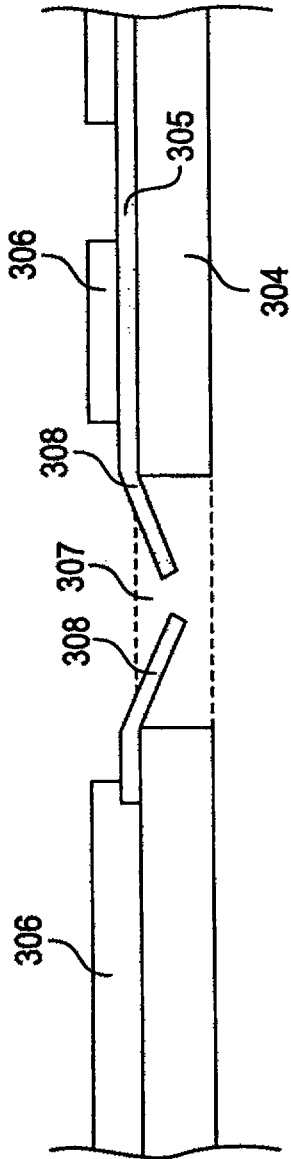


FIG. 3B

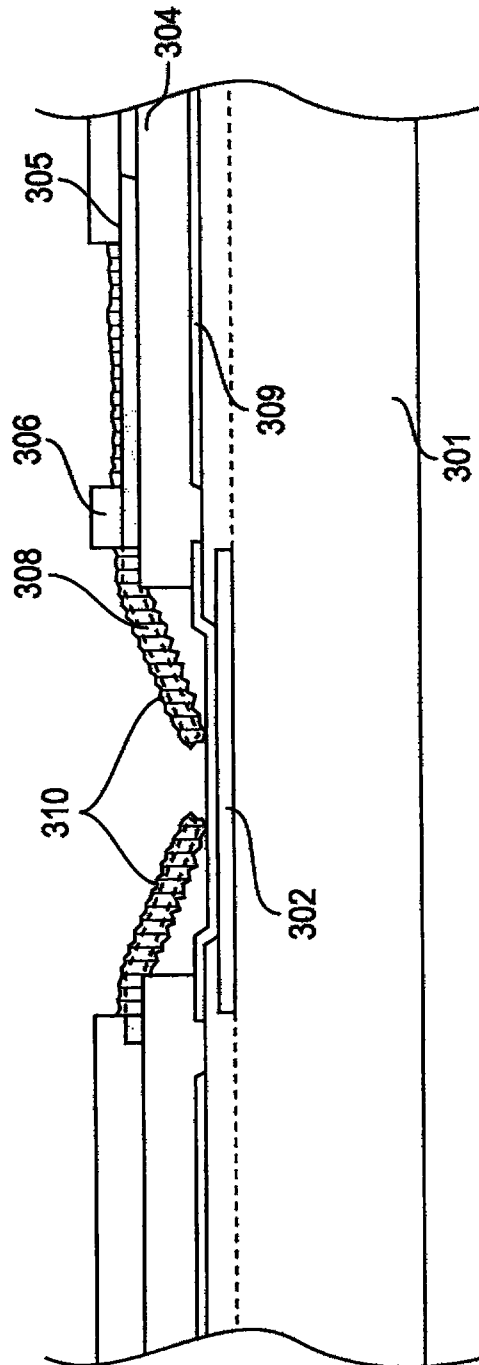


FIG. 3C

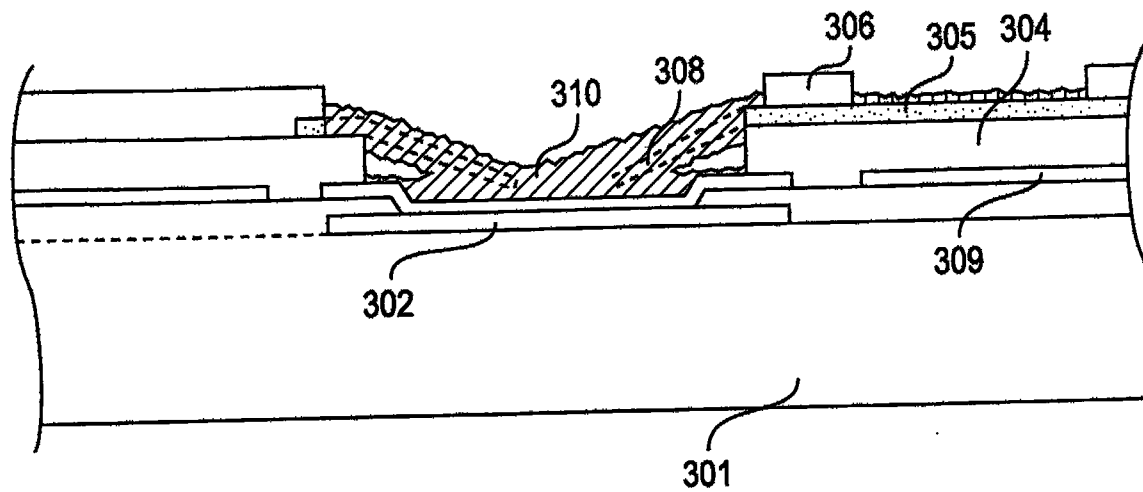


FIG. 3D

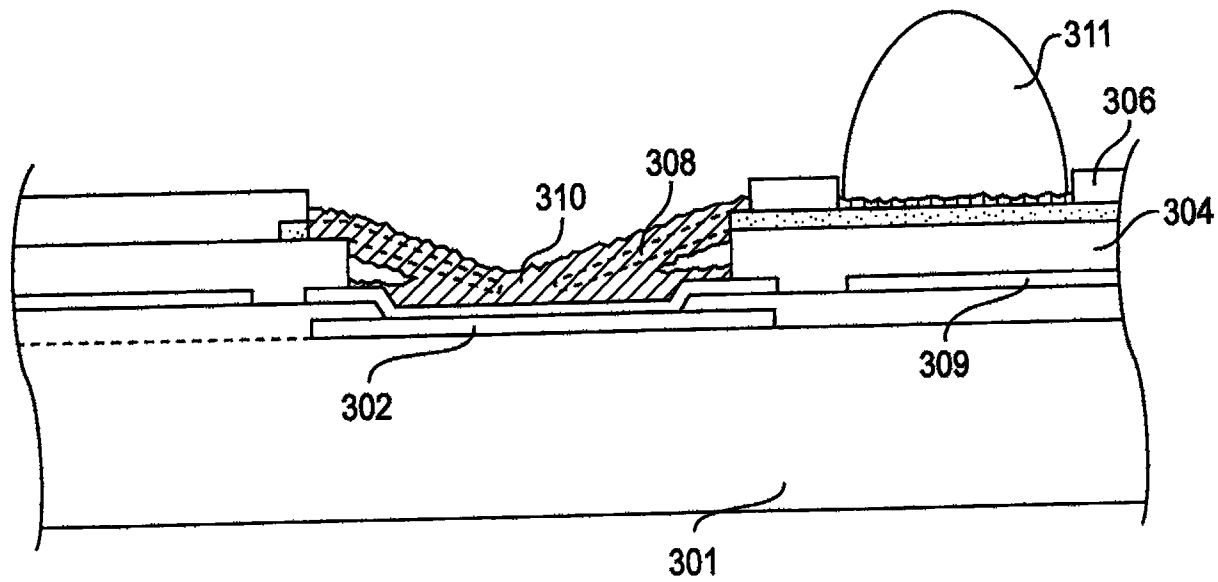


FIG. 3E

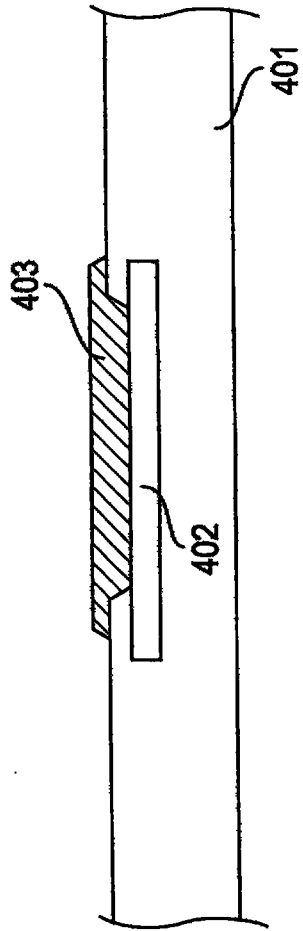


FIG. 4A

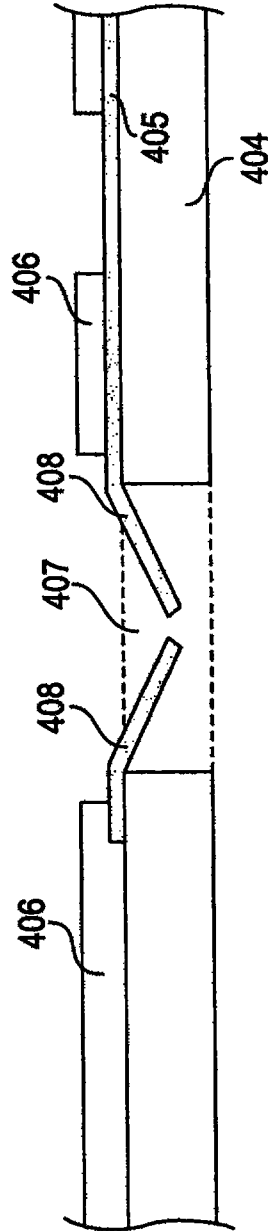


FIG. 4B

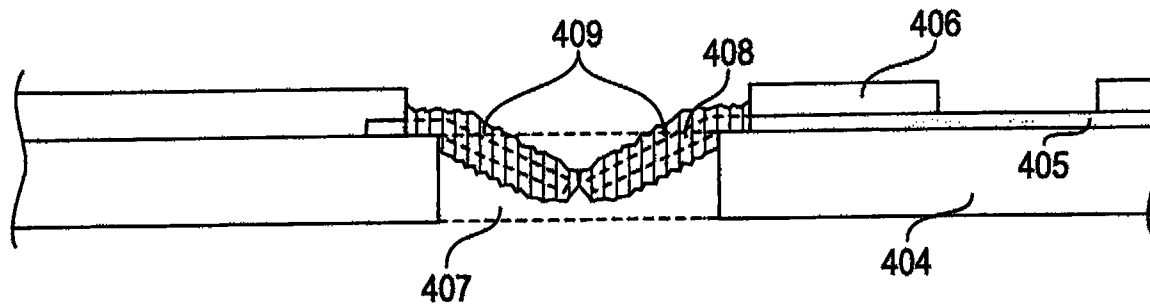


FIG. 4C

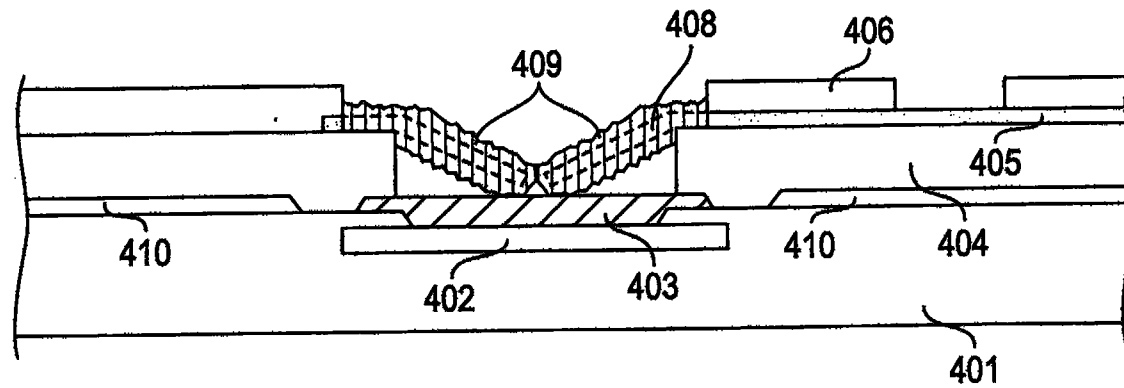
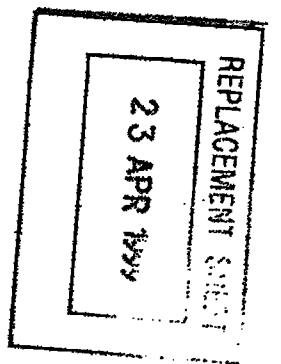


FIG. 4D



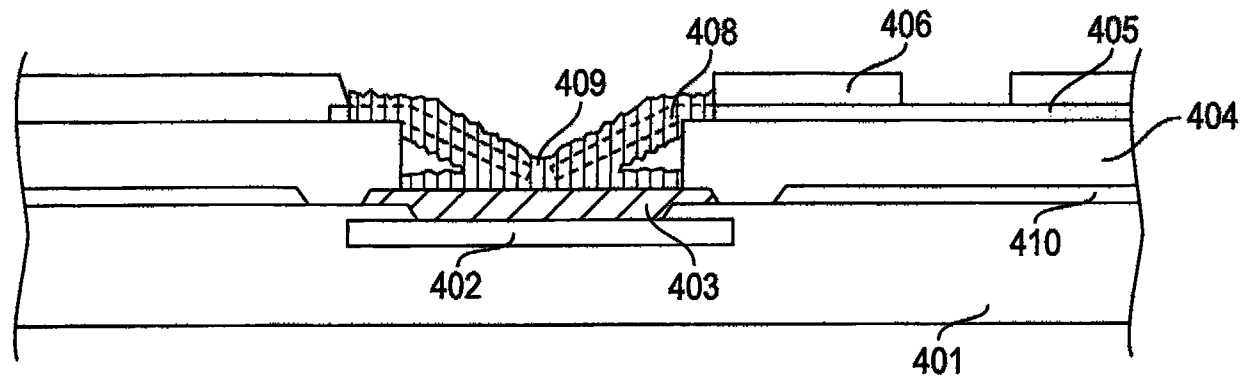


FIG. 4E

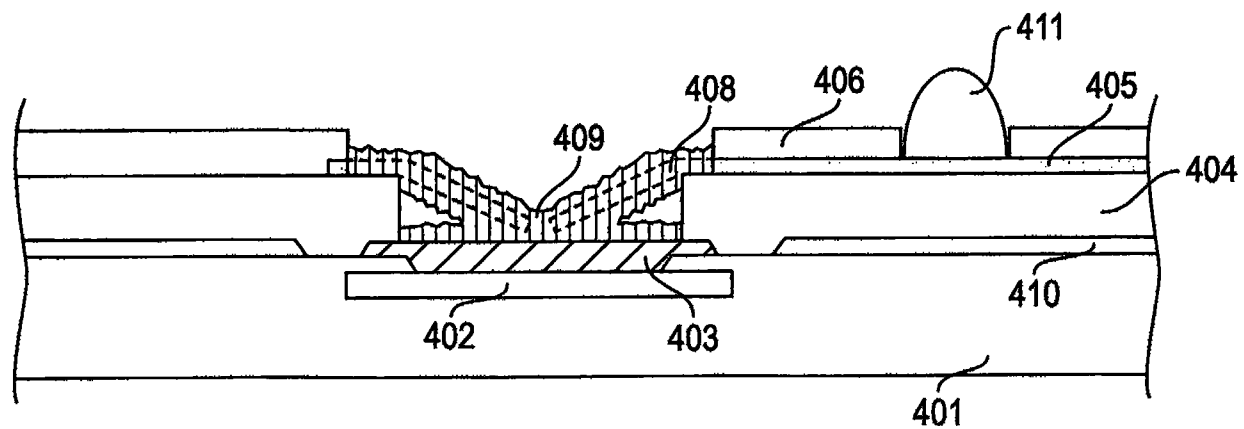


FIG. 4F