

COOLING AND COMPRESSION CLAMP FOR SHORT LEAD POWER DEVICES

CROSS REFERENCE TO RELATED APPLICATIONS

5 **[0001]** This application is a PCT application that claims priority to U.S. Utility Application No. 16/115,692, filed on August 29, 2018 and also claims the benefit of U.S. Provisional Application No. 62/567,505, filed on October 3, 2017. The entire disclosures of the above applications are incorporated herein by reference.

FIELD

10 **[0002]** The present disclosure relates to a cooling and compression clamp for electrical connections subject to repeated power and thermal cycling.

BACKGROUND

15 **[0003]** This section provides background information related to the present disclosure, which is not necessarily prior art.

20 **[0004]** Solder fatigue may occur at soldered electrical connections that experience repeated thermal expansion and contraction during normal use. Solder fatigue is a common challenge for radio frequency (RF) power conversion systems, which experience thousands to millions of power cycles during their application lifetime (*e.g.*, RF plasma generators used in semiconductor manufacturing). Critical parameters that determine the ultimate lifetime of a solder joint include temperature excursion (ΔT), and mechanical strain induced by coefficient of thermal expansion (CTE). Repeated power and/or thermal cycling can cause the solder to creep and possibly fracture, causing a high resistance connection and potential connection failure.

25 **[0005]** While such current solder connections are suitable for their intended use, they are subject to improvement. The present teachings include a cooling and compression clamp for short lead power devices that advantageously reduces solder fatigue. The present teachings provide for
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numerous additional advantages and unexpected results, as explained in detail herein and as one skilled in the art will appreciate.

SUMMARY

5 **[0006]** This section provides a general summary of the disclosure, and is not a comprehensive disclosure of its full scope or all of its features.

10 **[0007]** The present teachings include a clamp configured to be coupled to a printed circuit board to cool and compress one or more electrical connections subject to repeated power and thermal cycling. A first conductive column of the clamp is configured to compress a first electrical connection between a first power device lead and a first printed circuit board trace of the printed circuit board, and draw thermal energy away from the first power device lead. The first conductive column extends from a load spreading plate. The load spreading plate is an insulator that electrically isolates a fastener extending therefrom from the first conductive column. The fastener is
15 configured to cooperate with the circuit board to connect the clamp to the circuit board, compress the load spreading plate against the first conductive column to compress the first electrical connection, and connect the clamp to ground.

20 **[0008]** The present teachings further include a clamp configured to be coupled to a printed circuit board to cool and compress one or more electrical connections subject to repeated power and thermal cycling. The clamp includes a conductive column configured to compress an electrical connection between a drain lead from a transistor of a transistor package and a printed circuit board trace that supplies energy to an RF plasma output network. The
25 conductive column is also configured to draw thermal energy away from the first drain lead to cool the first drain lead. The conductive column extends from a load spreading plate. A fastener extends from the load spreading plate, which is an insulator that electrically isolates the fastener from the conductive column. The fastener is configured to: cooperate with the circuit
30 board to connect the clamp to the circuit board; and compress the load spreading plate against the conductive column to compress the electrical connection.

[0009] The present teachings also include a circuit board for an RF plasma generator that provides solid state power for thin films processing equipment. The circuit board includes a first transistor mounted to the circuit board with a retention member. A first drain lead extends from the first transistor. A first printed circuit board trace is for supplying energy to an RF plasma output network. The first printed circuit board trace is connected to the first drain lead to provide a first electrical connection therebetween. A first conductive column compresses the first electrical connection between the first printed circuit board trace and the first drain lead, and is configured to draw thermal energy away from the first drain lead to cool the first drain lead. The first column extends from a load spreading plate. A fastener extends from the load spreading plate. The load spreading plate is an insulator that electrically isolates the fastener from the first conductive column. The fastener is configured to: cooperate with the circuit board to connect the clamp to the circuit board; and to compress the load spreading plate against the first conductive column to compress the first electrical connection.

[0010] Further areas of applicability will become apparent from the description provided herein. The description and specific examples in this summary are intended for purposes of illustration only and are not intended to limit the scope of the present disclosure.

DRAWINGS

[0011] Figure 1 illustrates a clamp in accordance with the present teachings, which is coupled to a printed circuit board to cool and compress electrical connections subject to repeated power and thermal cycling; and

[0012] Figure 2 is an isolated perspective view of the clamp of Figure 1.

[0013] Corresponding reference numerals indicate corresponding parts throughout the several views of the drawings.

DETAILED DESCRIPTION

[0014] Figures 1 and 2 illustrate a cooling and compression clamp 10 in accordance with the present teachings. The clamp 10 is configured to be coupled to a printed circuit board 110 to cool and compress one or more electrical connections subject to repeated power and thermal cycling. The clamp 10 includes the first column 12A. The first column 12A is made of any suitable conductive metal, such as copper. In the example illustrated, the column 12A includes a leg 14A and a foot 16A, which is generally a base of the column 12A. An undersurface 18A of the foot 16A contacts an electrical connection in order to compress the electrical connection and conduct thermal energy from the connection, as explained herein. To accommodate the electrical connection, the undersurface 18A may define a recess 20A.

[0015] To facilitate dispersion of thermal energy from the column 12A, and ultimately from the electrical connection, the column 12A may include one or more thermal energy dispersion surfaces. The thermal energy dispersion surfaces may be located at any suitable position about the column 12A, such as along the leg 14A. The thermal dispersion surfaces can be any suitable surface feature to facilitate release of thermal energy conducted to the column 12A from the electrical connection. In the example illustrated, the thermal energy dispersion surfaces are in the form of first grooves 22A.

[0016] In the example illustrated, the clamp 10 further includes a second column 12B in addition to a first column 12A. The second column 12B can be the same as, or similar to, the first column 12A. Therefore, the description of the first column 12A also describes the second column 12B. The features of the second column 12B that are the same as, or similar to, the features of the first column 12A are designated in the drawings with the same reference numerals, but with the suffix "B" rather than "A."

[0017] Although the clamp 10 is illustrated as including both the first column 12A and the second column 12B, the clamp 10 can be provided with only a single column or more than two columns. For example, Figure 1 illustrates a transistor package 130 in the form of a Gemini package, which has two electrical connections associated therewith, as explained further herein. Thus the exemplary clamp 10 of Figure 1 includes two columns 12A and 12B – one for each electrical connection to be compressed and cooled.

The number of columns that the clamp 10 includes will generally correspond to the number of electrical connections to be compressed and cooled.

[0018] The clamp 10 further includes a load spreading plate 30. The load spreading plate 30 is an insulator, and can be made of any suitable insulative material, such as fiberglass. Both the first column 12A and the second column 12B extend from the plate 30. The first and second columns 12A and 12B are connected to the plate 30 in any suitable manner. For example, the clamp 10 can be preassembled as a single unit with the first and second columns 12A and 12B attached to the load spreader plate 30 by way of pin pressing and riveting. The plate 30 defines a bore 32, which extends through the plate 30. The bore 32 is sized and shaped to receive any suitable fastener 40 configured to secure the clamp 10 to the circuit board 110. In the example illustrated, the fastener 40 is a screw including a head 42 and a shaft 44, which extends from the head 42. Between the fastener 40 (specifically the head 42 thereof) and the plate 30 is a compression member 50. The compression member 50 can be any suitable compression member, such as a washer or spring, which facilitates compression of the plate 30 against the columns 12A and 12B to press the columns 12A and 12B onto the electrical connections. If the first column 12A, the second column 12B, and the fastener 40 are at the same electrical potential, the plate 30 may alternatively be constructed as a conductive material.

[0019] At a distal end of the shaft 44 are threads 46, which cooperate with a receptacle of the circuit board 110 in order to secure the clamp 10 to the circuit board 110. The shaft 44 connects to ground in order to ground the clamp 10. The plate 30 advantageously electrically isolates the fastener 40 from the first column 12A and the second column 12B. The plate 30 also isolates RF and DC signals.

[0020] As illustrated in Figure 1, the clamp 10 is positioned such that the first column 12A is seated over a first electrical connection made between a first power device lead 112A and a first printed circuit board trace (or suitable metal surface) 114A. The second column 12B is arranged over a second electrical connection between a second power device lead 112B and a second printed circuit board trace 114B (or suitable metal surface). The electrical connection between the first power device lead 112A and the first

printed circuit board trace 114A, as well as the electrical connection between the second power device lead 112B and the second printed circuit board trace 114B, can be any suitable electrical connection, such as any suitable solder or solderless electrical connection.

5 **[0021]** In the example illustrated, the first power device lead 112A is a first drain (or source) lead from the transistor package 130, and specifically a first transistor 132A thereof. The second power device lead 112B is a second drain (source) lead from a second transistor 132B of the transistor package 130. A first input or gate lead 134A is connected to the first
10 transistor 132A, and a second input or gate lead 134B is connected to the second transistor 132B. The transistor package 130 further includes a lid 140, which covers the first transistor 132A and the second transistor 132B. The lid 140 is secured to the circuit board 110 in any suitable manner, such as with a first retention member 142A and a second retention member 142B. In
15 the example illustrated, the first printed circuit board trace 114A and the second printed circuit board trace 114B supply power to a plasma chamber 210 for semiconductor manufacturing.

[0022] The transistor package 130 is illustrated as a Gemini-style package configured in a push-pull configuration for wideband, low distortion
20 operation. However, any other suitable transistor package can be used. For example, a transistor package including only a single transistor may be used, or multiple transistors can be formed on a single die. The transistor package 130, the first power device lead 112A, the second power device lead 112B, the first input lead 134A and the second input lead 134B, are included with an
25 RF power supply 150. The RF power supply 150 can be any power supply suitable for providing power to the plasma chamber 210 in order to generate a waveform. The present teachings are applicable for use with any suitable RF plasma generators, such as any suitable VHF generator. The clamp 10 can also be used with an MKS EDGE™ platform generator.

30 **[0023]** With the clamp 10 arranged as illustrated in Figure 1, when the fastener 40 is screwed to the circuit board 110, the fastener 40 compresses the plate 30 against the first and second columns 12A and 12B, which compresses the first column 12A against the first power device lead 112A, and compresses the second column 12B against the second power

device lead 112B. The compression provided by the clamp 10 on the electrical connections is generally constant. This maintains the electrical connections between the first and second power device leads 112A, 112B and the first and second printed circuit board traces 114A, 114B respectively
5 (or any other suitable metal surfaces), even during large temperature fluctuations at the electrical connections, which may result in expansion and contraction of the connection. Furthermore, the clamp 10 advantageously draws thermal energy from the first and second power device leads 112A and 112B by conduction through the first and second columns 12A and 12B,
10 which reduces the temperature of the first and second power device leads 112A and 112B, thereby reducing the possibility of solder fatigue and extending the life of each electrical connection. The columns 12A and 12B are made of high thermal conductive material, such as copper, which is an extremely good material for pulling heat energy from the leads 112A and
15 112B to the columns 12A and 12B. The energy accumulated in the copper is then radiated to the surrounding air by way of convection and forced air cooling. The clamp 10 also advantageously minimizes parasitic capacitance from the first and second power device leads 112A and 112B to ground, which maintains good RF performance.

20 **[0024]** To improve heat transfer between the first power device lead 112A and the first column 12A, a thermal interface material 50A may be arranged therebetween. Similarly, to improve heat transfer between the second power device lead 112B and the second column 12B, a thermal interface material 50B may be arranged therebetween. The thermal interface
25 materials 50A and 50B may be any suitable thermal interface materials. For example, the thermal interface materials 50A and 50B may each be a thin sheet (0.25-0.5mm thick) with adhesive on one side, which is cut to shape and adhered to the undersurfaces 18A and 18B of the columns 12A and 12B respectively.

30 **[0025]** The clamp 10 is particularly useful in applications where the first power device lead 112A and/or the second power device lead 112B is very short (such as 3.0mm), which would preclude use of a mechanical fastener, such as a screw, to secure the first and/or second power device leads 112A, 112B to their respective traces 114A, 114B. When the first and

second power device leads 112A and 112B are so short, it will also not be possible to form an omega (Ω) loop in the leads 112A, 112B, as is known in the art, to accommodate expansion and contraction of the first and second power device leads 112A and 112B during temperature fluctuations thereof

5 **[0026]** The clamp 10 advantageously reduces the temperatures of the first and second power source device leads 112A and 112B to reduce temperature fluctuations thereof, and maintains the clamp 10 compressed against the leads 112A and 112B to reduce the mechanical strain induced by repeated thermal expansion and contraction (coefficient of thermal expansion
10 (CTE)). As a result, incremental damage to the soldered connections, as estimated by the following formula, is reduced:

$$\Delta D = \left[\frac{F \cdot DNP \cdot \Delta CTE \cdot \Delta T}{h} \right]$$

In this equation: F = engineering factor, ~ 1.2 to 0.7 for filleted SJs, ~ 1.5 to 1.0 for SJs without fillets; DNP = distance from the neutral point/plane; ΔCTE = CTE mismatch; ΔT = cyclic temperature excursion; h = solder joint.

15 **[0027]** The foregoing description of the embodiments has been provided for purposes of illustration and description. It is not intended to be exhaustive or to limit the disclosure. Individual elements or features of a particular embodiment are generally not limited to that particular embodiment, but, where applicable, are interchangeable and can be used in a selected
20 embodiment, even if not specifically shown or described. The same may also be varied in many ways. Such variations are not to be regarded as a departure from the disclosure, and all such modifications are intended to be included within the scope of the disclosure.

[0028] The foregoing description is merely illustrative in nature and is
25 in no way intended to limit the disclosure, its application, or uses. The broad teachings of the disclosure can be implemented in a variety of forms. Therefore, while this disclosure includes particular examples, the true scope of the disclosure should not be so limited since other modifications will become apparent upon a study of the drawings, the specification, and the
30 following claims. It should be understood that one or more steps within a method may be executed in different order (or concurrently) without altering the principles of the present disclosure. Further, although each of the

embodiments is described above as having certain features, any one or more of those features described with respect to any embodiment of the disclosure can be implemented in and/or combined with features of any of the other embodiments, even if that combination is not explicitly described. In other words, the described embodiments are not mutually exclusive, and permutations of one or more embodiments with one another remain within the scope of this disclosure.

[0029] Spatial and functional relationships between elements (for example, between modules, circuit elements, semiconductor layers, etc.) are described using various terms, including “connected,” “engaged,” “coupled,” “adjacent,” “next to,” “on top of,” “above,” “below,” and “disposed.” Unless explicitly described as being “direct,” when a relationship between first and second elements is described in the above disclosure, that relationship can be a direct relationship where no other intervening elements are present between the first and second elements, but can also be an indirect relationship where one or more intervening elements are present (either spatially or functionally) between the first and second elements. As used herein, the phrase at least one of A, B, and C should be construed to mean a logical (A OR B OR C), using a non-exclusive logical OR, and should not be construed to mean “at least one of A, at least one of B, and at least one of C.”

[0030] In the figures, the direction of an arrow, as indicated by the arrowhead, generally demonstrates the flow of information (such as data or instructions) that is of interest to the illustration. For example, when element A and element B exchange a variety of information but information transmitted from element A to element B is relevant to the illustration, the arrow may point from element A to element B. This unidirectional arrow does not imply that no other information is transmitted from element B to element A. Further, for information sent from element A to element B, element B may send requests for, or receipt acknowledgements of, the information to element A.

[0031] In this application, including the definitions below, the term “module” or the term “controller” may be replaced with the term “circuit.” The term “module” may refer to, be part of, or include: an Application Specific Integrated Circuit (ASIC); a digital, analog, or mixed analog/digital discrete circuit; a digital, analog, or mixed analog/digital integrated circuit; a

combinational logic circuit; a field programmable gate array (FPGA); a processor circuit (shared, dedicated, or group) that executes code; a memory circuit (shared, dedicated, or group) that stores code executed by the processor circuit; other suitable hardware components that provide the described functionality; or a combination of some or all of the above, such as in a system-on-chip.

[0032] The module may include one or more interface circuits. In some examples, the interface circuits may include wired or wireless interfaces that are connected to a local area network (LAN), the Internet, a wide area network (WAN), or combinations thereof. The functionality of any given module of the present disclosure may be distributed among multiple modules that are connected via interface circuits. For example, multiple modules may allow load balancing. In a further example, a server (also known as remote, or cloud) module may accomplish some functionality on behalf of a client module.

[0033] Some or all hardware features of a module may be defined using a language for hardware description, such as IEEE Standard 1364-2005 (commonly called "Verilog") and IEEE Standard 1076-2008 (commonly called "VHDL"). The hardware description language may be used to manufacture and/or program a hardware circuit. In some implementations, some or all features of a module may be defined by a language, such as IEEE 1666-2005 (commonly called "SystemC"), that encompasses both code, as described below, and hardware description.

[0034] The term code, as used above, may include software, firmware, and/or microcode, and may refer to programs, routines, functions, classes, data structures, and/or objects. The term shared processor circuit encompasses a single processor circuit that executes some or all code from multiple modules. The term group processor circuit encompasses a processor circuit that, in combination with additional processor circuits, executes some or all code from one or more modules. References to multiple processor circuits encompass multiple processor circuits on discrete dies, multiple processor circuits on a single die, multiple cores of a single processor circuit, multiple threads of a single processor circuit, or a combination of the above. The term shared memory circuit encompasses a single memory circuit that

stores some or all code from multiple modules. The term group memory circuit encompasses a memory circuit that, in combination with additional memories, stores some or all code from one or more modules.

[0035] The term memory circuit is a subset of the term computer-readable medium. The term computer-readable medium, as used herein, does not encompass transitory electrical or electromagnetic signals propagating through a medium (such as on a carrier wave); the term computer-readable medium may therefore be considered tangible and non-transitory. Non-limiting examples of a non-transitory computer-readable medium are nonvolatile memory circuits (such as a flash memory circuit, an erasable programmable read-only memory circuit, or a mask read-only memory circuit), volatile memory circuits (such as a static random access memory circuit or a dynamic random access memory circuit), magnetic storage media (such as an analog or digital magnetic tape or a hard disk drive), and optical storage media (such as a CD, a DVD, or a Blu-ray Disc).

[0036] The apparatuses and methods described in this application may be partially or fully implemented by a special purpose computer created by configuring a general purpose computer to execute one or more particular functions embodied in computer programs. The functional blocks and flowchart elements described above serve as software specifications, which can be translated into the computer programs by the routine work of a skilled technician or programmer.

[0037] The computer programs include processor-executable instructions that are stored on at least one non-transitory computer-readable medium. The computer programs may also include or rely on stored data. The computer programs may encompass a basic input/output system (BIOS) that interacts with hardware of the special purpose computer, device drivers that interact with particular devices of the special purpose computer, one or more operating systems, user applications, background services, background applications, etc.

[0038] The computer programs may include: (i) descriptive text to be parsed, such as HTML (hypertext markup language), XML (extensible markup language), or JSON (JavaScript Object Notation), (ii) assembly code, (iii) object code generated from source code by a compiler, (iv) source code

for execution by an interpreter, (v) source code for compilation and execution by a just-in-time compiler, etc. As examples only, source code may be written using syntax from languages including C, C++, C#, Objective-C, Swift, Haskell, Go, SQL, R, Lisp, Java®, Fortran, Perl, Pascal, Curl, OCaml, Javascript®, HTML5 (Hypertext Markup Language 5th revision), Ada, ASP (Active Server Pages), PHP (PHP: Hypertext Preprocessor), Scala, Eiffel, Smalltalk, Erlang, Ruby, Flash®, Visual Basic®, Lua, MATLAB, SIMULINK, and Python®.

[0039] None of the elements recited in the claims are intended to be a means-plus-function element within the meaning of 35 U.S.C. §112(f) unless an element is expressly recited using the phrase “means for,” or in the case of a method claim using the phrases “operation for” or “step for.”