

SINGLE OR MULTI-LAYER PRINTED CIRCUIT BOARD WITH RECESSED OR EXTENDED BREAKAWAY TABS AND METHOD OF MANUFACTURE THEREOF

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application claims priority from U.S. Patent Application Serial No. 10/184,387, filed June 27, 2002, entitled "Process for Creating Vias for Circuit Assemblies".

BACKGROUND OF THE INVENTION

[0002] Presently, printed circuit boards are fabricated as part of a larger panel. Each printed circuit board can be configured in any shape, although most printed circuit boards in common use are made in rectangular shapes of standard sizes. When fabrication of a printed circuit board is complete, it is cut and separated from the larger panel, mostly by way of a machine cutting or routing process in which a channel is cut around the printed circuit board. In certain designs, the channel around the printed circuit board does not completely encircle the perimeter of the printed circuit board. Rather, tabs are left at several places around the perimeter of the printed circuit board to attach it to the larger panel until the board is singulated from the larger panel by breaking the tabs. Typically, metal planes in the printed circuit board do not extend to its edge where they would be cut by the routing process. In this way, no conductive metal is left exposed on the edges of the printed circuit board.

[0003] The existing methods of cutting printed circuit boards from larger panels are unsatisfactory for high density boards because the limited dimensional stability of the printed circuit boards does not allow registration of one high density pattern to the next on the larger panel. Cut lines made around the periphery of the printed circuit board further weaken the panel material, exasperating misregistration of one pattern to the next.

[0004] Electronic systems assembled onto conventional printed circuit boards rely upon thermal conduction from integrated circuits dissipating heat to the printed circuit board to remove some of the heat from the integrated circuits. For intermediate ranges of heat, up to about 2 watts per chip, conduction to the printed circuit board is sufficient to cool the integrated circuits without the need for bulky and expensive heat sinks. In high performance systems, however, as the density of the system and the percentage of the substrate covered by the integrated circuits increases, the thermal path to the printed circuit board is less efficient. At a point when the density of the system increases sufficiently, the printed circuit board is not effective as a heat sink for the integrated circuits. However, the need for effective

thermal conduction from the integrated circuits to the substrate and therefrom to the ambient becomes more important as system density increases. Because of the evolution toward higher system density and larger integrated circuit coverage, means are needed for cooling the substrate in order to maintain the integrated circuits on the substrate at a safe operating temperature.

[0005] In addition to thermal conduction, high performance systems increasingly require low impedance power and ground voltage supplies to run the integrated circuits at high clock speeds. Typically, the AC impedances of power and ground supplies are lowered by the use of low impedance bypass capacitors connected to the power and ground planes. On conventional printed circuit boards, capacitors are connected to power and ground planes through vias which extend through some thickness of the board, increasing the impedance of this contact and degrading performance of the system. As switching speeds increase, the problem of making low impedance connections between bypass capacitors and the power and ground planes becomes more important.

[0006] It is, therefore, an object of the present invention to overcome the above problems and others by providing a printed circuit board having one or more printed circuit board layers having a conductive plane which extends to the edge of the printed circuit board but which is substantially, but not completely, covered by an insulating material. The edge of the conductive layer not covered by the insulating material can be on the edge of a tab which is utilized to couple the board to a disposable part of a larger panel that the board is formed from during fabrication. The exposed edge of the conductive layer becomes exposed upon breaking the tab and singulating the printed circuit board from the disposable part of the larger panel. In one embodiment, the tab terminates in a recess in the perimeter of the printed circuit board. In another embodiment, the tab extends outward from the perimeter of the printed circuit board.

[0007] The conductive plane can be formed from metal, such as a copper foil, that can serve the dual purpose of conducting heat away from electrical components disposed on one or both surfaces of the printed circuit board or printed circuit board layer and for providing power or ground to the electrical components. The tab which extends outward from the edge of the second embodiment of the printed circuit board can be coupled to a mechanical fixture and/or an electrical fixture to provide a path for the flow of heat from the printed circuit board to externally coupled mechanical fixtures and/or to provide electrical power to the

electrically conducting layer of the printed circuit board. Still other objects will become apparent to those of ordinary skill in the art upon reading and understanding the following detailed description.

SUMMARY OF THE INVENTION

[0008] The present invention is a circuit board that includes a conductive sheet sandwiched between an insulating top layer and an insulating bottom layer. The top and bottom layers and the conductive sheet define a circuit board layer having an edge that includes an edge of the conductive sheet. An insulating edge layer covers substantially all of the edges of the conductive sheet.

[0009] The conductive sheet can include at least one via therethrough. The insulating layers can be formed from a common dielectric material deposited on the conductive sheet in a manner known in the art, such as conformal coating. At least one of the top and bottom layers can have a circuit pattern formed thereon.

[0010] The insulating edge layer can include at least one opening where a part of the edge of the conductive sheet is exposed in response to separating the circuit board layer from a panel. In one embodiment, the exposed part of the edge can be within a perimeter of the circuit board layer. Moreover, the exposed part of the edge can be on a tab attached to the circuit board layer where the tab extends into a recess in the circuit board layer.

[0011] The top and bottom insulating layers and the conductive sheet define a panel that includes the circuit board layer coupled to a disposable part of the panel by the tab. The insulating edge layer covers the edges of the tab and the circuit board layer prior to singulation of the circuit board layer from the disposable part of the panel. The tab is responsive to a breaking force applied thereto for breaking whereupon the circuit board layer separates from the disposable part of the panel with at least part of the tab remaining attached to the circuit board layer.

[0012] In another embodiment, the conductive sheet includes a tab that extends outward from between the top layer and the bottom layer. At least part of the edge of the tab is exposed when the circuit board layer is separated from the disposable part of the panel. The at least part of the edge is outside a perimeter of the circuit board layer. The tab in this embodiment has a top surface and a bottom surface. At least part of one of the top surface and the bottom surface of the tab can be exposed, i.e., not covered by insulating material.

[0013] A plurality of circuit board layers can be laminated together to form a multi-layer circuit board. The tab of one circuit board layer of the multi-layer circuit board can be offset from the tab of another circuit board layer of the multi-layer circuit board. An electronic component can be connected between the tab of one circuit board layer and the tab of the other circuit board layer. The conductive sheet of one circuit board layer can define the ground plane of the multi-layer circuit board and the conductive sheet of another circuit board layer can define a power plane of the multi-layer circuit board.

[0014] The invention is also a method of forming a circuit board that includes providing a first conductive sheet and selectively removing one or more portions of the first conductive sheet to form a first panel having a first circuit board that is coupled to a disposable part of the first panel by at least one tab that extends from an edge of the first circuit board to an edge of the disposable part of the first panel. An insulating coating is applied to the first circuit board so at least each edge of the first circuit board is covered thereby. The first circuit board is separated from the disposable part in a manner whereupon at least part of the tab remains attached to the first circuit board and this part of the tab includes an exposed edge of the conductive sheet of the first circuit board.

[0015] The insulating coating can be applied to the first circuit board in a manner whereupon at least each edge of the at least one tab is covered thereby. The at least part of the tab can terminate one of inside and outside a perimeter of the first circuit board.

[0016] The method can also include providing a second conductive sheet and selectively removing one or more portions of the second conductive sheet to form a second panel having a second circuit board that is coupled to a disposable part of the second panel by at least one tab that extends from an edge of the second circuit board to an edge of the disposable part of the second panel. An insulating coating is applied to the second circuit board so that at least each edge of the second circuit board is covered thereby. The first and second circuit boards are then laminated together and the second circuit board is separated from the disposable part of the second panel in a manner whereupon at least part of the tab remains attached to the second circuit board and the at least part of the tab includes an exposed edge of the conductive sheet of the second circuit board.

[0017] The at least part of each tab can terminate inside or outside a perimeter of the corresponding circuit board. When the first and second circuit boards are laminated together, the at least one tab of the first circuit board is offset from the at least one tab of the second

circuit board. An electrical component can be electrically connected between the at least one tab of the first circuit board and the at least one tab of the second circuit board.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Fig. 1 is a cutaway perspective view of a printed circuit board layer having a perforate conductive plane surrounded by an insulating material in accordance with the present invention;

[0019] Fig. 2 is a cutaway perspective view of a portion of a printed circuit board layer of the type shown in Fig. 1 including a circuit pattern formed on the outward facing surfaces thereof;

[0020] Figs. 3 and 4 are plan views of panels having different circuit board layers formed therefrom in accordance with one embodiment of the present invention;

[0021] Fig. 5 is a plan view of the panels shown in Figs. 3 and 4 laminated together with the circuit board layers thereof in registry;

[0022] Fig. 6 is an isolated plan view of a tab which the panels in Figs. 3 and 4 utilize to connect their circuit board layers to disposable parts of the panels;

[0023] Fig. 7 is an isolated plan view of the tab shown in Fig. 6 after breaking in response to the application of a breaking force applied thereto;

[0024] Fig. 8 is a view taken along lines VIII-VIII in Fig. 7;

[0025] Figs. 9 and 10 are plan views of panels including printed circuit board layers in accordance with another embodiment of the present invention;

[0026] Fig. 11 is a plan view of the panels shown in Figs. 9 and 10 laminated together with the circuit board layers thereof in registry;

[0027] Fig. 12 is a plan view of the laminated printed circuit board layers shown in Fig. 11 singulated from the disposable parts of their respective panels;

[0028] Fig. 13 is a section taken along XIII-XIII in Fig. 12; and

[0029] Fig. 14 is a plan view of the singulated laminated circuit board layers shown in Fig. 12 with certain tabs thereof coupled to a mounting fixture and with certain tabs thereof coupled to an electrical fixture.

DETAILED DESCRIPTION OF THE INVENTION

[0030] With reference to Fig. 1, a printed circuit board layer 2 includes an electrically conductive sheet or foil 4. Sheet 4 can be formed from a copper foil, an iron-nickel alloy, or combinations thereof. Sheet 4 can be a perforate sheet as shown in Fig. 1 or can be a solid sheet. It is desirable for sheet 4 to have a coefficient of thermal expansion comparable to that of silicon materials from which integrated circuits are typically prepared in order to prevent failure of adhesion joints utilized to adhere the integrated circuit or a packaged integrated circuit (not shown) to printed circuit board layer 2. Describing sheet 4 as perforate means that sheet 4 is a mesh sheet having a plurality of through-holes or vias 6 spaced at regular intervals.

[0031] An electrically insulative coating 8 is formed around sheet 4. This coating 8 can be formed around sheet 4 in any manner known in the art, such as conformal coating. More specifically, coating 8 forms an insulating top layer 10 which covers a top surface 12 of sheet 4, an insulating bottom layer 14 which covers a bottom surface 16 of sheet 4 and an insulating edge layer 18 which covers an edge 20 of sheet 4. When sheet 4 is coated with coating 8, an interior surface of each through-hole or via 6 is also coated with coating 8. Thus, no portion of sheet 4 is left uncovered by coating 8.

[0032] With reference to Fig. 2, and with continuing reference to Fig. 1, printed circuit board layer 2 formed in the above-described manner can have a conductive pattern formed on the outward facing surface of top layer 10 and/or the outward facing surface of bottom layer 14 by conventional processes. Specifically, utilizing one or more photolithographic techniques and one or more metallization techniques, the conductive pattern can be formed on the outward facing surface of top layer 10 and/or the outward facing surface of bottom layer 14. This conductive pattern can include un-plated through-holes or vias 6-1, plated, blind through-holes or vias 6-2, and/or plated through-holes or vias 6-3. Additional details regarding formation of printed circuit board layer 2 and for forming a conductive pattern, including one or more of the various types of through-holes or vias 6, on top layer 10 and/or bottom layer 14 can be found in U.S. Patent Application Serial No. 10/184,387, filed June 27, 2002, entitled "Process For Creating Vias For Circuit Assemblies" which is assigned to the same Assignee as the present application and which is incorporated herein by reference.

[0033] The preparation of one or more printed circuit board layers 2 in a panel form and the assembly of plural printed circuit board layers to form a multi-layer printed circuit board assembly will now be described.

[0034] With reference to Fig. 3, in accordance with a first embodiment of the invention, one or more first printed circuit board (PCB) layers 30 are fabricated as part of a panel 32. Each first PCB layer 30 is surrounded by a disposable part 34 of panel 32. In accordance with the present invention, each first PCB layer 30 is coupled to disposable part 34 of panel 32 by one or more tabs 36.

[0035] The general steps to prepare panel 32 to the form shown in Fig. 3 will now be described. Initially, a first conductive sheet, like conductive sheet 4, of the size of panel 32 is provided. This sheet can either be a solid sheet or a perforate sheet depending on the application. Next, cut lines or slots 38 are formed in the conductive sheet by pattern etching or a machine cutting or routing process to define the perimeter of each first PCB layer 30 of panel 32. These slots 38 are interrupted by tabs 36 which hold each first PCB layer 30 to disposable part 34 during processing.

[0036] Next, an electrically insulative coating, like coating 8, is deposited on the conductive sheet forming panel 32 in a manner whereupon the top surface, the bottom surface, and the edges of the electrically conductive sheet associated with each first PCB layer 30 that were exposed during the formation of slots 38 are covered thereby. If the conductive sheet is perforate, the electrically insulative coating also covers the interior surface of each through-hole or via. In addition, the top and bottom surfaces and the edges of each tab 36 defined during the formation of slots 38 can also be covered by the electrically insulative coating. The top and bottom surfaces and the edges of disposable part 34 defined during formation of slots 38 can also be covered with the electrically insulative coating. However, this is not required. Typically, however, all of the edges, surfaces and, if vias are provided, the interior surface of each via of the conductive sheet of panel 32 are covered by the electrically insulative coating.

[0037] Next, photolithographic processing techniques and metallization techniques known in the art and described in the above-identified United States patent application incorporated herein by reference are utilized to define a circuit pattern 40 on one or both of the exposed surfaces of the electrically insulative coating deposited on the portion of the electrically conductive sheet associated with each first PCB layer 30.

[0038] If each first PCB layer 30 is ready for use after circuit pattern 40 is formed thereon, each first PCB layer 30 can be singulated from panel 32 by applying a breaking force to the tabs connecting each first PCB layer 30 to disposable part 34. However, if desired, one or more additional layers of electrically insulative coating (not shown) and circuit patterns (not shown) can be formed over circuit pattern 40, with the various layers of circuit patterns interconnected in a desired manner utilizing conventional processes. Thereafter, each first PCB layer 30 can be singulated from panel 32 by applying a breaking force to each tab connecting each first PCB layer 30 to disposable part 34.

[0039] Alternatively, each first PCB layer 30 of panel 32 can be laminated to a second PCB layer 42 of a panel 44 shown in Fig. 4. Panel 44 includes one or more second PCB layers 42 connected to a disposable part 46 of panel 44 by tabs 48 defined during formation of slots 50 in the electrically conductive sheet of panel 44 in the same manner described above in connection with the formation of slots 38 in panel 32.

[0040] An electrically insulative coating is deposited on the conductive sheet forming panel 44 in a manner whereupon the top surface, the bottom surface and the edges of electrically conductive sheet associated with each second PCB layer 42 that were exposed during the formation of slots 50 are covered thereby. If the conductive sheet is perforate, the electrically insulative coating also covers the interior surface of each through-hole or via. In addition, the top and bottom surfaces and the edges of each tab 48 defined during the formation of slots 50 can also be covered by the electrically insulative coating. The top and bottom surfaces and the edges of disposable part 46 defined during formation of slots 50 can also be covered with the electrically insulative coating. However, this is not required. Typically, however, all of the edges, surfaces and, if vias are provided, the interior surface of each via of the conductive sheet of panel 44 are covered by the electrically insulative coating.

[0041] Each second PCB layer 42 has a circuit pattern 52 formed on one or both of the exposed surfaces of the electrically insulative coating deposited on the portion of the electrically conductive sheet associated with each second PCB layer 42. If desired, each second PCB layer 42 can include one or more additional layers of electrically insulative coating and circuit patterns formed over circuit pattern 52, with the various layers of circuit patterns interconnected in the desired manner utilizing conventional processes.

[0042] With reference to Fig. 5, and with ongoing reference to Figs. 3 and 4, panels 32 and 44 can be laminated together in a manner known in the art, with each first PCB layer

30 positioned in registry with a corresponding second PCB layer 42 to form a multi-layer PCB assembly 60. Appropriate techniques known in the art can be utilized to form one or more electrical connections between each circuit pattern 40 and the corresponding circuit pattern 52. For simplicity of description, the formation of these one or more electrical connections between circuit pattern 40 and corresponding circuit pattern 52 will not be described herein.

[0043] As shown best in Fig. 5, tabs 36 of panel 32 do not overlay tabs 48 of panel 44 when panels 32 and 44 are laminated together. In this manner, the PCB layers 30 and 42 forming each multi-layer PCB assembly 60 can be singulated from their disposable parts 34 and 46, respectively, independent of each other. If desired, however, one or more tabs 36 and 48 can be in alignment with each other when panels 32 and 44 are laminated.

[0044] With reference to Figs. 6 and 7, and with continuing reference to Figs. 3-5, each tab 36 and 48 will now be described with respect to an exemplary tab 36 of panel 32. However, it is to be appreciated that each tab 48 of panel 44 is similar to each tab 36 of panel 32 and, therefore, the following description of exemplary tab 36 is applicable to each tab 48.

[0045] As shown in Fig. 6, exemplary tab 36 extends between first PCB layer 30 and disposable part 34. To facilitate breaking, exemplary tab 36 includes a narrowing 62, also known as a Charpy notch, along its length. This narrowing 62 enables exemplary tab 36 to break at a well-defined position whereupon exemplary tab 36 separates into a first part 64 that remains attached to first PCB layer 30 and a second part 66 that remains attached to disposable part 34.

[0046] The ends of slots 38 on opposite sides of exemplary tab 36 define a recess 68 within a perimeter 70 of first PCB layer 30. For purpose of the present description, perimeter 70 of first PCB layer 30 includes the outer edge 72 of first PCB layer 30 and the imaginary extension 74 of outer edges 72 across each recess 68. As shown, the narrowing 62 of each tab 36 is within perimeter 70 of first PCB layer 30. Hence, when exemplary tab 36 separates into first part 64 and second part 66, a distal end 76 of each first part 64 terminates within recess 68.

[0047] With reference to Fig. 8, and with continuing reference to all previous Figs., since first PCB layer 30 and exemplary tab 36 include an electrically conductive sheet 78, like sheet 4 in Fig. 1, coated with an electrically insulative coating 80, like coating 8 in Fig. 1, breaking exemplary tab 36 exposes a small portion 82 of the edge of electrically conductive

sheet 78 and the surrounding electrically insulative coating 80. Since only the distal end 76 of first part 64 of exemplary tab 36 includes small portion 82 of electrically conductive sheet 78 exposed, substantially all of the edge of electrically conductive sheet 78 is covered by electrically insulative coating 80 and, more particularly, the insulating edge layer of electrically insulative coating 80. Accordingly, inadvertent electrical contact with the edge of electrically conductive sheet 78 covered with the insulating edge layer of electrically insulative coating 80 is avoided.

[0048] The electrically conductive sheet of first PCB layer 30 and second PCB layer 42 can be utilized to conduct heat away from electrical components disposed on one or both surfaces thereof. In addition, the electrically conductive sheets of PCB layers 30 and 42 of each multi-layer PCB assembly 60 can be utilized to provide power and ground to electrical components disposed on the outward facing surfaces of multi-layer PCB assembly 60. This is accomplished by connecting the power lead of each integrated circuit disposed on multi-layer PCB assembly 60 to the conductive sheet of one PCB layer 30 and 42 and connecting the ground lead of each integrated circuit to the conductive sheet of the other PCB layer 30 and 42. The conductive sheet of each PCB layer 30 and 42 can then be connected to an appropriate one of a power terminal and a ground terminal of an external power supply via the small portion 82 of the edge of the electrically conductive sheet exposed on the first part 64 of one or more tabs 36 by suitable fixture means.

[0049] With reference to Fig. 9, in accordance with a second embodiment of the invention, a first PCB layer 90 is fabricated in the same manner as first PCB layer 30 discussed above in connection with Fig. 3. In this second embodiment, however, one or more tabs 92 extend outward from a perimeter 94 of first PCB layer 90 and connect it to a disposable part 96 of a panel 98 that also includes first PCB layer 90 and tab 92. In a manner similar to PCB layers 30 and 42 and tabs 36 and 48, respectively, first PCB layer 90 and tabs 92 can be formed from an electrically conductive sheet having its top and bottom surfaces and edges coated with an electrically insulative coating. However, in this second embodiment, the electrically insulative coating can be omitted from one or more tabs 92 or can be removed from one or more tabs 92 after deposit. One or more of tabs 92 can each include a mounting hole 100 that can be utilized to couple tab 92 to mounting hardware or external electrical circuitry, such as a power supply.

[0050] A circuit pattern 101 can be formed on one or both exposed surfaces of first PCB layer 90 utilizing photolithographic processing techniques and metallization techniques known in the art. Once first PCB layer 90 has circuit pattern 101 formed on one or both exposed surfaces thereof, first PCB layer 90 and each tab 92 can be singulated from panel 98, especially disposable part 96, and utilized as is. If desired, however, one or more additional layers of electrically insulative coating and circuit patterns can be formed over circuit pattern 101, with the various layers of circuit patterns interconnected in a desired manner utilizing conventional processes. Thereafter, first PCB layer 90 and each tab 92 can be singulated from panel 98.

[0051] With reference to Figs. 10 and 11, if desired, panel 98 can be laminated to a panel 106 in a manner known in the art with first PCB layer 90 in registry with a second PCB layer 102 of panel 106 to form a multi-layer PCB assembly 104, shown best in Figs. 11-13. Second PCB layer 102 is part of panel 106 that includes tabs 108 and disposable part 110. One or more tabs 108 can each include a mounting hole 112 that can be utilized to couple tab 108 to appropriate mechanical hardware or electrical circuitry. In a manner similar to PCB layers 30 and 42 and tabs 36 and 48, respectively, second PCB layer 102 and tabs 108 can be formed from an electrically conductive sheet coated with an electrically insulative coating. However, in this second embodiment, the electrically insulative coating can be omitted from each tab 108 or can be removed from each tab 108 after deposit.

[0052] A circuit pattern 114 can be formed on one or both surfaces of second PCB layer 102 utilizing photolithographic processing techniques and metalization techniques known in the art. Once first PCB layer 90 and second PCB layer 102 are laminated in registry, appropriate techniques known in the art can be utilized to form one or more electrical connections between circuit pattern 101 and the circuit pattern 114.

[0053] With reference to Fig. 12, and with continuing reference to Fig. 11, next, a breaking force can be applied to each tab 92 and 108 to singulate first and second PCB layers 90 and 102 and, hence, multi-layer PCB assembly 104, from disposable parts 96 and 110. To facilitate the application of a breaking force to each tab 92 and 108, tabs 92 and 108 can be positioned on first and second PCB layers 90 and 102 so that they do not overlay each other. As shown, all of each tab 92 and all of each tab 108 remains with first and second PCB layers 90 and 102, respectively. To this end, a breaking force applied to each tab 92 and each tab 108 causes it to break from disposable part 96 and 110, respectively. To enable each tab 92

and 108 to break cleanly from disposable parts 96 and 110, a break or score line can be formed at the boundary of each tab 92 and 108 and each disposable part 96 and 110 to weaken the mechanical connection therebetween. A suitable breaking force can be applied to each tab 92 and 108 by a mechanical press having a ram with a suitably shaped tip for causing the breaking force to be applied to the tab, especially the score line.

[0054] With reference to Fig. 13, and with continuing reference to Figs. 11 and 12, at a suitable time one or more electrical components 120, such as a packaged integrated circuit, an unpackaged flip-chip integrated circuit, a resistor, a capacitor and/or an inductor can be coupled to appropriate points of circuit pattern 101 and/or circuit pattern 114 of multi-layer PCB assembly 104 in a manner known in the art. Moreover, as shown in Fig. 14, one or more tabs 92 and/or 108 can be coupled to a mounting fixture 122 or an electrical fixture, such as a power supply 124. Since each tab 92 is part of an electrically conductive sheet 130 associated with first PCB layer 90, and since each tab 108 is part of an electrically conductive sheet 132 associated with second PCB layer 102, connecting one or more tabs 92 to one terminal of power supply 124 and connecting one or more tabs 108 to the other terminal of power supply 124 biases electrically conductive sheets 130 and 132 accordingly. The provisioning of electrical power to electrically conductive sheets 130 and 132 in this manner simplifies the provisioning of electrical power to each electrical component, e.g., electrical component 120, coupled to one or both outward facing surfaces of multi-layer PCB assembly 104.

[0055] In addition, other electrical components, such as one or more capacitors 134, can be connected between adjacent pairs of tabs 92 and 108. The inclusion of one or more capacitors 134 between adjacent pairs of tabs 92 and 108 reduces the need to install filter capacitors on one or both of the outward facing surfaces of multi-layer PCB assembly 104 to provide electrical filtering for electrical components disposed thereon.

[0056] Like the distal end of exemplary tab 36, the distal end 136 of each tab 92 and the distal end 137 of each tab 108 includes an exposed edge of electrically conductive sheet 130 and 132, respectively. In addition, all or part of the top surface and/or bottom surface of the electrically conductive sheets 130 and 132 associated with adjacent pairs of tabs 92 and 108, respectively, can be exposed in order to facilitate the connection of electronic components, such as capacitors 134, therebetween.

[0057] As can be seen, the present invention provides a printed circuit board having one or more printed circuit board layers each of which has a conductive plane that extends to the edge of the printed circuit board but which is substantially, but not completely, covered by an insulating material. The edge of the conductive layer not covered by the insulating material is positioned on the edge of a tab which is utilized to couple the board to a disposable part of a larger panel that the printed circuit board is formed from during fabrication. The exposed edge of the conductive layer becomes exposed upon breaking the tab and singulating the printed circuit board from the disposable part of the panel.

[0058] The conductive layer of each circuit board layer can serve the dual purpose of conducting heat away from electrical components disposed on one or both surfaces of the printed circuit board or printed circuit board layer and providing power or ground to the electrical components.

[0059] The present invention has been described with reference to the preferred embodiments. Obvious modifications and alterations will occur to others upon reading and understanding the preceding detailed description. For example, multi-layer PCB assembly 60 was described as being formed by laminating together PCB layers 30 and 42. However, a multi-layer PCB assembly can be formed from three or more PCB layers laminated together and electrically connected in a desired manner. Moreover, an electrical component, e.g., capacitor 134, was described as being connected to tabs 92 and 108 of adjacent PCB layers 90 and 102 of multi-layer PCB assembly 104. However, an electrical component can be connected between tabs of adjacent or non-adjacent PCB layers of a multi-layer PCB assembly having three or more PCB layers. It is intended that the invention be construed as including all such modifications and alterations insofar as they come within the scope of the appended claims or the equivalents thereof.

THE INVENTION IS CLAIMED TO BE:

1. A process for exposing predetermined areas of a substrate comprising the following steps:

(a) applying a curable coating composition to a substrate, some or all of which is electrically conductive, to form an uncured coating thereon;

(b) applying a resist over said uncured coating;

(c) imaging said resist in predetermined locations;

(d) developing said resist to expose predetermined areas of the uncured coating;

(e) removing the exposed areas of the uncured coating; and

(f) heating the coated substrate of step (e) to a temperature and for a time sufficient to cure the coating.

2. The process of claim 1 wherein the exposed areas of the uncured coating are removed in step (e) to form one or more vias.

3. The process of claim 1 wherein upon completion of step (a) the coated substrate is heated to a temperature and for a time sufficient to remove any solvent and/or water from said uncured coating, but insufficient to cure the coating.

4. The process of claim 1 wherein the substrate is metal.

5. The process of claim 4 wherein the metal substrate is a perforate metal core.

6. The process of claim 5 wherein the metal core is selected from perforate copper foil, nickel-iron alloys, and combinations thereof.

7. The process of claim 6 wherein the metal core is a nickel-iron alloy.

8. The process of claim 6 wherein before the application of the curable coating composition in step (a), a layer of copper metal is applied to the metal core.

9. The process of claim 1 wherein the substrate is a printed circuit board.

10. The process of claim 1, further comprising the following step:

(g) stripping the remaining resist.

11. The process of claim 10 wherein step (f) is performed prior to step (g).

12. The process of claim 10 wherein step (g) is performed prior to step (f).

13. The process of claim 10, further comprising the following subsequent steps:

(h) applying a layer of metal to all surfaces;

(i) applying a second resist to the layer of metal applied in step (h);

(j) processing said second resist to form a predetermined pattern of exposed underlying metal;

(k) etching said exposed metal; and

(l) stripping the remaining second resist to form an electrical circuit pattern.

14. The process of claim 13 wherein the layer of metal applied in step (h) comprises copper.

15. The process of claim 13 wherein upon completion of step (1), steps (a) through (l) of said process are repeated one or more times to form multiple layers of interconnecting electrical circuit patterns.

16. The process of claim 10 wherein step (f) is performed prior to step (g).

17. The process of claim 10 wherein step (g) is performed prior to step (f).

18. The process of claim 1 wherein the curable coating composition is applied by electrodeposition.

19. The process of claim 1 wherein the curable coating composition is applied by screen printing.

20. The process of claim 1 wherein the curable coating composition is applied by curtain coating.

21. The process of claim 1 wherein the curable coating composition is applied by roll coating.

22. The process of claim 1 wherein the curable coating composition is applied by immersion coating techniques.

23. The process of claim 1 wherein the curable coating composition is spray-applied.

24. The process of claim 1 wherein the curable coating composition is applied by spin coating.

25. The process of claim 1 wherein said curable coating composition comprises:

- (a) one or more active hydrogen-containing resins; and
- (b) one or more curing reagents reactive with the active hydrogens of (a).

26. The process of claim 25 wherein said active hydrogen-containing resin comprises at least one polymer selected from a polyepoxide polymer, an acrylic polymer, a polyester polymer, a urethane polymer, a silicon based polymer, a polyether polymer, a polyurea polymer, a vinyl polymer, a polyamide polymer, a polyimide polymer, mixtures thereof and copolymers thereof.

27. The process of claim 25 wherein said curing agent (b) is selected from blocked polyisocyanates, carbodiimides, aziridines, epoxies, aminoplasts, active esters, and mixtures thereof.

28. The process of claim 1 wherein steps (d) and (e) occur simultaneously.

29. The process of claim 1 wherein the resist is removed in step (d) by applying an acidic solution, and the curable coating is removed in step (e) by applying a basic solution.

30. The process of claim 1 wherein the resist is removed in step (d) by applying a basic solution, and the curable coating is removed in step (e) by applying an acidic solution.

31. The process of claim 1 wherein the curable coating is removed in step (e) by applying an organic solvent.

32. The process of claim 1 wherein the cured coating composition comprises a dielectric material.

33. A process for fabricating a multi-layer electrical circuit assembly comprising the following steps:

- (a) applying a curable coating composition to a substrate, some or all of which is electrically conductive, to form an uncured coating thereon;

- (b) applying a resist over said uncured coating;

- (c) imaging said resist in predetermined locations;

- (d) developing said resist to expose predetermined areas of the uncured coating;

- (e) removing the exposed areas of the uncured coating to form a via;

- (f) heating the coated substrate of step (e) to a temperature and for a time sufficient to cure the coating;

- (g) stripping the remaining resist;

- (h) applying a layer of metal to all surfaces;

- (i) applying a second resist to the layer of metal applied in step (h);

- (j) processing said second resist to form a predetermined pattern of exposed underlying metal;

- (k) etching said exposed metal;

- (l) stripping the remaining second resist; and

- (m) optionally repeating steps (a) through (l) one or more times to form multiple layers of interconnecting electrical circuit patterns.

34. The process of claim 33 wherein the exposed areas of the uncured coating are removed in step (e) to form one or more vias.

35. The process of claim 33 wherein upon completion of step

(a) the coated substrate is heated to a temperature and for a time sufficient to remove any solvent and/or water from said uncured coating, but insufficient to cure the coating.

36. The process of claim 33 wherein the substrate is metal.

37. The process of claim 36 wherein the metal substrate is a perforate metal core.

38. The process of claim 37 wherein the metal core is selected from perforate copper foil, nickel-iron alloys, and combinations thereof.

39. The process of claim 38 wherein the metal core is a nickel-iron alloy.

40. The process of claim 37 wherein before the application of the curable coating composition in step (a), a layer of copper metal is applied to the metal core.

41. The process of claim 33 wherein the substrate is a printed circuit board.

42. The process of claim 33 wherein the curable coating composition is applied by electrodeposition.

43. The process of claim 33 wherein the curable coating composition is applied by screen printing.

44. The process of claim 33 wherein the curable coating composition is applied by curtain coating.

45. The process of claim 33 wherein the curable coating composition is applied by roll coating.

46. The process of claim 33 wherein the curable coating composition is applied by immersion coating techniques.

47. The process of claim 33 wherein the curable coating composition is spray-applied.

48. The process of claim 33 wherein the curable coating composition is applied by spin coating.

49. The process of claim 33 wherein said curable coating composition comprises:

- (a) one or more active hydrogen-containing resins; and
- (b) one or more curing reagents reactive with the active hydrogens of (a).

50. The process of claim 49 wherein said active hydrogen-containing resin comprises at least one polymer selected from a polyepoxide polymer, an acrylic polymer, a polyester polymer, a urethane polymer, a silicon based polymer, a polyether polymer, a polyurea polymer, a polyurea polymer, a vinyl polymer, a polyamide polymer, a polyimide polymer, mixtures thereof and copolymers thereof.

51. The process of claim 49 wherein said curing agent (b) is selected from blocked polyisocyanates, carbodiimides, aziridines, epoxies, aminoplasts, active esters, and mixtures thereof.

52. The process of claim 33 wherein steps (d) and (e) occur simultaneously.

53. The process of claim 33 wherein the resist is removed in step (d) by applying an acidic solution, and the curable coating is removed in step (e) by applying a basic solution.

54. The process of claim 33 wherein the resist is removed in step (d) by applying a basic solution, and the curable coating is removed in step (e) by applying an acidic solution.

55. The process of claim 33 wherein the curable coating is removed in step (e) by applying an organic solvent.

56. The process of claim 33 wherein the cured coating composition comprises a dielectric material.

57. The process of claim 33 wherein the layer of metal applied in step (h) comprises copper.

58. A coated substrate formed by the process of claim 1.

59. A circuit assembly formed by the process of claim 31.