

SOLAR CELL HAVING AN EMITTER REGION WITH WIDE BANDGAP SEMICONDUCTOR MATERIAL

TECHNICAL FIELD

[0001] Embodiments of the present invention are in the field of renewable energy and, in particular, solar cells having emitter regions composed of wide bandgap semiconductor material.

BACKGROUND

[0002] Photovoltaic cells, commonly known as solar cells, are well known devices for direct conversion of solar radiation into electrical energy. Generally, solar cells are fabricated on a semiconductor wafer or substrate using semiconductor processing techniques to form a p-n junction near a surface of the substrate. Solar radiation impinging on the surface of, and entering into, the substrate creates electron and hole pairs in the bulk of the substrate. The electron and hole pairs migrate to p-doped and n-doped regions in the substrate, thereby generating a voltage differential between the doped regions. The doped regions are connected to conductive regions on the solar cell to direct an electrical current from the cell to an external circuit coupled thereto.

[0003] Efficiency is an important characteristic of a solar cell as it is directly related to the capability of the solar cell to generate power. Likewise, efficiency in producing solar cells is directly related to the cost effectiveness of such solar cells. Accordingly, techniques for increasing the efficiency of solar cells, or techniques for increasing the efficiency in the manufacture of solar cells, are generally desirable. Some embodiments of the present invention allow for increased solar cell manufacture efficiency by providing novel processes for fabricating solar cell structures. Some embodiments of the present invention allow for increased solar cell efficiency by providing novel solar cell structures.

SUMMARY OF INVENTION

[0003a] According to a first aspect of the present invention, there is provided a method of fabricating a solar cell, the method comprising:

forming, in a process tool having a controlled atmosphere, a thin dielectric layer of aluminum oxide (Al_2O_3) on a surface of a single crystalline N-type silicon semiconductor substrate of the solar cell, the semiconductor substrate having a bandgap; and, without removing the semiconductor substrate from the controlled atmosphere of the process tool,

forming a semiconductor layer on the thin dielectric layer, the semiconductor layer being transparent in the visible spectrum and having a bandgap at least approximately 0.2 electron Volts (eV) above the bandgap of the semiconductor substrate and a bandgap of greater than 3 eV and comprising a material selected from the group consisting of: aluminum nitride (AlN), aluminum gallium nitride ($\text{Al}_x\text{Ga}_{1-x}\text{N}$, where $0 < x < 1$), and boron nitride (BN).

[0003b] According to a second aspect of the present invention, there is provided a method of fabricating a solar cell, the method comprising:

forming a first emitter region on a surface of a N-type silicon semiconductor substrate of the solar cell, the first emitter region comprising a semiconductor material doped to a first conductivity type and formed on a first thin dielectric layer; and

forming a second emitter region on the surface of the semiconductor substrate, the forming comprising:

forming, in a process tool having a controlled atmosphere, a thin dielectric layer of aluminum oxide (Al_2O_3) on a surface of a single crystalline N-type silicon semiconductor substrate of the solar cell, the semiconductor substrate having a bandgap; and, without removing the semiconductor substrate from the controlled atmosphere of the process tool,

forming a semiconductor layer on the thin dielectric layer, the semiconductor layer being transparent in the visible spectrum and having a bandgap at least approximately 0.2 electron Volts (eV) above the bandgap of the semiconductor substrate and a bandgap of greater than 3 eV and comprising a material selected from the group consisting of: aluminum nitride (AlN), aluminum gallium nitride ($\text{Al}_x\text{Ga}_{1-x}\text{N}$, where $0 < x < 1$), and boron nitride (BN); and

doping the semiconductor layer with charge carrier dopant impurity ions of a second, opposite conductivity type.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figure 1 illustrates a band diagram as a function of increasing energy (E) for a conventional heterojunction contact without an interfacial tunnel oxide.

[0005] Figure 2 illustrates a band diagram as a function of increasing energy (E) for a heterojunction contact with an interfacial tunnel oxide, in accordance with an embodiment of the present invention.

[0006] Figure 3 is a flowchart representing operations in a method of fabricating a solar cell, in accordance with an embodiment of the present invention.

[0007] Figure 4A illustrates a cross-sectional view of an operation in the fabrication of a solar cell wherein a foundational structure for fabricating a solar cell is provided and includes a silicon substrate, a thin dielectric layer, and a deposited silicon layer, in accordance with another embodiment of the present invention.

[0008] Figure 4B illustrates a cross-sectional view of an operation in the fabrication of a solar cell wherein a layer of doping material is deposited over the deposited silicon layer of Figure 4A, in accordance with another embodiment of the present invention.

[0009] Figure 4C illustrates a cross-sectional view of an operation in the fabrication of a solar cell wherein a first oxide layer 410 is deposited over the layer of doping material of Figure 4B, in accordance with another embodiment of the present invention.

[0010] Figure 4D illustrates a cross-sectional view of an operation in the fabrication of a solar cell wherein a material removal process is performed on the structure of Figure 4C to form an exposed polysilicon region, in accordance with another embodiment of the present invention.

[0011] Figure 4E illustrates a cross-sectional view of an operation in the fabrication of a solar cell wherein an etching process is performed on the structure of Figure 4D to facilitate etching the exposed polysilicon regions and to form a first texturized silicon region on the back side of the solar cell, in accordance with another embodiment of the present invention.

[0012] Figure 4F illustrates a cross-sectional view of an operation in the fabrication of a solar cell wherein an oxide layer is formed over the layer of doping material and first texturized silicon region of Figure 4E, in accordance with another embodiment of the present invention.

[0013] Figure 4G illustrates a cross-sectional view of an operation in the fabrication of a solar cell wherein a doped polysilicon layer is formed from the structure of Figure 4F, in accordance with another embodiment of the present invention.

[0014] Figure 4H illustrates a cross-sectional view of an operation in the fabrication of a solar cell wherein a wide band gap doped semiconductor layer is formed on the structure of Figure 4G, in accordance with another embodiment of the present invention.

[0015] Figure 4I illustrates a cross-sectional view of an operation in the fabrication of a solar cell wherein a wide band gap doped semiconductor is deposited over the texturized silicon region of Figure 4H, in accordance with another embodiment of the present invention.

[0016] Figure 4J illustrates a cross-sectional view of an operation in the fabrication of a solar cell wherein partial removal of the wide band gap doped semiconductor of Figure 4H is performed, in accordance with another embodiment of the present invention.

[0017] Figure 4K illustrates a cross-sectional view of an operation in the fabrication of a solar cell wherein a first metal grid or gridline is formed on the back side of the structure of Figure 4J, in accordance with another embodiment of the present invention.

[0018] Figure 4L illustrates a cross-sectional view of an operation in the fabrication of a solar cell wherein a second metal grid or gridline is formed on the back side of the structure of Figure 4K, in accordance with another embodiment of the present invention.

DETAILED DESCRIPTION

[0019] Solar cells having emitter regions composed of wide bandgap semiconductor material are described herein. In the following description, numerous specific details are set forth, such as specific process flow operations and material regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known fabrication techniques, such as subsequent metal contact formation techniques, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the figures are illustrative representations and are not necessarily drawn to scale.

[0020] Disclosed herein are methods of fabricating solar cells. In one embodiment, a method includes forming, in a process tool having a controlled atmosphere, a thin dielectric layer on a surface of a semiconductor substrate of the solar cell. The semiconductor substrate has a bandgap. Without removing the semiconductor substrate from the controlled atmosphere of the process tool, a semiconductor layer is formed on the thin dielectric layer. The semiconductor layer has a bandgap at least approximately 0.2 electron Volts (eV) above the bandgap of the semiconductor substrate.

[0021] Also disclosed herein are solar cells having emitter regions composed of wide bandgap semiconductor material. In one embodiment, a solar cell includes a silicon substrate. A first emitter region is disposed on a surface of the silicon substrate and is composed of an aluminum nitride (AlN) layer doped to a first conductivity type. The AlN layer is disposed on a thin aluminum oxide (Al₂O₃) layer. A second emitter region is disposed on the surface of the silicon substrate and is composed of a semiconductor material doped to a second, opposite, conductivity type. The second semiconductor material is disposed on a thin dielectric layer. First and second contacts are disposed on, and conductively coupled to, the first and second emitter regions, respectively.

[0022] Passivation of solar cells surfaces is typically accomplished with diffusion and oxidation to form a thin dielectric material on one or more surfaces of the solar cell. Forming such a thin dielectric material may provide a structural approach to repelling minority carriers at a surface of the solar cell. Furthermore, the oxidation process may be designed to effectively tie-up interface defects that may exist at the outer most surfaces of the solar cell. The formed dielectric material may have several functions such as, but not limited to, use as a moisture barrier, use as a hydrogen source and, possibly, use as an anti-reflection coating.

[0023] The above three aspects of solar cell surface passivation are typically achieved in two or more process operation during the fabrication of the solar cell. However, using multiple process operations may invoke a new set of issues, namely, handling complexity and increased processing cost. Also, typically, is an oxide and diffusion operation are performed in one tool (e.g., in a diffusion furnace), then the dielectric formation is generally performed in a separate process tool. Unfortunately, when the formed oxide is removed from the first process tool (e.g., the furnace) the oxide may be exposed to the atmospheric conditions and contaminants, such as

moisture. Accordingly, in an embodiment of the present invention, a high quality oxide is formed and then inhibited from exposure to air and water prior to performing further processing operations.

[0024] Diffusion followed by dielectric deposition often involves multiple process tooling at a relatively high cost. Thus, in an embodiment, a silicon passivation operation is performed by growth of a thin, e.g., less than approximately 3 nanometers (and, possibly, less than approximately 2 nanometers) silicon oxide layer in a controlled atmosphere furnace tool. Within the same tool (and, specifically, without exposure to outside lab or fab atmospheric or ambient conditions), deposition of a doped wide bandgap semiconductor on the thin oxide layer follows. In one such embodiment, the furnace is either a low pressure chemical vapor deposition (CVD) furnace or a rapid thermal anneal, or rapid thermal processing (RTP) tool. In a specific embodiment, the oxide growth and deposition occurs on both sides of a substrate or wafer ultimately used to form a solar cell. In an embodiment, the film deposited on the oxide layer is wide bandgap semiconductor material, e.g., with a bandgap greater than approximately 3 electron Volts (eV), having one or more of a large valence band offset, moisture barrier properties, a low stress on silicon, and the ability to be contacted ohmically. Polycrystalline silicon is often coupled with a silicon substrate, but may not be most suitable for blocking minority carriers. By contrast, in an embodiment, the wide bandgap semiconductor material both blocks minority carriers and is highly conducting for majority carriers.

[0025] In an embodiment, wide bandgap materials are considered relative to a silicon substrate and may include, but are not limited to, doped amorphous-silicon, silicon carbide, or aluminum gallium nitride, as described in greater detail below. Doped polysilicon is another option that has been previously disclosed. Doped amorphous-silicon may be a good selection for passivation and ohmic contact. In one embodiment, the doped amorphous-silicon used is formed sufficiently thin to minimize optical absorption. In another embodiment, even higher bandgap materials are used to facilitate optical transmission on a light-receiving surface of a substrate, as described in greater details below. In an embodiment, a vacuum tool configuration with a tube low pressure chemical vapor deposition (LPCVD) reactor that can reach high temperatures, e.g., approximately 900 degrees Celsius, is used to form both an oxide and an overlying wide bandgap semiconductor material. In another embodiment, an RTP tool combined with a plasma enhanced CVD (PECVD) tool is

used to form both an oxide and an overlying wide bandgap semiconductor material. Other possible embodiments are described in greater detail below.

[0026] To better illustrate some of the concepts involved pertaining to at least some of the embodiments described herein, Figure 1 illustrates a band diagram as a function of increasing energy (E) for a conventional heterojunction contact without an interfacial tunnel oxide. Referring to Figure 1, the band diagram 100 of a conventional N-type substrate and wide bandgap passivation/contact showing valence energy level (E_{valence}), Fermi level, and conduction energy level (E_{conduction}) for electrons (majority carriers) and holes (minority carriers). Superior passivation may be achieved with a large minority carrier band offset, and superior ohmic contact may be achieved with a small majority carrier offset. However, it often proves difficult to fabricate a high bandgap material directly on a silicon substrate.

[0027] In comparison, Figure 2 illustrates a band diagram as a function of increasing energy (E) for a heterojunction contact with an interfacial tunnel oxide, in accordance with an embodiment of the present invention. Referring to Figure 2, the band diagram 200 of an N-type substrate and wide bandgap passivation/contact with a thin interfacial tunnel oxide there between showing valence energy level (E_{valence}), Fermi level, and conduction energy level (E_{conduction}) for electrons (majority carriers) and holes (minority carriers) is provided. In an embodiment, an interfacial oxide (e.g., a thin layer of SiO₂) 250 is provided to aid in the lowering of surface defect density. That is, in one embodiment, a thin dielectric (e.g., a tunneling oxide layer) is included between a silicon substrate and wide bandgap semiconductor interface to tie up surface states. In a specific embodiment, the passivation of the silicon substrate by dielectric 250 provides an interface with less than approximately 10¹² defects/cm². In an embodiment, even with the inclusion of such a dielectric layer, the Fermi level is near the band edge, as depicted in Figure 2.

[0028] There are possibly many processing schemes that may be suitable for providing a solar cell having a wide bandgap semiconductor material above a surface of a semiconductor substrate, with an interfacial dielectric and/or passivation layer disposed there between. As a basic example of such a process scheme, Figure 3 is a flowchart 300 representing operations in a method of fabricating a solar cell, in accordance with an embodiment of the present invention. Referring to operation 302 of flowchart 300, a method of fabricating a solar cell includes forming a thin dielectric layer on a surface of a semiconductor substrate of the solar cell. The thin dielectric

layer is formed in a process tool having a controlled atmosphere. Referring to operation 304 of flowchart 300, the method then includes forming a semiconductor layer on the thin dielectric layer without removing the semiconductor substrate from the controlled atmosphere of the process tool. In one such embodiment, the semiconductor layer has a bandgap at least approximately 0.2 electron Volts (eV) greater than the bandgap of the semiconductor substrate. In an embodiment, the method further includes forming an emitter region for the solar cell from the semiconductor layer.

[0029] There may be processing advantages associated with one or more embodiments of the present invention. For example, one or more embodiments described herein provide a single-operation passivation process. One or more embodiments described herein provide an ability to use such passivation for fabricating a back N-type contact, simplifying a solar cell process sequence beyond the single-operation passivation process. One or more embodiments described herein provide an approach to having no atmospheric exposure of a formed oxide. One or more embodiments described herein provide an approach for forming a high optical reflectance contact. One or more embodiments described herein provide an approach requiring no need for opening a contact window in the back of an N-type contact. One or more embodiments described herein provide an approach for facilitating full area metal contact formation.

[0030] In accordance with an embodiment of the present invention, an improved technique for manufacturing solar cells is to provide a thin dielectric layer and a deposited wide band gap semiconductor layer on the back side of a silicon substrate in a single process tool. A detailed processing scheme is provided below in order to illustrate one of the many possible embodiments for forming a wide bandgap semiconductor material and semiconductor substrate pair for forming emitter regions. Specifically, Figures 4A-4L illustrate cross-sectional views of various stages in the fabrication of a solar cell having an emitter region composed of a wide bandgap semiconductor material, in accordance with another embodiment of the present invention.

[0031] As an overview, in the particular embodiment illustrated, regions of doped polysilicon are first formed by dopant driving into deposited silicon layers, or by in-situ formation of doped polysilicon regions. An oxide layer and a layer of a wide band gap doped semiconductor are then formed on the front and back sides of

the solar cell, in a single process tool. One variant involves texturizing the front and back surfaces prior to formation of the oxide and wide band gap doped semiconductor formation. Contact holes may then be formed through the upper layers to expose the doped polysilicon regions. A metallization process may then be performed to form contacts onto the doped polysilicon layer. A second group of contacts may also be formed by directly connecting metal to emitter regions on the silicon substrate formed by the wide band gap semiconductor layer positioned between regions of the doped polysilicon on the back side of the solar cell. It is to be understood that embodiments of the present invention need not include all operations depicted and described, nor are embodiments limited to those depicted and described.

[0032] Referring to Figure 4A, a foundational structure 400 for fabricating a solar cell includes a silicon substrate 402 (e.g., an N-type single crystalline substrate), a thin dielectric layer 406, and a deposited silicon layer 404. In some embodiments, the silicon substrate 402 is cleaned, polished, planarized, and/or thinned or otherwise processed prior to the formation of the thin dielectric layer 406. The thin dielectric layer 406 and deposited silicon layer 404 may be grown through a thermal process.

[0033] Referring to Figures 4B and 4C, a layer of doping material 408 followed by a first oxide layer 410 are deposited over the deposited silicon layer 404 through conventional deposition processes. The layer of doping material 408 may include a doping material, or dopant 409, and may be composed of, but is not limited to, a layer of positive-type doping material such as boron or a layer of negative-type doping material such as phosphorous or arsenic. Although the thin dielectric layer 406 and deposited silicon layer 404 are described as being grown by a thermal process or deposited through conventional deposition process, respectively, each layer may be formed using an appropriate process. For example, a chemical vapor deposition (CVD) process, low-pressure CVD (LPCVD), atmospheric pressure CVD (APCVD), plasma-enhanced CVD (PECVD), thermal growth, or sputtering process, or another suitable technique may be used. In one embodiment, the doping material 408 is formed on the substrate 402 by a deposition technique, sputter, or print process, such as inkjet printing or screen printing, or by ion implantation.

[0034] Referring to Figure 4D, solar cell 400 is depicted following a material removal process applied to the structure of Figure 4C. The material removal process forms an exposed polysilicon region 424. Suitable examples of a material removal process include a mask and etch process, a laser ablation process, and other similar

techniques. The exposed polysilicon region 424 and layer of doping material 408 may be patterned to have a suitable shape and size for ultimate emitter formation. A suitable pattern layout may include, but is not limited to, formation of an interdigitated pattern. Where a masking process is used, it may be performed using a screen printer or an inkjet printer to apply a mask ink in predefined interdigitated pattern. Thus, conventional chemical wet etching techniques may be used to remove the mask ink resulting in the interdigitated pattern of exposed polysilicon regions 424 and layer of doping material 408. In one embodiment, portions or the entirety of the first oxide layer 410 are removed. Such removal may be accomplished in the same etching or ablation process in which regions of the deposited silicon layer 404, and dielectric layer 406 are removed.

[0035] Referring to Figure 4E, a second etching process may be performed to facilitate etching the exposed polysilicon regions 424 and to form a first texturized silicon region 430 on the back side of the solar cell 400 and a second texturized silicon region 432 on the front side of the solar cell 400 for increased solar radiation collection. A texturized surface may be one which has a regular or an irregular shaped surface for scattering incoming light, decreasing the amount of light reflected off of the light-receiving surface of the solar cell 400.

[0036] Referring to Figure 4F, the solar cell 400 may be heated 440 to drive the doping material 409 from the layer of doping material 408 into the deposited silicon layer 404. The same heating 440 may also form a silicon oxide or a second oxide layer 412 over the layer of doping material 408 and first texturized silicon region 430. During this process, a third oxide layer 414 may be grown over the second texturized silicon region 432. In one embodiment, both the oxide layers 412, 414 are composed of a high quality oxide. In a specific such embodiment, a high-quality oxide is a low interface state density oxide typically grown by thermal oxidation at temperatures greater than approximately 900 degrees Celsius and which can provide for improved passivation of exposed regions of substrate 402.

[0037] Thus, in an embodiment, at least a portion of the second oxide layer 412 is formed by consuming a portion of the semiconductor substrate 402 by thermal oxidation. In one such embodiment, consuming the portion of the semiconductor substrate 402 includes thermally oxidizing a portion of a single-crystalline N-type silicon substrate to form a silicon dioxide (SiO_2) 412 layer having a thickness of approximately 3 nanometers or less on the exposed surfaces of the silicon substrate.

In an alternative embodiment, a thin dielectric layer is formed on the first texturized silicon region 430 by depositing a dielectric material layer on the first texturized silicon region 430. In one such embodiment, the depositing involves forming an aluminum oxide (Al_2O_3) layer on the surface of a single-crystalline N-type silicon substrate. In a specific such embodiment, the aluminum oxide (Al_2O_3) layer is an amorphous aluminum oxide (Al_2O_3) layer. Such embodiments may be performed by, e.g., atomic layer deposition (ALD), or other suitable deposition techniques.

[0038] Referring to Figure 4G, in one embodiment, forming a doped polysilicon layer may be accomplished during the formation of oxide layers 412, 414 while simultaneously raising the temperature to drive the dopants 409 from the layer of doping material 408 into the deposited silicon layer 404. In one such embodiment, doping the deposited silicon layer 404 with dopants 409 from the layer of doping material 408 forms a crystallized doped polysilicon layer or a doped polysilicon layer 450. In a specific such embodiment, the doped polysilicon layer 450 is a layer of positively doped polysilicon if a positive-type doping material is used. In a particular such embodiment, the silicon substrate 402 is composed of a bulk N-type silicon substrate. In another specific embodiment, the doped polysilicon layer 450 is a layer of negatively doped polysilicon if a negative-type doping material is used. In a particular such embodiment, the silicon substrate 102 is composed of a bulk P-type silicon substrate. Overall, then, the deposited silicon layer 404 may therefore be doped with the doping material 409 from the layer of dopant material 408 to form a doped polysilicon layer 450.

[0039] Referring to Figure 4H, without removing the substrate 402 from the controlled atmosphere of the process tool used to form oxide layers 412, 414, a first wide band gap doped semiconductor layer 460 is deposited on the back side of the solar cell 400. In an embodiment, the first wide bandgap semiconductor layer 460 has a bandgap at least approximately 0.2 electron Volts (eV) above the bandgap of the semiconductor substrate 402. For example, the first wide bandgap semiconductor layer 460 may have a bandgap at least approximately 0.2 electron Volts (eV) above the bandgap of an N-type single crystalline silicon substrate with a bandgap of approximately 1.0 eV. In one such embodiment, the first wide bandgap semiconductor layer 460 is substantially transparent in the visible spectrum. In a specific such embodiment, the first wide bandgap semiconductor layer 460 has a bandgap greater than approximately 3 eV and is composed of a material such as, but

not limited to, aluminum nitride (AlN), aluminum gallium nitride ($\text{Al}_x\text{Ga}_{1-x}\text{N}$, where $0 < x < 1$), boron nitride (BN), 4H-phase silicon carbide (SiC) (approximately 3.23 eV), or 6H-phase silicon carbide (SiC) (approximately 3.05 eV). In another embodiment, the semiconductor substrate 402 is composed of single-crystalline N-type silicon and the first wide bandgap semiconductor layer 460 has a bandgap greater than approximately 1.5 eV and is composed of a material such as, but not limited to, amorphous silicon (a-Si, approximately 1.5 eV), silicon carbide (SiC, different phases above approx 2.0 eV), aluminum nitride (AlN), aluminum gallium nitride ($\text{Al}_x\text{Ga}_{1-x}\text{N}$, where $0 < x < 1$), or boron nitride (BN).

[0040] In an embodiment, forming oxide layers 412, 414 and the first wide bandgap semiconductor layer 460 in the same process tool involves using a low pressure chemical vapor deposition (LPCVD) chamber, a rapid thermal anneal (RTA) chamber, a rapid thermal processing (RTP) chamber, an atmospheric pressure chemical vapor deposition (APCVD) chamber, a hydride vapor phase epitaxy (HVPE) chamber, or both of an RTP chamber and a plasma enhanced chemical vapor deposition (PECVD) chamber. In an embodiment, the “same” process tool may be a single or multi-chamber process tool, so long as the atmosphere is a controlled atmosphere different from the atmosphere of the facility housing the process tool.

[0041] In an embodiment, the method further doping the first wide bandgap semiconductor layer 460 with charge carrier dopant impurity atoms having a concentration approximately in the range of $1 \times 10^{17} - 1 \times 10^{21}$ atoms/cm³. In one such embodiment, the doping is performed *in situ* during the forming of the first wide bandgap semiconductor layer 460. In an alternative such embodiment, the doping is performed subsequent to the forming of the first wide bandgap semiconductor layer 460.

[0042] Referring to Figure 4I, a second wide band gap doped semiconductor layer 462 may be deposited over the second texturized silicon region 432 on the front side of the solar cell 400. In an embodiment, the layers 460 and 462 are formed in the same process operation. In another embodiment, however, the layers 460 and 462 are formed in different process operations, in a same or different process tool. In one embodiment, both the wide band gap doped semiconductor layers 460, 462 on the back side and front side of the solar cell 400 are composed of a wide band gap negative-type doped semiconductor. In one embodiment, the second wide band gap doped semiconductor 462 is relatively thin as compared to the first thick wide band

gap doped semiconductor layer 460. In a specific such embodiment, the second thin wide band gap doped semiconductor layer 462 is approximately 10% to 30% of the thickness of the first thick wide band gap doped semiconductor layer 460. In another embodiment, both wide band gap doped semiconductor layers 460, 462 on the back side and front side of the solar cell 400 are composed of a wide band gap positive-type doped semiconductor. Subsequently, an anti-reflective coating (ARC) layer 470 may be deposited over the second wide band gap doped semiconductor 462, as depicted in Figure 4I. In one such embodiment, the ARC layer 470 is composed of silicon nitride.

[0043] Referring to Figure 4J, partial removal of the first wide band gap doped semiconductor 460, second oxide layer 412 and the layer of doping material 408 on the back side of the solar cell 400 is performed to form a series of contact openings 480. In one embodiment, the removal technique is accomplished using an ablation process. One such ablation process is a laser ablation process. In another embodiment, the removal technique is a conventional patterning process, such as screen printing or ink jet printing of a mask followed by an etching process. In an embodiment, forming the first wide bandgap semiconductor layer 460 includes forming a portion over at least a portion of the doped polysilicon layer 450, even after patterning of the doped polysilicon layer 450, as depicted in Figure 4J.

[0044] Referring to Figure 4K, a first metal grid or gridline 490 is formed on the back side of the solar cell 400. The first metal gridline 490 may be electrically coupled to the doped polysilicon 450 within the contact openings 480. In one embodiment, the first metal gridline 490 is formed through the contact openings 480 to the first wide band gap doped semiconductor 460, second oxide layer 412, and the layer of doping material 408 to connect a positive electrical terminal of an external electrical circuit to be powered by the solar cell 400.

[0045] Referring to Figure 4L, a second metal grid or gridline 492 is formed on the back side of the solar cell 400. The second metal gridline 492 may be electrically coupled to the second texturized silicon region 432. In one embodiment, the second metal gridline 492 is coupled to the first wide band gap doped semiconductor 460, second oxide layer 412, and the first texturized silicon region 430 acting as a heterojunction in areas of the back side of the solar cell 400 to connect to a negative electrical terminal of an external electrical circuit to be powered by the solar cell 400. In some embodiments, the forming of metal grid lines referenced in Figures 4K and 4L are performed through an electroplating process, screen printing process,

ink jet process, plating onto a metal formed from aluminum metal nanoparticles, or other metallization or metal formation processing operation.

[0046] Thus, in an embodiment, a first emitter region is formed from doped polycrystalline silicon, while a second emitter region is formed from a wide bandgap semiconductor material. In another embodiment, however, instead of doped polysilicon, the first emitter regions is also formed from a material having a bandgap at least approximately 0.2 electron Volts (eV) above the bandgap of 402, e.g., above a single-crystalline N-type silicon substrate.

[0047] In another aspect, as described above, with reference to Figure 4F, some embodiments include the use of a more exotic oxide layer as a passivating layer between a substrate and wide bandgap interface. In an exemplary embodiment, one such solar cell includes a silicon substrate. A first emitter region is disposed on a surface of the silicon substrate and is composed of an aluminum nitride (AlN) layer doped to a first conductivity type. The AlN layer is disposed on a thin aluminum oxide (Al₂O₃) layer. A second emitter region is disposed on the surface of the silicon substrate and is composed of a semiconductor material doped to a second, opposite, conductivity type. The second semiconductor material is disposed on a thin dielectric layer. First and second contacts are disposed on, and conductively coupled to, the first and second emitter regions, respectively.

[0048] In one such embodiment, the semiconductor material has a bandgap at least approximately 0.2 electron Volts (eV) above the bandgap of the silicon substrate. That is, both types of emitter regions include wide band gap materials. However, in another such embodiment, the semiconductor material is composed of polycrystalline silicon, e.g., similar to the structures described in association with Figures 4A-4K. In an embodiment, the first emitter region is disposed on a textured portion of the surface of the silicon substrate, and the second emitter region is disposed on a flat portion of the surface of the silicon substrate.

[0049] In one embodiment, the first and second emitter regions are disposed on a back-contact surface of the semiconductor substrate. The silicon substrate further includes a light-receiving surface opposite the back-contact surface. The light-receiving surface has a thin aluminum oxide (Al₂O₃) layer disposed thereon, and an aluminum nitride (AlN) layer disposed on the thin aluminum oxide (Al₂O₃) layer. In one embodiment, a portion of the aluminum nitride (AlN) layer is disposed over at

least a portion of the second emitter region, similar to the structure described in association with Figure 4J.

[0050] Several embodiments described herein include forming emitter regions for solar cells by providing a thin dielectric layer and a deposited wide band gap semiconductor layer on the back side of a silicon substrate in a single process tool. It is to be understood that other embodiments need not be limited there to. For example, in an embodiment, a passivation layer for a solar cell is formed by providing a thin dielectric layer and a deposited wide band gap semiconductor layer on the front and back sides of a silicon substrate in a single process tool. An emitter region need not be formed from the passivation layer.

[0051] Thus, solar cells having emitter regions composed of wide bandgap semiconductor material and methods of fabricating solar cells have been disclosed. In accordance with an embodiment of the present invention, a method includes forming a thin dielectric layer on a surface of a semiconductor substrate of the solar cell in a process tool having a controlled atmosphere. The semiconductor substrate has a bandgap. A semiconductor layer is then formed on the thin dielectric layer without removing the semiconductor substrate from the controlled atmosphere of the process tool. The semiconductor layer has a bandgap at least approximately 0.2 electron Volts (eV) above the bandgap of the semiconductor substrate. In one such embodiment, the method further includes forming an emitter region for the solar cell from the semiconductor layer. In another such embodiment, forming the semiconductor layer involves forming a layer substantially transparent in the visible spectrum.

What is claimed is:

1. A method of fabricating a solar cell, the method comprising:
forming, in a process tool having a controlled atmosphere, a thin dielectric layer of aluminum oxide (Al_2O_3) on a surface of a single crystalline N-type silicon semiconductor substrate of the solar cell, the semiconductor substrate having a bandgap; and, without removing the semiconductor substrate from the controlled atmosphere of the process tool, forming a semiconductor layer on the thin dielectric layer, the semiconductor layer being transparent in the visible spectrum and having a bandgap at least approximately 0.2 electron Volts (eV) above the bandgap of the semiconductor substrate and a bandgap of greater than 3 eV and comprising a material selected from the group consisting of: aluminum nitride (AlN), aluminum gallium nitride ($\text{Al}_x\text{Ga}_{1-x}\text{N}$, where $0 < x < 1$), and boron nitride (BN).
2. A method of fabricating a solar cell, the method comprising:
forming a first emitter region on a surface of a N-type silicon semiconductor substrate of the solar cell, the first emitter region comprising a semiconductor material doped to a first conductivity type and formed on a first thin dielectric layer; and
forming a second emitter region on the surface of the semiconductor substrate, the forming comprising:
forming, in a process tool having a controlled atmosphere, a thin dielectric layer of aluminum oxide (Al_2O_3) on a surface of a single crystalline N-type silicon semiconductor substrate of the solar cell, the semiconductor substrate having a bandgap; and, without removing the semiconductor substrate from the controlled atmosphere of the process tool, forming a semiconductor layer on the thin dielectric layer, the semiconductor layer being transparent in the visible spectrum and having a bandgap at least approximately 0.2 electron Volts (eV) above the bandgap of the semiconductor substrate and a bandgap of greater than 3 eV and comprising a material selected from the group consisting of: aluminum nitride (AlN), aluminum gallium nitride ($\text{Al}_x\text{Ga}_{1-x}\text{N}$, where $0 < x < 1$), and boron nitride (BN); and
doping the semiconductor layer with charge carrier dopant impurity ions of a second, opposite conductivity type.
3. The method of claim 1, further comprising:
forming an emitter region for the solar cell from the semiconductor layer.
4. The method of claim 1, further comprising:
doping the semiconductor layer with charge carrier dopant impurity atoms having a concentration approximately in the range of 1×10^{17} – 1×10^{21} atoms/cm³.
5. The method of claim 4, wherein the doping is performed in situ during the

forming of the semiconductor layer.

6. The method of claim 4, wherein the doping is performed subsequent to the forming of the semiconductor layer.

7. The method of claim 1, wherein forming the thin dielectric layer on the surface of the semiconductor substrate comprises consuming a portion of the semiconductor substrate by thermal oxidation.

8. The method of claim 1, wherein forming the thin dielectric layer and the semiconductor layer in the process tool comprises using a low pressure chemical vapor deposition (LPCVD) chamber, a rapid thermal anneal (RTA) chamber, a rapid thermal processing (RTP) chamber, an atmospheric pressure chemical vapor deposition (APCVD) chamber, a hydride vapor phase epitaxy (HVPE) chamber, or both of an RTP chamber and a plasma enhanced chemical vapor deposition (PECVD) chamber.

9. The method of claim 1, further comprising:
texturizing the surface of the semiconductor substrate prior to forming the thin dielectric layer.

10. The method of claim 1, wherein forming the thin dielectric layer and the semiconductor layer on the surface of the semiconductor substrate comprises forming on a back-contact surface of the semiconductor substrate, the forming further comprising forming the thin dielectric layer and the semiconductor layer on a light-receiving surface of the semiconductor substrate.

11. The method of claim 2, further comprising:
texturizing the surface of the semiconductor substrate prior to forming the second thin dielectric layer.