

SPECIFICATION

Receiver having a frequency synthesising circuit

The invention relates to a radio receiver.

Funkschau 1976 Volume 20, pages 839-842, discloses a receiver having a frequency synthesising circuit comprising a reference oscillator, a radio-frequency section, a local oscillator and an intermediate frequency section, the local oscillator being tunable by means of the reference oscillator to a frequency which deviates the intermediate frequency from the frequency of a transmitter to be received.

In this known receiver the input of the local oscillator is coupled to the frequency of an extremely stable reference oscillator, so that a very constant oscillator tuning is obtained. However it is not possible, as customary with receivers without frequency synthesising, to compensate for any variation in the tuning of the intermediate frequency section by causing compensating frequency variations of the local oscillator to be produced.

Whilst it would be possible to perform such a correction by means of an automatic frequency control circuit acting on a received signal, there is always the risk that the circuit locks in to an unwanted transmitter.

It is an object of the invention to provide a different method of correcting the oscillator frequency so that the risk of locking-in to an unwanted transmitter is reduced significantly or eliminated altogether.

According to the present invention there is provided a receiver comprising a radio-frequency section having an input for receiving an incoming signal via an aerial, a mixer having a first input coupled to an output of the radio-frequency section, a frequency synthesiser circuit including a tunable local oscillator which is connected to a second input of the mixer and an input for a tuning datum signal, an intermediate frequency section coupled to an output of the mixer, a reference oscillator having an output which is used to tune the frequency of the local oscillator, and an intermittently operable measuring circuit constructed or arranged to carry out the following operations (a) producing a measuring signal which can be applied to an input of the radio-frequency or intermediate section, instead of a signal to be received, (b) changing the frequency of the measuring signal or of the local oscillator signal, (c) measuring the response of the intermediate-frequency section to the changes in the measuring signal or in the local oscillator signal and (d) processing the measured response and producing a tuning datum signal which is applied to said input of the frequency synthesising circuit.

By temporarily supplying a measuring signal instead of an aerial signal to the receiver,

the receiver is prevented from locking-in to an unwanted transmitter. Using a correction circuit also ensures that, although the measuring signal is no longer supplied, the local oscillator of the receiver can be kept tuned very accurately to the frequency of the desired transmitter, without an automatic frequency control circuit.

The present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a block schematic diagram of a receiver made in accordance with the invention, and

Figure 2 is a block diagram of a portion of a measuring circuit for a receiver made in accordance with the invention.

In Fig. 1 a signal which is applied via a radio-frequency section 5 to a mixer stage 7 is obtained from an output 1 of a measuring circuit 3. In addition a signal, supplied by a local oscillator 9 is applied to the mixer stage 7. An output signal of the mixer stage 7 is applied to an intermediate-frequency section 11.

The local oscillator 9 forms part of a frequency synthesising circuit. The output signal of the oscillator 9 is applied via a pre-scaler 13, which divides by a fixed figure "P" and a scaler 15, which divides by an adjustable figure n , to an input of a phase detector 17, a further input of which is supplied with a reference signal via a scaler 19 dividing by q , from a reference oscillator 21 operating at a frequency f_{ref} . An output signal of the phase detector 17 controls the frequency f_{osc} of the oscillator so that $1/p \cdot 1/n f_{osc} = 1/q f_{ref}$ so that $f_{osc} = n p/q f_{ref}$. So the adjustable number n determines the frequency to which the oscillator is tuned. This number n is adjustable by means of a group of signals obtained via a group of leads from a group of outputs 23 of the measuring circuit 3. For clarity, these groups are shown single in Fig. 1.

The measuring circuit 3 has a switch 25 which can be operated by a measuring command generator 27. The measuring command generator 27 is controlled by a clock signal generator 28 and supplies periodically, for example every ten minutes, a signal with which the switch 25 is adjusted for a brief period of time to the position not shown in the drawing.

In the position, shown in the drawing, of the switch 25 a signal derived from an aerial 29 is available at the output 1 and a group of signals deriving from a correction circuit 31 is applied to the group of outputs 23. The correction circuit 31 serves for correcting a tuning datum, supplied by a control circuit 33, for a deviation of the frequency to which the intermediate-frequency section 11 is tuned relative to a standard intermediate frequency. This deviation can, for example, oc-

cur owing to temperature variations, ageing or inaccuracy during the adjustment.

The datum with which the tuning datum is corrected is derived from a calibration circuit 35 with which the deviation from the standard intermediate frequency is determined.

This occurs in the position, not shown in the drawing, of the switch 25. A signal, which is obtained from the reference oscillator

- 10 21 via a frequency multiplier 37 is applied to the output 1 of the measuring circuit via the upper contact of the switch 25. If the frequency multiplication factor of the frequency multiplier is h the frequency of the signal
15 applied to the radio-frequency section 5 is $h f_{ref}$.

- By means of the second contact of the switch 25 which symbolises a group of contacts a tuning datum is applied to the group
20 of outputs 23, which tuning datum is varied owing to the closing of the third contact of the switch 25 from the oscillator frequency corresponding to the desired intermediate frequency to a lower value, until the amplitude
25 of an intermediate frequency signal detected by a detector 41 and measured by means of a threshold circuit 39 exceeds a given threshold value. Thereafter, the tuning datum at the group of outputs 23 is changed so that the
30 oscillator frequency increases until the threshold circuit 39 again indicates that the threshold value is exceeded. The tuning datum located halfway between the two tuning data at which the threshold value is exceeded is
35 the correct tuning datum and the deviation thereof relative to the tuning datum associated with the desired oscillator frequency is determined and applied to the correction circuit 31, whereby the tuning data for transmitters
40 to be received are corrected.

- For the circuit discussed above h may be taken twenty seven for an FM-receiver having a reference oscillator 21 operating at 4 MHz. The frequency of the measuring signal then
45 becomes 108 MHz and the non-corrected oscillator frequency 118.7 MHz if the standard intermediate frequency is 10.7 MHz.

- If a measuring signal at an intermediate frequency is applied instead of one at a radio-frequency, then this may be done by switching-off the H.F. input signal and by tuning the local oscillator 9 to a suitable frequency. For a standard intermediate frequency of 10.7 MHz the frequency of the local oscillator 9 can, for
50 example, be varied around $10.7/2 = 5.35$ MHz for determining the frequency the intermediate frequency section is tuned to.

- For an A.M.-receiver having a standard intermediate frequency of 460 KHz and a reference oscillator frequency of 4 MHz the frequency of the measuring signal can be taken as 4 MHz ($h = 1$) and the oscillator frequency can be varied around 4.46 MHz.

- Instead of the detector 41 and the threshold circuit 39 it is alternatively possible, if so

desired, to use, for example, a frequency discriminator having a zero-crossing indicator. The zero-crossing frequency must then be determined with the calibration circuit 35.

- 70 If so desired, the measuring command generator 27 can be coupled to the control circuit 33 in such a way that a measuring cycle is performed a given period of time after the receiver has been switched-on.

- 75 If the measuring signal is applied at the radio frequency it is in principle possible to vary the frequency of this measuring signal instead of the oscillator signal. If so desired the measuring signal can alternatively be obtained from a separate oscillator. However,
80 the methods described above are, in general, simpler to be performed.

- In Fig. 2 components corresponding to components in Fig. 1 have been given the same reference numerals. Fig. 2 does not show the switching-over of the input of the radio-frequency section 5 of Fig. 1. Fig. 2 shows an embodiment of the remaining part of the measuring circuit 25 of Fig. 1.

- 90 As indicated above, the measuring command generator 27 is controlled by the clock signal generator 28 and the control circuit 33. The group of outputs 23 supplies a group of tuning data to the adjustable scaler 15 of Fig.
95 1.

- If an output 43 of the measuring command generator 27 supplies a measuring command signal this signal is applied to a reset input 45 of a flip-flops 47, to a reset input 49 of a flip-flop 51 and to a reset input 53 of a counter 55, which serves as an error store. Each of the flip-flops 47, 51 has an output 57, 59 which then becomes zero. The counter 55 has a group of outputs 61 which then all become
100 zero too. A NOR-gate 63 connected to the outputs 61 then supplies an output signal one to a NAND-gate 65, another input of which receives an output signal of an AND-gate 67 which is zero at this moment. The output
105 signal of the NAND-gate 65 then becomes one and closes a switch 69, causing clock pulses to be applied to various sections of the circuit.

- The output of an AND-gate 67 is zero
115 because an input thereof is connected to the output 59 of the flipflop 51 and this output 59 has become zero at the start of the measuring cycle.

- The output signal zero of the AND-gate 67
120 is further supplied to a reset input 71 of the measuring command generator 27, so that said generator is reset.

- The output signal of the AND-gate 67 furthermore adjusts a group of change-over
125 switches 73 to the position shown in the drawing as a result of which, owing to the output signal of the AND-gate 67 which is also applied to a writing signal input 75 of the counter 31, a group of tuning data from a
130 store 77 is entered into the counter 31. This

tuning datum is applied to the group of outputs 23 as a result of which the frequency synthesising circuit tunes to a frequency corresponding to the frequency of the output signal of the multiplier 37 of Fig. 1, so that a signal having the standard intermediate frequency is applied to the intermediate frequency section 11. This causes the threshold circuit 39 to supply an output signal "one" to a setting input 79 of a flip-flop 81. The reset input of this flip-flop 81 is connected to the output of the switch 69 and receives clock pulses.

Under the influence of the output signal zero of the AND-gate 67 a switch 83 is adjusted to the position shown in the drawing, which causes the output signal of the flip-flop 47 to be fed to a switch 85 which is adjusted to the position shown in the drawing. Furthermore, the output signal of the AND-gate 67 is applied to an input of AND-gate 87, to another input of which the inverted signal of the most significant output of the group of outputs 61 of the counter 55 is applied. The output of this AND-gate is connected to an input of an OR-gate 89, the other input of which is connected to the output 57 of the flip-flop 47. The output signal of the AND-gate 87 is zero because the output signal of the AND-gate 67 is zero. The output signal of the OR-gate 89 is also zero because its two inputs signals are zero.

The output signal zero of the OR-gate 89 moves a switch 91 to the position shown in the drawing, which causes the clock signal from the output of the switch 69 to be fed to the down counting input 93 of the counter 31. Furthermore, the output signal of the OR-gate 89 adjusts a switch 95 to the position shown in the drawing, causing a down-counting input 97 of a counter 99 to be connected to an output of a change-over switch 101. The switch 101 is operated by the signal originating from the output 59 of the flip-flop 51 and is, consequently, adjusted to the position shown in the drawing.

A reset input 103 of the counter 99 is connected via a capacitance to the output of the OR-gate 89. A group of outputs 105 of the counter 99 is connected to a further input of the AND-gate 67 through a NOR-gate 107. If the counter 99 is in a zero position, its outputs 105 are zero and the output signal of the NOR-gate 107 is one.

Furthermore, a signal is applied from the output of AND-gate 67 to an OR-gate 109, to a further input of which the output signal of the flip-flop 81 is applied. This output signal is zero because this flip-flop 81 is kept in the set state by the voltage at its input 79. The output of the OR-gate 109 is connected to the clock signal inputs 111, 113 of the flip-flops 47, 51.

In the position, shown in the drawing, obtained by starting a measuring cycle, clock pulses are now applied through the switch 91

to the counting-down input 93 of the counter 31 so that the tuning frequency is reduced, through the switch 85 to a counting-down input of the counter 55, via a two-scaler 117 and the switches 101 and 95 to the counting-down input of the counter 99 and to a resetting input 119 of the flip-flop 81.

However, this flip-flop 81 remains set for the time its setting input 79 is high.

The further progress of the measuring cycle is not determined in the first place by the flip-flop 81. If the threshold circuit 39 indicates that a threshold is exceeded and brings the voltage at the setting input 79 of the flip-flop 81 from one to zero, the output of the flip-flop 81 becomes high at the next clock pulse at the resetting input 119.

The flip-flop 81 is of the set-reset type and supplies a positive pulse at its output, said pulse being passed-on to the inputs 111 and 113 of the flip-flops 47, 51 through the OR-gate 109. The flip-flop 47 is of the JK-type, the J and K-input being connected to a positive voltage. This flip-flop 47 changes state owing to the signal at its input 111 and its output 57 becomes one. The flip-flop 51 is of the D-type and takes-over, at the instant the positive pulse at the input 113 occurs, the signal value at its D-input 121, which is connected to the output 57 of the flip-flop 47. This value was zero and, consequently, the output 59 of the flip-flop 51 remains zero.

As a result of the fact that the output 57 of the flip-flop 47 becomes one, the switch 85 is switched to the position not shown in the drawing, so that an up-counting input 123 of the counter 55 is connected to the output of the switch 69. The output signal of the OR-gate 89 becomes one too so that the switch 91 is switched to the position not shown in the drawing and an up-counting input 125 of the counter 31 is connected to the output of the switch 69. Also the switch 95 is switched to the position not shown in the drawing as a result of the fact that the output signal of the OR-gate 89 becomes one. As a consequence, an up-counting input 127 of the counter 99 is fed with clock pulses through the two-scaler 117. Furthermore, the counter 99 is reset as a result of the fact that its input 103 counts one. The position of the counter 31 is now a tuning datum (-A), that of the counter 55 is (-A) and that of the counter 99 is zero, if A clock pulses have occurred between the start and the change in state.

The counters 31, 55 and 99 now count upwards till the threshold circuit 39 again supplies a down-going signal after B clock pulses. The flip-flop 81 supplies a pulse again to the OR-gate 109 which passes this pulse on to the inputs 111, 113 of the flip-flops 47, 51. The flip-flop 51 now takes over the output signal one of the flip-flop 47 so that its output 59 becomes one and the flip-flop 47 changes state again so that its output 57

becomes zero.

The position of the counter 31 is now tuning datum ($-A + B$), that of the counter 55 is ($-A + B$) and that of the counter 99 is ($+B/2$). The output signals of the counter 99 now cause the output of the NOR-gate 107 to become zero so that the input of the AND-gate 67, connected thereto, becomes zero and the output signal thereof remains zero.

- 10 As a result of the fact that the output signal of the flip-flop 51 becomes one the switch 101 is changed-over so that it now passes pulses of the clock frequency. The output signal of the OR-gate 89 becomes zero again so that the switch 95 returns to the position shown in the drawing. The switch 85 also returns to the position shown in the drawing, which also holds for the switch 91.

- 20 The counters 31, 55 and 99 now count $B/2$ clock-pulses downwards, which causes the output signal of the NOR-gate 107 to become one, the output signal of the AND-gate 67 also becoming one as the other input thereof remains one because the state of the flip-flops 81, 47, 51 has now changed.

- 25 The counter 55 now contains the number ($-A + B/2$) indicating how much the tuning of the measured intermediate frequency deviates relative to the standard intermediate frequency. This number must now be introduced as a correction in the tuning datum for a transmitter to be received. This is done under the influence of the gates 63, 65, 67, 87, 89.

- 35 Owing to the fact that the output of the AND-gate 67 becomes one, the switch 83 is adjusted to the position not shown in the drawing. The switch 85 is now operated by the output signal of the OR-gate 89 and, owing to an inverter circuit 129, in the opposite sense relative to the switch 91. Also the switch 73 is adjusted to the position not shown in the drawing and a tuning number for a desired transmitter is now entered into the counter 31 as the result of the signal at the writing input 75.

If the counter 55 has a negative content, its most significant output is one, this output being zero in the case of a positive content.

- 50 The AND-gate 87 then supplies a signal zero when the content of the counter is negative, and a one when the content is positive. This signal is passed by the OR-gate 89. The counters 31 and 55 now run in the opposite sense. If the content of the counter 55 was positive, the counter 55 counts down and the counter 31 counts upwards. The reverse occurs with a negative content of the counter 55.
- 60 If the content of the counter 55 has become zero, the output of the NOR-gate 63 becomes one and, consequently, the output of the NAND-gate 65, and the switch 69 is adjusted to the position now shown in the drawing, which causes the counters to stop.

The tuning datum in the counter 31 has then been corrected for a deviation in the tuning of the intermediate frequency section relative to a standard frequency.

- 70 Although in the preceding a receiver having a frequency synthesising circuit with an adjustable scaler was discussed it will be obvious that these measures are also possible for other types of frequency synthesising circuits for which the tuning datum must be entered in the form of a number.

- 75 In addition, it will be obvious that processing the measured deviation of the intermediate frequency relative to a standard frequency into the tuning datum can be effected in a different manner if so desired.

- 80 Parts of a receiver in accordance with the invention, of course may be realised with the aid of a processor, such as a microprocessor, and may be present only temporarily because a processor alternately constructs circuits for performing different functions under control of a program using a same unit for those different functions.

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CLAIMS

1. A receiver comprising a radio-frequency section having an input for receiving an incoming signal via an aerial, a mixer having a first input coupled to an output of the radio-frequency section, a frequency synthesiser circuit including a tunable local oscillator which is connected to a second input of the mixer and an input for a tuning datum signal, an intermediate frequency section coupled to an output of the mixer, a reference oscillator having an output which is used to tune the frequency of the local oscillator, and an intermittently operable measuring circuit constructed or arranged to carry out the following operations (a) producing a measuring signal which can be applied to an input of the radio-frequency or intermediate section, instead of a signal to be received, (b) changing the frequency of the measuring signal or of the local oscillator signal, (c) measuring the response of the intermediate-frequency section to the changes in the measuring signal or in the local oscillator signal and (d) processing the measured response and producing a tuning datum signal which is applied to said input of the frequency synthesising circuit.
2. A receiver as claimed in Claim 1, wherein parts of the receiver are implemented with the aid of a programmed microprocessor.
3. A receiver as claimed in Claim 1, wherein the measuring circuit comprises means for carrying out the said operations (a) to (d).
4. A receiver as claimed in Claim 3, wherein the measuring circuit includes means for changing the frequency of the local oscillator.
5. A receiver as claimed in any one of Claims 1 to 4, wherein the measuring signal is derived from the reference oscillator.
6. A receiver as claimed in any one of



becomes zero.

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- 10 As a result of the fact that the output signal of the flip-flop 51 becomes one the switch 101 is changed-over so that it now passes pulses of the clock frequency. The output signal of the OR-gate 89 becomes zero again
- 15 so that the switch 95 returns to the position shown in the drawing. The switch 85 also returns to the position shown in the drawing, which also holds for the switch 91.

- The counters 31, 55 and 99 now count
- 20 $B/2$ clock-pulses downwards, which causes the output signal of the NOR-gate 107 to become one, the output signal of the AND-gate 67 also becoming one as the other input thereof remains one because the state of the flip-flops 81, 47, 51 has now changed.

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- 30 as a correction in the tuning datum for a transmitter to be received. This is done under the influence of the gates 63, 65, 67, 87, 89.

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- 75 which the tuning datum must be entered in the form of a number.

- In addition, it will be obvious that processing the measured deviation of the intermediate frequency relative to a standard frequency
- 80 into the tuning datum can be effected in a different manner if so desired.

- Parts of a receiver in accordance with the invention, of course may be realised with the aid of a processor, such as a microprocessor,
- 85 and may be present only temporarily because a processor alternately constructs circuits for performing different functions under control of a program using a same unit for those different functions.

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CLAIMS

1. A receiver comprising a radio-frequency section having an input for receiving an incoming signal via an aerial, a mixer having a first input coupled to an output of the radio-frequency section, a frequency synthesiser circuit including a tunable local oscillator which is connected to a second input of the mixer and an input for a tuning datum signal, an
- 100 intermediate frequency section coupled to an output of the mixer, a reference oscillator having an output which is used to tune the frequency of the local oscillator, and an intermittently operable measuring circuit constructed or arranged to carry out the following operations (a) producing a measuring signal which can be applied to an input of the radio-frequency or intermediate section, instead of a signal to be received, (b) changing the frequency of the measuring signal or of the local oscillator signal, (c) measuring the response of the intermediate-frequency section to the changes in the measuring signal or in the local oscillator signal and (d) processing the measured response and producing a tuning datum signal which is applied to said input of the frequency synthesising circuit.

2. A receiver as claimed in Claim 1, wherein parts of the receiver are implemented with the aid of a programmed microprocessor.

3. A receiver as claimed in Claim 1, wherein the measuring circuit comprises means for carrying out the said operations (a) to (d).

4. A receiver as claimed in Claim 3, wherein the measuring circuit includes means for changing the frequency of the local oscillator.

5. A receiver as claimed in any one of Claims 1 to 4, wherein the measuring signal is derived from the reference oscillator.

- 130 6. A receiver as claimed in any one of



Claims 1 to 5, further comprising means for actuating the measuring circuit periodically.

5. A receiver substantially as hereinbefore described with reference to or as shown in the accompanying drawings.

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