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**An Improved Cost/Performance System Memory Unit
Using Extended Data Out Dynamic Random Access Memory**

BACKGROUND OF THE INVENTION

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1. Field of the Invention:

The present invention relates to the field of computer systems. More specifically, the present invention relates to system memory of computer systems.

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2. Background Information:

All computer systems include some amount of system memory. System memory is substantially slower than the processor. Most computer systems further include cache memory to bridge the performance gap between the processor and the system memory. While cache memory is still slower than the processor, it is faster than system memory. As processor speed continues to increase, various techniques have been developed to allow cache memory to keep up with the faster processors. Some of these improved cache memory units are capable of performing a cache access in as little as six clock cycles at 66 MHz processor speed (15ns per clock period). The improved cycle time represents 30% - 50% reduction of the cycle time required by the traditional cache memory units. In contrast, the memory access cycle time for the most common system memory units using CMOS technology based dynamic random access memory (DRAM) has remained pretty much unchanged, requiring 18 - 20 clock cycle at 66 MHz. Therefore, it is desirable to be able to reduce the memory access cycle time of system memory to keep pace with the improved cache memory.

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One emerging solution to the "slow" system memory problem is to use faster Synchronous DRAMs (SDRAMs) based on bi-CMOS technology. SDRAMs are about 100% faster than the

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conventional DRAMs. As a result, these faster system memory units can reduce the cycle time of a memory access by almost 50%. At 66 MHz, a memory access can be completed in as little as seven to ten clock cycles. However, today, SDRAMs cost twice as much as the conventional

5 DRAMs. In other words, it takes almost 100% increase in system memory cost to achieve 50% reduction in memory access cycle time. Thus, the faster system memory unit using SDRAMs is not an economically viable solution for the low end computer systems, such as entry level microprocessor based portable or desktop computers.

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Thus, it is desirable to close the performance gap between the improved cache memory and the "slow" system memory with a much more cost effective solution. As will be disclosed in more detail below, the present invention advantageously achieves these and other

15 desirable results.

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SUMMARY OF THE INVENTION

Under the present invention, the desired results are advantageously achieved by providing a system memory unit to a computer system comprising memory address and control generation circuitry, a number of banks of extended data out dynamic random access memory (EDODRAM, also known as Hyperpage DRAM in the art), and a number of registers. The memory address and control generation circuitry is used to generate memory addresses for the EDODRAMs, advantageously delivered over two address bus lines. Additionally, the memory address and control generation circuitry is used to generate control signals for the EDODRAMs and the registers, including advantageously "shortened" column address strobe signals (CAS). The EDODRAMs are used to accept, store, and output data, in accordance to the memory addresses provided. The registers are used to stage the data being streamed out of or into the EDODRAMs. As a result of the advantageous manner of delivering memory addresses and CAS signals to the EDODRAMs, the cycle time of a memory access is reduced, even if the slower CMOS technology based circuit elements are used to constitute the memory address and control generation circuitry, the EDODRAMs, and the registers.

During operation, the memory address and control generation circuitry provides the MSBs of the generated memory addresses over one address bus line, and the LSBs of the generated memory addresses over another address bus line, thereby allowing the column memory address to be rapidly changed. The memory address and control generation circuitry, exploiting the independence of EDODRAMs' data out relative to the CAS signals, advantageously withdraws the CAS signal at an early time for each column memory address to allow early precharge of memory cell and in turn faster response to the column memory address.

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Experience has shown that at a processor speed of 66 MHz, under the present invention, a memory access can be performed in about 11 - 13 clock cycles, which represents around 35% reduction in cycle time, even when conventional CMOS technology based circuit elements are used to constitute the system memory unit. More importantly, the 35% reduction in cycle time is achieved with very little increase in cost.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates an exemplary computer system incorporating the teachings of the present invention.

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Figure 2 illustrates the relevant portions of one embodiment of the system memory unit of the present invention of **Figure 1** in further detail.

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Figure 3 illustrates the key elements of the address generation portion of one embodiment of the memory address and control generation circuitry of **Figure 2** in further detail.

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Figures 4a - 4b are two timing diagrams for the system memory unit of the present invention of **Figure 1** operating at an exemplary processor speed of 66 MHz.

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DETAILED DESCRIPTION

In the following description, for purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without the specific details. In other instances, well known systems are shown in diagrammatic or block diagram form in order not to obscure the present invention unnecessarily.

Referring now to **Figure 1**, a block diagram illustrating an exemplary computer system incorporating the teachings of the present invention is shown. The exemplary computer system **10** comprises a processor **12**, a cache memory **14**, a system memory **16**, and a controller **15** coupled to each other through the processor bus **13**. Additionally, the exemplary computer system **10** further comprises a number of I/O devices **18** coupled to the controller **15** through an I/O bus **20**. In the presently preferred embodiment, the processor **12** is disposed in a single integrated circuit (chip). The processor chip, the cache memory **14**, the system memory **16**, the controller **15**, and the two buses **13** and **20** are disposed on a single circuit board. Except for the teachings incorporated in the system memory unit **16**, the processor **12**, the cache memory **14**, ..., and the I/O bus **20** are intended to represent a broad category of these elements found in many computer systems. Their constitutions and functions are well known and will not be further described.

While the present invention is being described with the exemplary computer system having the illustrated architecture, and the above described disposition, based on the description to follow, it will be appreciated that the present invention may be practiced with computer systems having different architectures and these elements physically disposed in other manners.

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Referring now to **Figure 2**, a block diagram illustrating the relevant portions of one embodiment of the system memory **16** of **Figure 1** in further detail. As illustrated, the system memory **16** comprises memory address and control generation circuitry **22**, a number of banks of EDODRAM **24**, a number of registers **26a - 26b**, and preferably a buffer **34**, coupled to each other as shown. As illustrated, the coupling between memory address and control generation circuitry **22** and the EDODRAMs **24** preferably includes at least two address bus lines **28a** and **28b**. The EDODRAMs **24** are organized in pages.

The memory address and control generation circuitry **22** is used to generate memory addresses for the EDODRAMs **24**. Additionally, the memory address and control generation circuitry **22** is used to generate control signals for the EDODRAMs **24** and the registers **26a - 26b**. The buffer **34** is used to buffer the most significant bits (MSBs) of the memory addresses. The buffer **34** is preferably employed to reduce the amount of power required to drive the MSBs of the memory addresses over the first address bus line **28a** for the EDODRAMs **24**, since typically system memory includes a large number of banks. The EDODRAMs **24** are used to accept, store, and output data. The EDODRAMs **24** store and output data in accordance to the memory addresses provided. The registers **26a - 26b** are used to stage the data being stored into or output from the EDODRAMs **24**.

During operation, the memory address and control generation circuitry **22** receives address and control signals over the processor bus **13**. In response, the memory address and control generation circuitry **22** generates memory addresses for the EDODRAMs **24**. Additionally, the memory address and control generation circuitry **22** provides control signals to the EDODRAMs **24** and the registers **26a - 26b**, including a row address strobe signal (RAS) and a column address strobe signal (CAS) for the EDODRAMs **24**, and store signals (MST and WST) for the registers **26a - 26b**. The controller **15** generates all other control signals as needed by the EDODRAMs **24**.

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As illustrated, the MSBs of the memory addresses, row or column, are preferably provided to the EDODRAMs 24 over the first address bus line 28a, whereas the LSBs of the memory addresses, row or column, are preferably provided to the EDODRAMs 24 over the second address bus line 28b. As will be described in more detail below, as a result of the advantageous manner of providing the memory addresses to the EDODRAMs 24, the memory addresses, in particular the column addresses, are provided at a faster rate to the EDODRAMs 24. Additionally, the memory address and control generation circuitry 22, exploiting the independence of EDODRAMs' data out relative to the CAS signal, advantageously withdraws the CAS at an early time for each column memory address to allow early precharge of the memory cells. As will be also described in more detail below, as a result of the advantageous manner of providing the CAS signal, data are streamed out of or into the EDODRAMs 24 at a faster rate. Together, the faster provision of memory addresses and the faster response of the EDODRAMs 24 result in reduction in the total cycle time of a memory access.

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The EDODRAMs 24 receive the memory addresses and the control signals as inputs. In response, the EDODRAMs 24 stream data out of or into the EDODRAMs (MDATA). The register 26a stores each of the data being streamed out of the EDODRAMs 24 for a read access momentarily to accommodate processor set up time, responsive to the MST signal. The register 26b stores each of the data being streamed into the EDODRAMs 24 for a write access momentarily for symmetry of operation, responsive to the WST signal.

30

The memory address and control generation circuitry 22 will be described in more detail below. A particular example of EDODRAM 24 is CMOS technology based KM44C4004A manufactured by Samsung Corporation of Korea, having operating speeds of 60 ns for RAS to data and 15ns for CAS to data. The registers 26a - 26b are well

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known and will not be further described. The timing of the key signals to effectuate the consecutive and rapid streaming of data out of and into the EDODRAMs 24 will be described in more detail below.

5 Referring now to **Figure 3**, a block diagram illustrating the key element of the address generation portion of one embodiment of the memory address and control generation circuitry 22 of **Figure 2** in further detail is shown. The control signal generation portion of the memory address and control generation circuitry 22 may be
10 implemented in any number of manners known in the art. As illustrated, the address generation portion 23 comprises a register 32, an incrementor 28, and an assembly of XOR gates 30, coupled to each other as shown. The register 32 stores the start address received over the processor bus 13. The incrementor 28 generates a predetermined
15 series of increment values. The assembly of XOR gates 20 generates the LSBs of the memory addresses by performing a series of logical XOR operations against the LSBs of the stored start address read out of the register 32, and the generated increment values.

20 The manner in which the incrementor 28 generates the increment values, and the XOR operations performed are dependent on the system memory access characteristics of the processor 12 and/or the cache memory 14. For example, for Intel Corporation's Pentium™ processor, if the addresses for a line fill are 0x00001010H,
25 0x00001018H, 0x00001000H, and 0x00001008H, the row memory addresses are 0x000H, whereas the column memory addresses are 0x202H, 0x203H, 0x200H, and 0x201H. In other words, MA[10:2]s are 0x200H for all four column memory addresses, and MA[1:0]s are 0x2H, 0x3H, 0x0H, and 0x1H for the four column memory addresses.

30 The LSBs of the memory addresses are advantageously "split off" and delivered to the EDODRAMs 24 over the second address bus line 28b, to allow the column memory address to be changed at a faster rate by bypassing the buffer 34 and saving the time otherwise

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would have incurred in changing the content of the buffer 34 when changing the column memory address. Since only a small number of bits are being driven directly for the EDODRAMs 24, the faster rate of delivering column addresses is advantageously achieved with minimal increase in power requirement of the memory address and control generation circuitry 22.

Referring now to **Figures 4a - 4b**, two timing diagrams illustrating the relative timing for a number of key signals for a read and a write access against the system memory 16 of **Figure 1** are shown. The relative timings of both diagrams are illustrated at an exemplary processor speed of 66 MHz (15ns per clock period) 42, and assuming page hit, i.e. the row memory address remains unchanged from the prior access. Thus, for both the read and the write access, the page hit signals (PGHIT) 46, and the RAS signals 52 are simply maintained active through the entire duration (t_0 through t_{10}) as shown in the two diagrams. Similarly, the MSBs of the memory column address (MA[10:2]) 48, and therefore the buffered MSBs (BMA[10:2]) 52 are maintained for the entire duration (t_0 through t_{10}) as shown in the two diagrams.

Referring now only to **Figure 4a**, for a read access, since the LSBs of the memory column addresses can be generated rapidly, and except for the first memory column address, the subsequent column memory addresses are responded to in 15ns, the LSBs of the memory column addresses (MA[1:0]) 50 are provided and maintained using about 11 clock periods (t_0 through t_{10}) as illustrated. The CAS signal 56 is pulled down correspondingly and early withdrawn in eight clock periods (t_3 through t_{10}) as illustrated.

Thus, the memory data (MDATA) 58 are detected in the nine clock periods (t_3 through t_{11}) as illustrated. The internal register data (IREGDATA) 61 are stored in the nine clock periods (t_4 through t_{12}) as illustrated. The MST signal 60 is therefore pulled down correspondingly in the eight clock periods (t_5 through t_{12}) as illustrated.

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As a result, read data (ODATA) are detected in the eight clock periods (t_6 through t_{13}) as illustrated. In other words, the total cycle time for a read access is reduced to 13 clock periods, a 35% improvement in total cycle time, even if the slower CMOS technology based EDODRAMs are used.

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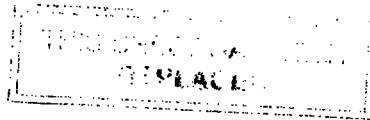
Referring now only to **Figure 4b**, for a write access, similarly, since the LSBs of the memory column addresses can be generated rapidly, and except for the first memory column address, the subsequent column memory addresses are responded to in 15ns, the
10 LSBs of the memory column addresses (MA[1:0]) **50** are provided and maintained using about 11 clock periods (t_0 through t_{10}) as illustrated. The CAS signal **54** is pulled down correspondingly and early withdrawn in eight clock periods (t_3 through t_{10}) as illustrated.

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Thus, with the write data **63** supplied using nine clock periods (t_0 through t_8) as illustrated, the internal register data (IREGDATA) **61** are stored in the nine clock periods (t_4 through t_{12}) as illustrated. The WST signal **59** is pulled down correspondingly in the eight clock periods (t_1 through t_8) as illustrated. As a result, memory data
20 are available for storage in the nine clock periods (t_2 through t_{10}) as illustrated. In other words, the total cycle time for a write access is reduced to 11 clock periods, a 39% improvement in total cycle time, even if the slower CMOS technology based EDODRAMs are used.

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While the present invention has been described in terms of presently preferred and alternate embodiments, those skilled in the art will recognize that the invention is not limited to the embodiments described. The method and apparatus of the present invention can be practiced with modification and alteration within the spirit and scope of
30 the appended claims. The description is thus to be regarded as illustrative instead of limiting on the present invention.



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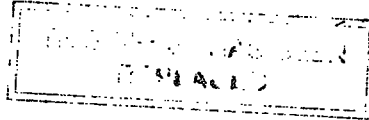
CLAIMS

What is claimed is:

- 5 1. A system memory unit comprising:
(a) address and control generation circuitry for generating a sequence of memory addresses and control signals for a read access, said control signals include column address strobe (CAS) signals that are early withdrawn;
- 10 (b) a number of banks of extended data out dynamic random access memory (EDODRAM) coupled to said address and control generation circuitry for storing a plurality of data in a plurality of memory cells of said EDODRAMs, and outputting a subset of said data responsive to said sequence of memory addresses and control signals,
- 15 said EDODRAM maintaining data out independent of said CAS signals and precharging memory cells upon withdrawal of said CAS signals.
2. The system memory unit as set forth claim 1, wherein, said address and control generation circuitry is sufficiently powered to directly
- 20 drive said generated sequence of memory addresses for all banks of EDODRAMs.
3. The system memory unit as set forth claim 1, wherein, said address and control generation circuitry generates common most
- 25 significant bits (MSBs) of said sequence of memory addresses and non-common least significant bits (LSBs) of said sequence of memory addresses, said non-common LSBs being generated consecutively, and said common MSBs being generated while said uncommon LSBs are generated.
- 30 4. The system memory unit as set forth in claim 3, wherein said address and control generation circuitry consecutively generates said uncommon LSBs in a plurality of consecutive clock

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periods, and generates said common MSBs during all of said consecutive clock periods;

said address and control generation circuitry further generates and withdraws said CAS signals correspondingly; and

- 5 said EDODRAMs consecutively outputs said subset of data correspondingly, precharging appropriate memory cells upon withdrawal of said CAS signals.

5. The system memory unit as set forth in claim 4, wherein
10 said address and control generation circuitry consecutively generates said uncommon LSBs in eleven consecutive clock periods, and generates said common MSBs during all of said eleven consecutive clock periods;

- said EDODRAMs consecutively outputs said subset of data
15 correspondingly in nine consecutive clock periods.

6. The system memory unit as set forth in claim 5, wherein,
 said system memory unit is coupled to a processor operating at a processor speed of at most 66 MHz; and
20 said address and control generation circuitry and said EDODRAMs are constituted with circuit elements based on CMOS technology.

7. The system memory unit as set forth in claim 3, wherein address
25 generation portion of said address and control generation circuitry comprises:

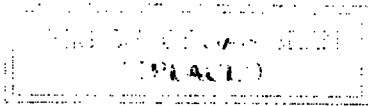
 (a.1) a register for storing and outputting an access address for said read access;

- (a.2) an incrementor for receiving a base value and generating a
30 plurality of incremental values in a predetermined manner; and

 (a.3) an XOR gate assembly coupled to said register and said incrementer for generating said LSBs using said access address and said incremental values.

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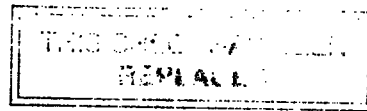




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8. The system memory unit as set forth in claim 3, wherein said system memory unit further comprises a buffer coupled to said address and control generation circuitry and said EDODRAMs for buffering said common MSBs of said sequence of memory addresses generated by said address and control generation circuitry for said EDODRAMs.
9. A system memory unit comprising:
- (a) address and control generation circuitry for generating a sequence of memory addresses and control signals for a write access, said control signals include column address strobe (CAS) signals that are early withdrawn;
 - (b) a number of banks of extended data out dynamic random access memory (EDODRAM) coupled to said address and control generation circuitry for accepting and storing a plurality of data in a plurality of memory cells of said EDODRAMs, responsive to said sequence of memory addresses and control signals, said EDODRAM maintaining data out independent of said CAS signals and precharging memory cells upon withdrawal of said CAS signals.
10. The system memory unit as set forth in claim 9, wherein, said address and control generation circuitry is sufficiently powered to directly drive said generated sequence of memory addresses for all banks of EDODRAMs.
11. The system memory unit as set forth in claim 9, wherein, said address and control generation circuitry generates common most significant bits (MSBs) of said sequence of memory addresses and non-common least significant bits (LSBs) of said sequence of memory addresses, said non-common LSBs being generated consecutively, and said common MSBs being generated while said uncommon LSBs are generated.
12. The system memory unit as set forth in claim 11, wherein





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said address and control generation circuitry consecutively generates said uncommon LSBs in a plurality of consecutive clock periods, and generates said common MSBs during all of said consecutive clock periods;

5 said address and control generation circuitry further generates and withdraws said CAS signals correspondingly; and

said EDODRAMs consecutively accepts and stores said subset of data correspondingly, precharging appropriate memory cells upon withdrawal of said CAS signals.

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13. The system memory unit as set forth in claim 12, wherein said address and control generation circuitry consecutively generates said uncommon LSBs in eleven consecutive clock periods, and generates said common MSBs during all of said eleven consecutive

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clock periods;
said EDODRAMs consecutively accept and store said subset of data correspondingly in nine consecutive clock periods.

14. The system memory unit as set forth in claim 13, wherein, said system memory unit is coupled to a processor operating at a processor speed of at most 66 MHz; and

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said address and control generation circuitry and said EDODRAMs are constituted with circuit elements based on CMOS technology.

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15. The system memory unit as set forth in claim 11, wherein address generation portion of said address and control generation circuitry comprises:

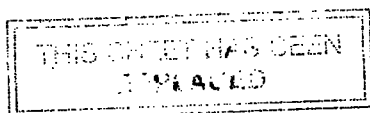
(a.1) a register for storing and outputting an access address for said write access;

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(a.2) an incrementor for receiving a base value and generating a plurality of incremental values in a predetermined manner; and

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(a.4) an XOR gate assembly coupled to said register and said incrementer for generating said LSBs using said access address and said incremental values.

5 16. The system memory unit as set forth in claim 11, wherein said system memory unit further comprises a buffer coupled to said address and control generation circuitry and said EDODRAMs for buffering said common MSBs of said sequence of memory addresses generated by said address and control generation circuitry for said EDODRAMs.

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17. A method for accepting, storing, and outputting data comprising:
(a) generating a sequence of memory addresses and control signals for a read access, said control signals include column address strobe (CAS) signals that are early withdrawn;

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(b) storing a plurality of data in a plurality of memory cells of a number of banks of extended data out dynamic random access memory (EDODRAM), and outputting a subset of said data responsive to said sequence of memory addresses and control signals, said outputting being achieved by maintaining data out independent of said CAS signals and precharging memory cells upon withdrawal of said CAS signals.

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18. The method as set forth in claim 17, wherein, said sequence of memory addresses are generated by generating common most significant bits (MSBs) of said sequence of memory addresses and non-common least significant bits (LSBs) of said sequence of memory addresses, said non-common LSBs being generated consecutively, and said common MSBs being generated while said uncommon LSBs are generated.

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19. A method for accepting, storing, and outputting data comprising:
(a) generating a sequence of memory addresses and control signals for a write access, said control signals include column address strobe (CAS) signals that are early withdrawn;

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(b) accepting and storing a plurality of data in a plurality of memory cells of a number of banks of extended data out dynamic random access memory (EDODRAM) in accordance to said sequence of memory addresses and control signals, said EDODRAM maintaining data out independent of said CAS signals and precharging memory cells upon withdrawal of said CAS signals.

20. The method as set forth in claim 19, wherein, said sequence of memory addresses are generated by generating common most significant bits (MSBs) of said sequence of memory addresses and non-common least significant bits (LSBs) of said sequence of memory addresses, said non-common LSBs being generated consecutively, and said common MSBs being generated while said uncommon LSBs are generated.

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21. A circuit board comprising:

(a) a system memory having

(a.1) address and control generation circuitry for generating a sequence of memory addresses and control signals for a read access, said control signals include column address strobe (CAS) signals that are early withdrawn,

(a.2) a number of banks of extended data out dynamic random access memory (EDODRAM) coupled to said address and control generation circuitry for storing a plurality of data in a plurality of memory cells of said EDODRAMs, and outputting a subset of said data responsive to said sequence of memory addresses and control signals, said EDODRAM maintaining data out independent of said CAS signals and precharging memory cells upon withdrawal of said CAS signals;

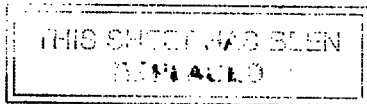
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(b) a cache memory unit for caching a subset of said data;

(c) a controller coupled to said system memory unit and said cache memory unit for providing control signals to said system and cache memory units; and

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(d) a bus coupled to said system memory unit and said cache memory unit for providing addresses to said system and cache memory units and transfer data in and out of said system and cache memory units.

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22. A circuit board comprising:

(a) a system memory having

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(a.1) address and control generation circuitry for generating a sequence of memory addresses and control signals for a write access, said control signals include column address strobe (CAS) signals that are early withdrawn,

15

(a.2) a number of banks of extended data out dynamic random access memory (EDODRAM) coupled to said address and control generation circuitry for accepting and storing a plurality of data in a plurality of memory cells of said EDODRAMs, responsive to said sequence of memory addresses and control signals, said EDODRAM maintaining data out independent of said CAS signals and precharging memory cells upon withdrawal of said CAS signals;

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(b) a cache memory unit for caching a subset of said data;

(c) a controller coupled to said system memory unit and said cache memory unit for providing control signals to said system and cache memory units; and

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(d) a bus coupled to said system memory unit and said cache memory unit for providing addresses to said system and cache memory units and transfer data in and out of said system and cache memory units.

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23. A computer system comprising:

(a) a processor for executing a plurality of instructions;

(b) a system memory having

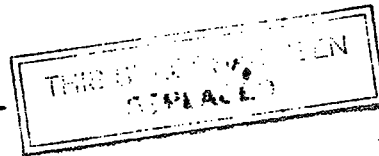
(b.1) address and control generation circuitry for generating a sequence of memory addresses and control signals for a

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5 read access, said control signals include column address
strobe (CAS) signals that are early withdrawn,
(b.2) a number of banks of extended data out dynamic
random access memory (EDODRAM) coupled to said
address and control generation circuitry for storing said
instructions and a plurality of data in a plurality of memory
cells of said EDODRAMs, and outputting a subset of said
instructions/data responsive to said sequence of memory
addresses and control signals, said EDODRAM
10 maintaining data out independent of said CAS signals and
precharging memory cells upon withdrawal of said CAS
signals; and
(c) a bus coupled to said processor and said system memory unit
for providing addresses to said system memory unit and
15 transferring instructions and data in and out of said system
memory unit.

24. A computer system comprising:
- (a) a processor for executing a plurality of instructions;
- 20 (b) a system memory having
- (a.1) address and control generation circuitry for generating
a sequence of memory addresses and control signals for a
write access, said control signals include column address
strobe (CAS) signals that are early withdrawn,
- 25 (a.2) a number of banks of extended data out dynamic
random access memory (EDODRAM) coupled to said
address and control generation circuitry for accepting and
storing a plurality of data in a plurality of memory cells of
said EDODRAMs, responsive to said sequence of memory
addresses and control signals, said EDODRAM
30 maintaining data out independent of said CAS signals and
precharging memory cells upon withdrawal of said CAS
signals; and

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(c) a bus coupled to said processor and said system memory unit for providing addresses to said system memory unit and transferring instructions and data in and out of said system memory unit.

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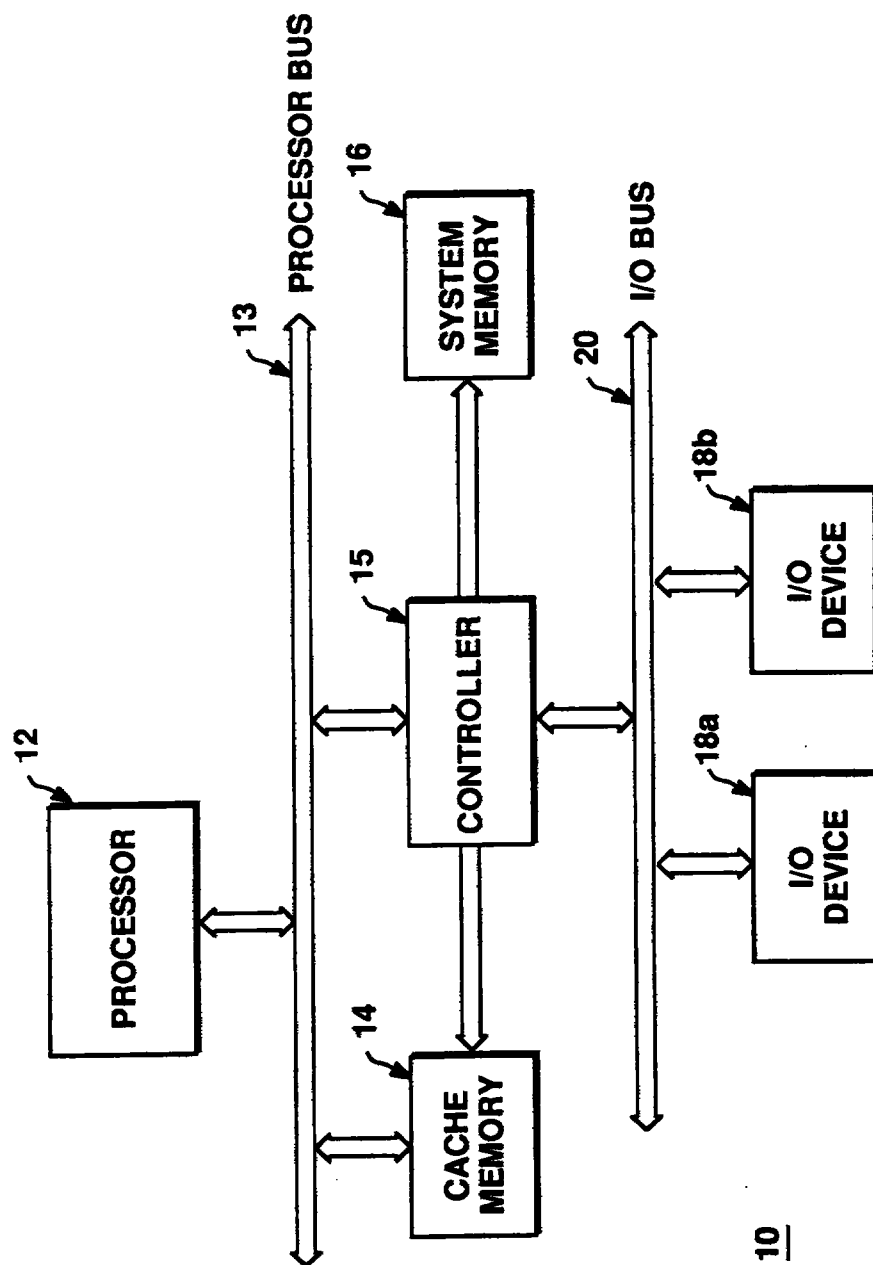


FIGURE 1

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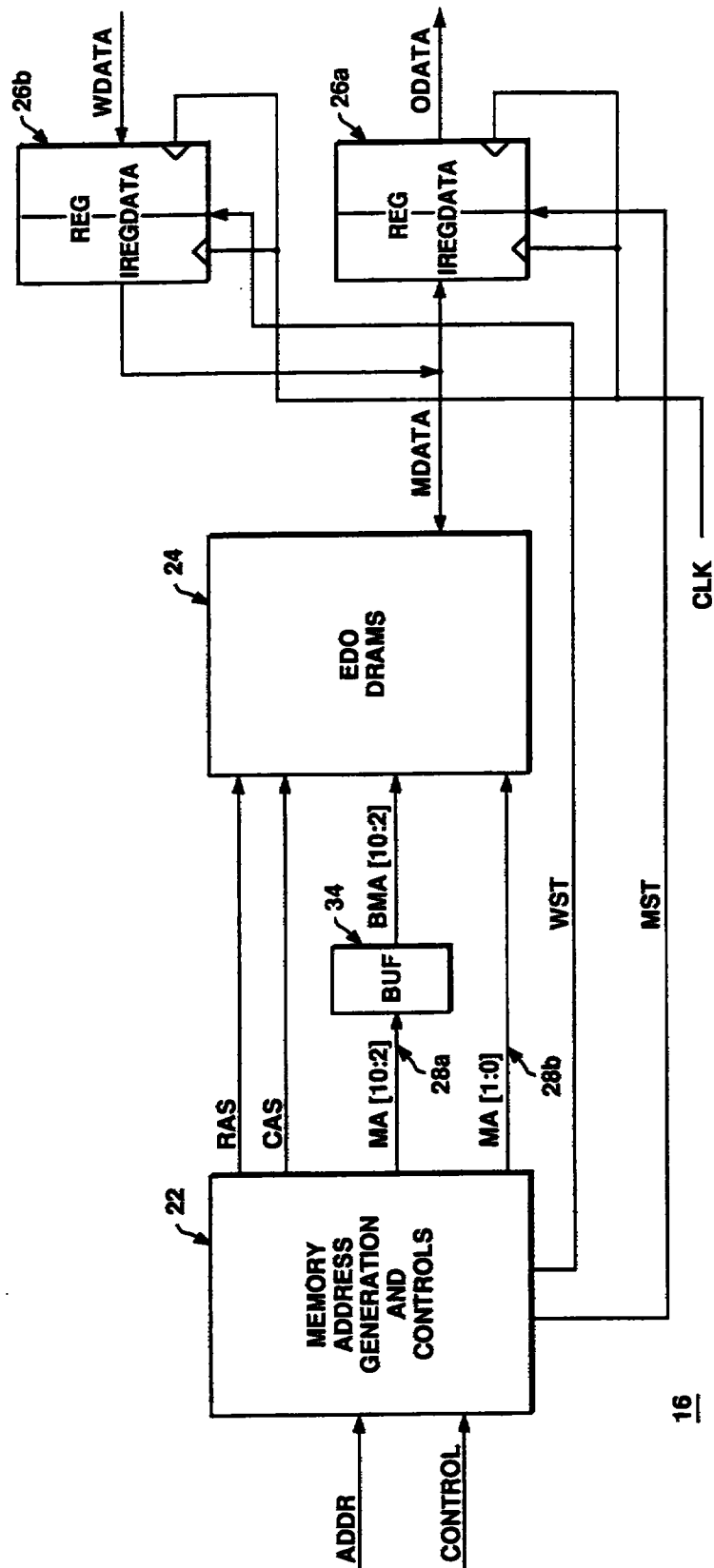


FIGURE 2

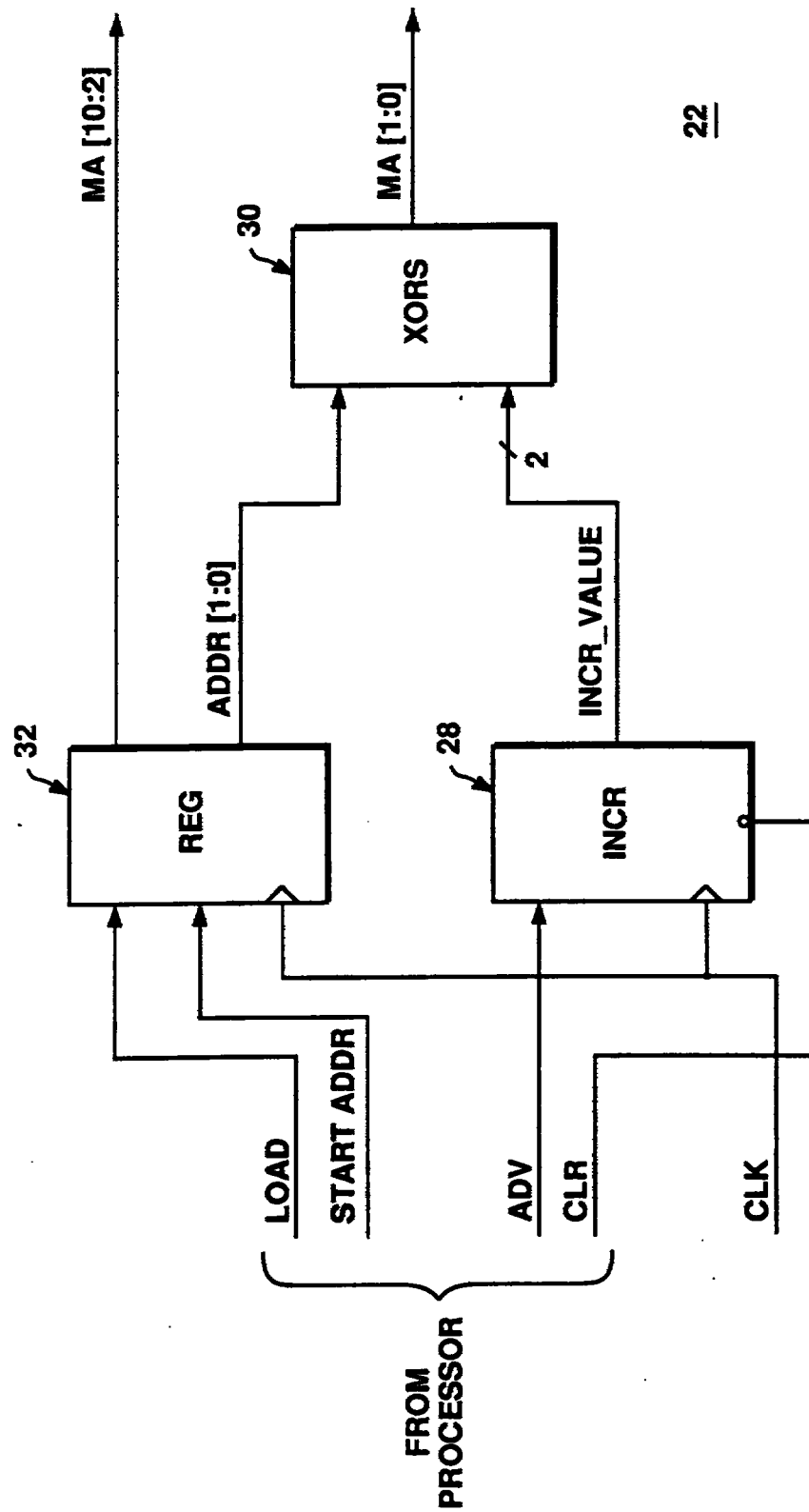


FIGURE 3

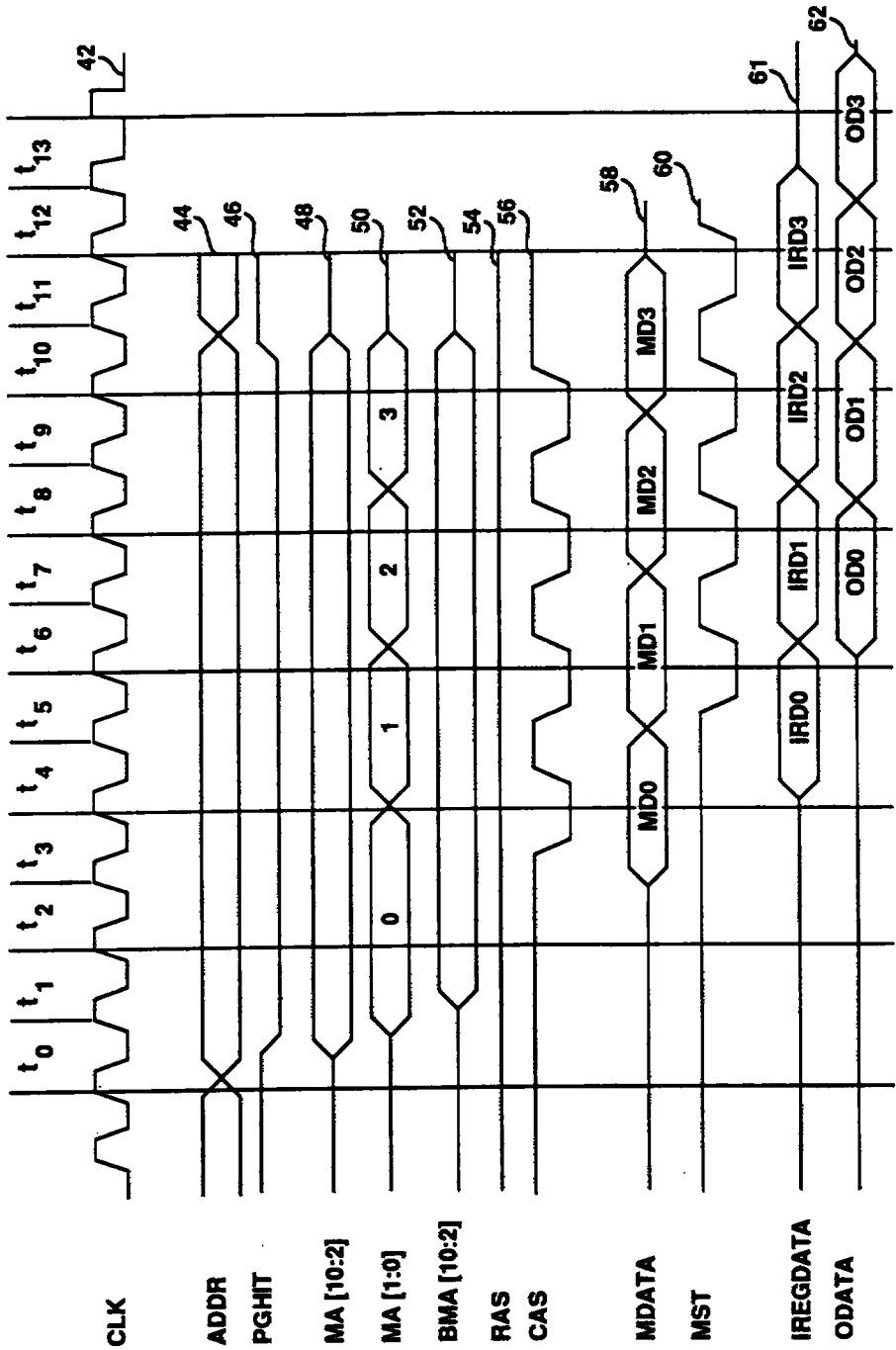


FIGURE 4a

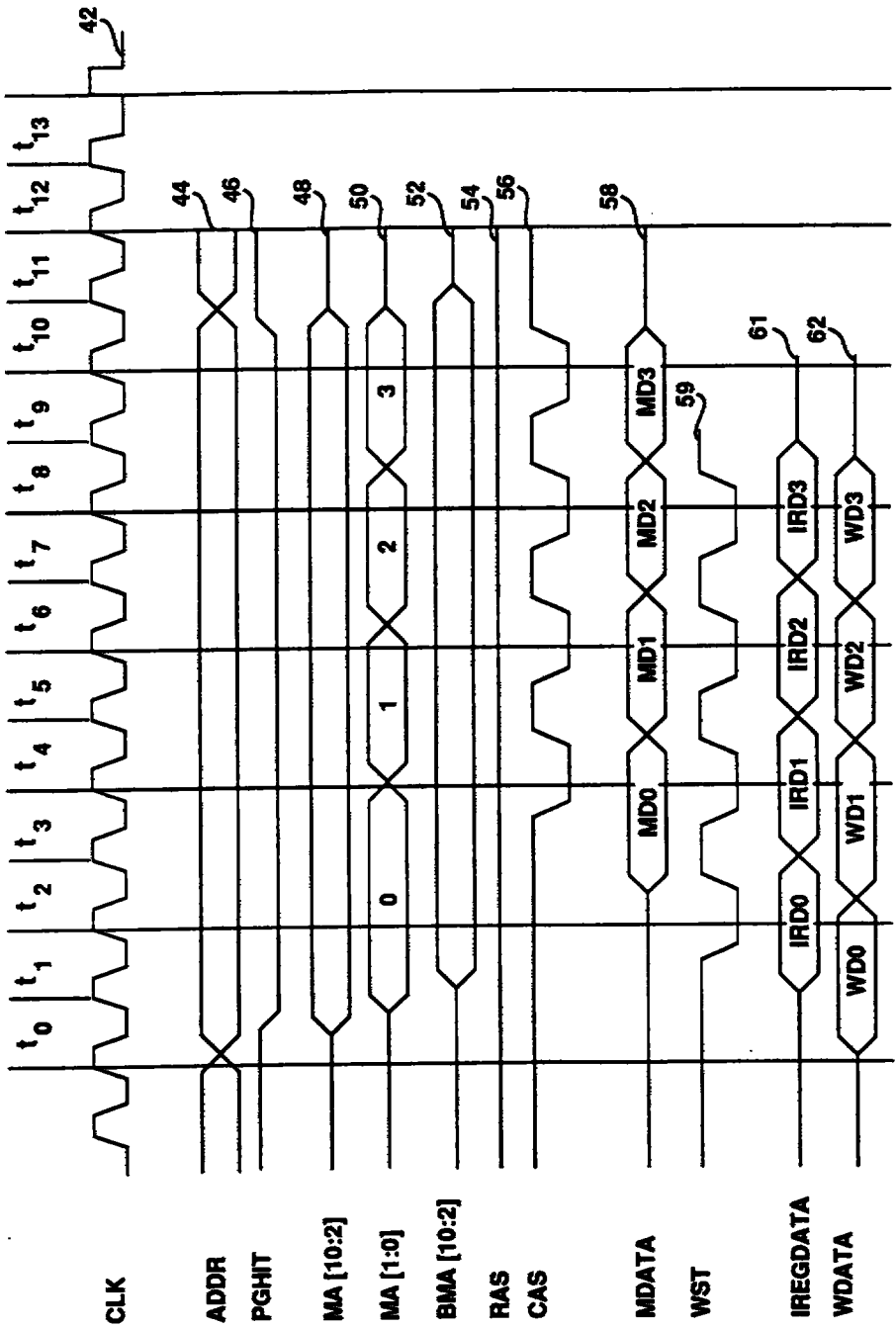


FIGURE 4b

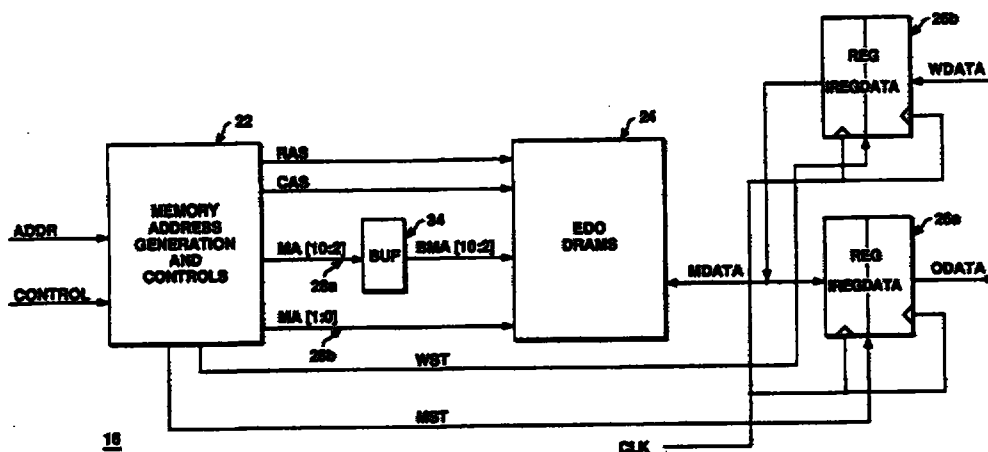


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(54) Title: **AN IMPROVED COST/PERFORMANCE SYSTEM MEMORY UNIT USING EXTENDED DATA OUT DYNAMIC RANDOM ACCESS MEMORY**



(57) Abstract

A system memory unit is provided to a computer system comprising memory address and control generation circuitry, a number of banks of extended data out dynamic random access memory (EDODRAM), and a number of registers. The memory address and control generation circuitry is used to generate memory addresses for the EDODRAMs, advantageously delivered over two address bus lines. Additionally, the memory address and control generation circuitry is used to generate control signals for the EDODRAMs and the registers, including advantageously "shortened" column address strobe (CAS) signals. The EDODRAMs are used to accept, store, and output data, in accordance to memory addresses provided. The registers are used to stage the data being streamed out of or into the EDODRAMs. As a result of the advantageous manners in which the memory addresses and the CAS signals are provided, the cycle time of a memory access is reduced, even if the slower CMOS technology based circuit elements are used to constitute the memory address and control generation circuitry, the EDODRAM, and the registers.

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