CLAIMS

1. A circuit comprising:

a memory array comprising

a plurality of bit lines;

a plurality of word lines;

a plurality of select lines, the plurality of bit lines and the plurality of select lines intersect the plurality of word lines; and

a plurality of memory cells each comprising;

a pair of transistors,

a first memory element, and

a second memory element, the first and second memory elements are connected to the plurality of word lines by way of the pair of transistors, the first and second memory elements are connected to the plurality of bit lines and the plurality of select lines,

wherein the first memory element is connected between one of the plurality of bit lines and a first shared collector emitter or source drain terminal of the pair of transistors, and the second memory element is connected between one of the plurality of select lines and a second shared collector emitter or source drain terminal of the pair of transistors.

2. The circuit of claim 1, wherein the pair of transistors are a complementary pair of bipolar junction pass transistors, the complementary pair of bipolar junction pass transistors comprises an NPN bipolar junction pass transistor and a PNP bipolar junction pass transistor.

3. The circuit of claim 1, wherein the pair of transistors are a complementary pair of junction field-effect transistors, the complementary pair of junction field-effect transistors comprises an n-channel junction field-effect transistor and a p-channel junction field effect-transistor.

4. The circuit of claim 1, wherein one transistor of the pair of transistors and a transistor of an opposite channel type in a memory cell adjacent to the one of the plurality of memory cells have a base or a gate terminal connected to a same one of the plurality of word lines.

5. The circuit of claim 1, wherein the first memory element and the second memory element are a phase-change memory, a resistive random access memory, or a magnetic random access memory.

6. The circuit of claim 1, wherein the first memory element and the second memory element have same characteristics, the first memory element and the second memory element are programmable to N states and the memory cell is programmable to $\frac{N(N+1)}{2}$ states.

7. The circuit of claim 1, wherein the first memory element and the second memory element have different characteristics, the first memory element and the second memory element are programmable to N states and the memory cell is programmable to N^2 states.

8. A circuit comprising:

a memory cell, the memory cell comprises a first memory element, a second memory element, a pair of transistors, the first memory element is connected between a bit line and a first shared collector emitter or source drain terminal of the pair of transistors, the second memory element is connected to between a select line and a second shared collector emitter or source drain terminal of the pair of transistors, the first transistor is connected to a first word line, and the second transistor is connected to a second word line.

9. The circuit of claim 8, wherein the first memory element is programmed by applying a first write voltage to the bit line, applying a second write voltage to the second word line, applying a first intermediate voltage to the select line, and applying a second intermediate voltage to the first word line.

10. The circuit of claim 9, wherein the select line is connected to a high impedance.

11. The circuit of claim 9, wherein the first write voltage is a positive supply voltage, the second write voltage is a negative supply voltage, and the first and second intermediate voltages are ground voltages.

12. The circuit of claim 9, wherein the first write voltage is greater than the first intermediate voltage, the first intermediate voltage is greater than or equal to the second intermediate voltage, and the second intermediate voltage is greater than the second write voltage.

13. The circuit of claim 8, wherein the first memory element is erased by applying a first erase voltage to the first word line, applying a second erase voltage to the bit line, applying a first intermediate voltage to the select line, and applying a second intermediate voltage to the second word line.

14. The circuit of claim 13, wherein the first erase voltage is a positive supply voltage, the second erase voltage is a negative supply voltage, and the first and second intermediate voltages are ground voltages, the first erase voltage is greater than the first intermediate voltage, the first intermediate voltage is greater than or equal to the second intermediate voltage, and the second intermediate voltage is greater than the second erase voltage.

15. The circuit of claim 8, wherein the pair of transistors are a complementary pair of bipolar junction pass transistors, the complementary pair of bipolar junction pass transistors comprises an NPN bipolar junction pass transistor and a PNP bipolar junction pass transistor.

16. The circuit of claim 8, wherein the pair of transistors are a complementary pair of junction field-effect transistors, the complementary pair of junction field-effect transistors comprises an n-type junction field-effect transistor and a p-type junction field effect-transistor.

17. The circuit of claim 8, wherein the first memory element and the second memory element are a phase-change memory, a resistive random access memory, or a magnetic random access memory.