(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
6 May 2010 (06.05.2010)

PCT

(10) International Publication Number
WO 2010/049497 A1

(51) International Patent Classification:
H01L 21/762 (2006.01)

(21) International Application Number:
PCT/EP2009/064308

(22) International Filing Date:
29 October 2009 (29.10.2009)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
08 57411 30 October 2008 (30.10.2008) FR

(71) Applicant *(for all designated States except US)*: **S.O.I.TEC SILICON ON INSULATOR TECHNOLOGIES** [FR/FR]; Chemin des Franques, Parc Technologique des Fontaines, F-38190 Bernin (FR).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **LANDRU, Didier** [FR/FR]; rue des Armariniers, F-38190 Champ Pres Froges (FR). **RADU, Ionut** [FR/FR]; 434 Avenue de la Résistance, F-38920 Crolles (FR). **VINCENT, Sébastien** [FR/FR]; 2 rue Desaix, F-38000 Grenoble (FR).

(74) Agent: **ILGART, Jean-Christophe**; Brevalex, 3, rue du Docteur Lancereaux, F-75008 Paris (FR).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: METHOD OF DETACHING SEMI-CONDUCTOR LAYERS AT LOW TEMPERATURE

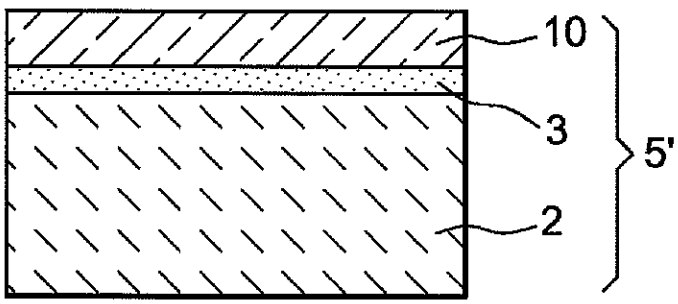


FIG. 1E

(57) Abstract: The invention relates to a method for producing UTBOX type structures comprising: a) the assembly of a substrate, known as "donor" substrate (1), with a substrate, known as "receiver" substrate (2), at least one of the two substrates comprising an insulating layer (3) of thickness less than 50 nm, b) a first heat treatment for reinforcing the assembly between the two substrates, at temperature below 400°C, carried out during the assembly and/or after assembly, to reinforce said assembly, c) a second heat treatment at temperature above 900°C, the exposure time between 400°C and 900°C being less than 1 minute or 30 seconds.

WO 2010/049497 A1