

Description

Title of Invention: NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE

Technical Field

[0001] The present invention relates to a non-volatile semiconductor memory device.

Background Art

[0002] In a conventional memory cell disclosed in Japanese Patent Laid-Open No. 2011-129816 (Patent Literature 1), a memory gate structure is disposed between two select gate structures (refer to FIG. 15 in Patent Literature 1). This memory cell includes a drain region connected with a bit line, and a source region connected with a source line. A select gate structure, a memory gate structure, and another select gate structure are disposed in this order on a well between the drain and source regions. In the memory cell thus configured, the memory gate structure includes a charge storage layer. Data is programmed by injecting charge into the charge storage layer and erased by removing the charge inside the charge storage layer.

[0003] FIG. 9 is a schematic view illustrating an exemplary circuit configuration of a conventional non-volatile semiconductor memory device 100. In this case, the non-volatile semiconductor memory device 100 includes, for example, a plurality of memory cells 102a, 102b, 102c, 102d, 102e, 102f, 102g, and 102h arranged in a matrix of rows and columns. Memory cell formation parts 101a, 101b, 101c, and 101d are provided for respective pairs of the memory cells 102a, 102b, 102c, 102d, 102e, 102f, 102g, and 102h arranged in the row direction.

[0004] In the non-volatile semiconductor memory device 100, one bit line BL1 (BL2) is shared by the memory cells 102a, 102c, 102e, and 102g (102b, 102d, 102f, and 102h), which are arranged in the column direction among the memory cells 102a, 102b, 102c, 102d, 102e, 102f, 102g, and 102h. A bit voltage is evenly applied to each of the bit lines BL1 and BL2. In the non-volatile semiconductor memory device 100, for example, the memory cell formation parts 101a, 101b, 101c, and 101d share respective memory gate lines MGL1, MGL2, MGL3, and MGL4 and respective drain side select gate lines DGL1, DGL2, DGL3, and DGL4. A predetermined voltage is applied to each of the memory gate lines MGL1, MGL2, MGL3, and MGL4 and each of the drain side select gate lines DGL1, DGL2, DGL3, and DGL4.

[0005] In the non-volatile semiconductor memory device 100, one source side select gate line SGL and one source line SL are shared by all memory cells 102a, 102b, 102c, 102d, 102e, 102f, 102g, and 102h. A predetermined source gate voltage is applied to the source side select gate line SGL, and a predetermined source voltage is applied to the source line SL.

[0006] The memory cells 102a, 102b, 102c, 102d, 102e, 102f, 102g, and 102h have identical configurations. For example, the memory cell 102a includes a memory gate electrode MG connected with a memory gate line MGL1, a drain side select gate electrode DG connected with a drain side select gate line DGL1, and a source side select gate electrode SG connected with the source side select gate line SGL. The memory cells 102a, 102b, 102c, 102d, 102e, 102f, 102g, and 102h each becomes a data programmed state when charge is injected into a charge storage layer EC by a quantum tunneling effect caused by a voltage difference between the memory gate electrode MG and a channel layer.

[0007] At a data reading operation to read, for example, data programmed to the memory cell 102a on the first row and the first column in the conventional non-volatile semiconductor memory device 100, a reading voltage of 1.5 V is applied to the bit line BL1 connected with the memory cell (hereinafter also referred to as a data reading cell) 102a from which data is to be read, whereas a non-reading voltage of 0 V is applied to the bit line BL2 connected with the memory cells 102b, 102d, 102f, and 102h from which no data is to be read.

[0008] Simultaneously, in the non-volatile semiconductor memory device 100, a voltage of 0 V is applied to the memory gate line MGL1, MGL2, MGL3, MGL4, a voltage of 1.5 V is applied to the source side select gate line SGL, and a voltage of 0 V is applied to the source line SL.

Simultaneously, in the non-volatile semiconductor memory device 100, a reading gate voltage of 1.5 V is applied to the drain side select gate line DGL1 connected with the data reading cell 102a, whereas a non-reading gate voltage of 0 V is applied to the drain side select gate lines DGL2, DGL3, and DGL4 connected with the memory cells 102c, 102d, 102e, 102f, 102g, and 102h from which no data is to be read.

[0009] Accordingly, in the data reading cell 102a, the well directly below the drain side select gate electrode DG connected with the bit line BL1 becomes a conductive state, whereas the well directly below the memory gate electrode MG is a non-conductive state when charge is stored in the charge storage layer EC (data is programmed). Accordingly, electrical connection between the source line SL and the bit line BL1 is blocked to maintain intactly the reading voltage of 1.5 V applied to the bit line BL1.

[0010] When no charge is stored in the charge storage layer EC of the data reading cell 102a (when no data is

programmed), the well directly below the memory gate electrode MG is in a conductive state, the source line SL at 0 V and the bit line BL1 at 1.5 V are electrically connected with each other through the data reading cell 102a, and the reading voltage of 1.5 V applied to the bit line BL1 decreases due to the source line SL at 0 V accordingly.

[0011] Simultaneously, in the other memory cells 102c, 102e, and 102g sharing the bit line BL1 with the data reading cell 102a, the well directly below the drain side select gate electrode DG becomes a non-conductive state due to voltage differences between the respective drain side select gate lines DGL2, DGL3, and DGL4 and the bit line BL1, and has no influence on the reading voltage of 1.5 V applied to the bit line BL1. Accordingly, the non-volatile semiconductor memory device 100 can detect whether charge is stored in the charge storage layer EC of the data reading cell 102a by detecting whether the reading voltage applied to the bit line BL1 has changed.

[0012] The following describes, for example, a planar layout of the memory cell formation part 101b among the memory cell formation parts 101a, 101b, 101c, and 101d provided in the non-volatile semiconductor memory device 100 thus configured. FIG. 10A is a schematic view illustrating an exemplary planar layout of the memory cell formation part 101b when viewed from above a semiconductor substrate. The following describes the memory cell formation part 101b in which the three memory cells 102c, 102d, and 102i are provided.

[0013] The memory cell formation part 101b includes a memory cell region ER3 in which the memory cells 102c, 102d, and 102i are disposed. A select gate contact region ER6 is disposed at one end of the memory cell region ER3, and another select gate contact region ER7 is disposed at the other end of the memory cell region ER3.

A non-select gate electrode formation region ER1 (ER5) is disposed at an end of the select gate contact region ER6 (ER7).

[0014] In this case, the memory cell formation part 101b includes the strip-shaped memory gate electrode MG extending across the non-select gate electrode formation region ER1, the select gate contact region ER6, the memory cell region ER3, the select gate contact region ER7, and the non-select gate electrode formation region ER5. A memory gate contact MGC is provided on the memory gate electrode MG in, for example, the non-select gate electrode formation regions ER1 and ER5.

[0015] The memory cell region ER3 includes a well W having a predetermined shape and disposed on a surface of the semiconductor substrate. For example, the memory gate electrode MG intersects strip-shaped memory disposition regions W1, W2, and W3 of the well W. The memory disposition regions W1, W2, and W3 are each divided into a source region WS and a drain region WD with the memory gate electrode MG interposed therebetween. In the memory cell formation part 101b, the source regions WS of the memory disposition regions W1, W2, and W3 are provided continuously with each other. A predetermined source voltage is evenly applied to each source region WS through a column-shaped source contact SC connected with the source line SL (FIG. 9).

[0016] In the memory cell formation part 101b, the drain regions WD of the memory disposition regions W1, W2, and W3 are separated from each other. Predetermined bit voltages are individually applied from the different bit lines BL1, BL2, ... to the respective drain regions WD through bit contacts BC provided to the respective drain regions WD.

[0017] In the memory cell region ER3 of the memory cell formation part 101b, a first sidewall 112 of the memory

gate electrode MG is disposed in the drain regions WD of the well W, and the drain side select gate electrode DG is disposed along this sidewall 112. A second sidewall 111 of the memory gate electrode MG is disposed in the source regions WS of the well W, and the source side select gate electrode SG is disposed along this sidewall 111. In this case, the drain side select gate electrode DG and the source side select gate electrode SG together with the memory gate electrode MG are shared by the memory cells 102c, 102d, and 102i arranged in one direction. The drain side select gate electrode DG and the source side select gate electrode SG are insulated from the memory gate electrode MG through a sidewall spacer (not illustrated) made of an insulation material.

[0018] The drain side select gate electrode DG includes a wide select gate contact formation part Ca provided with a drain side select gate contact DGC in the select gate contact region ER7. A predetermined voltage from the drain side select gate line DGL2 (FIG. 9) is applied to the drain side select gate electrode DG through the drain side select gate contact DGC and the select gate contact formation part Ca.

[0019] The source side select gate electrode SG includes a wide select gate contact formation part Cb provided with a source side select gate contact SGC in the select gate contact region ER6. A predetermined voltage from the source side select gate line SGL (FIG. 9) is applied to the source side select gate electrode SG through the source side select gate contact SGC and the select gate contact formation part Cb.

[0020] In the non-select gate electrode formation regions ER1 and ER5, no conduction layer made of, for example, a semiconductor material is disposed along the sidewalls 111 and 112 and end walls 113 of the memory gate electrode MG, providing physical disconnection structures

in which the drain side select gate electrode DG and the source side select gate electrode SG are not in contact with each other. With this configuration, in the memory cell formation part 101b, the drain side select gate electrode DG and the source side select gate electrode SG are insulated from each other through the physical disconnection structures in the non-select gate electrode formation regions ER1 and ER5. Accordingly, a predetermined voltage can be independently applied to the drain side select gate electrode DG and the source side select gate electrode SG.

Citation List

Patent Literature

[0021] Patent Literature 1: Japanese Patent Laid-Open No. 2011-129816

Summary of Invention

Technical Problem

[0022] In the conventional memory cell formation part 101b thus configured, a semiconductor layer I that should have been removed through a manufacturing process remains in the non-select gate electrode formation regions ER1 and ER5 as illustrated in FIG. 10B, in which any part corresponding to that in FIG. 10A is denoted by an identical reference sign. In this case, in the memory cell formation part 101b, the drain side select gate electrode DG and the source side select gate electrode SG are electrically connected with each other through the semiconductor layer I.

[0023] For example, at a data reading operation to read data from the memory cell 102a on the first row and the first column as illustrated in FIG. 9, when short-circuit defect occurs to the memory cell formation part 101b from which no data is to be read due to the electrical

connection between the drain side select gate electrode DG and the source side select gate electrode SG, the drain side select gate line DGL2 at 0 V and the source side select gate line SGL at 1.5 V are electrically connected with each other at the memory cell formation part 101b (illustrated with a wire L in FIG. 9).

[0024] As a result, the voltage of 0 V applied to the drain side select gate line DGL2 increases or the voltage of 1.5 V applied to the source side select gate line SGL shared by the memory cells 102a, 102b, ... decreases in the non-volatile semiconductor memory device 100, and accordingly, false reading operation potentially occurs due to voltage variation in the drain side select gate line DGL2 and the source side select gate line SGL.

[0025] In addition, in the non-volatile semiconductor memory device 100, short-circuit defect due to the electrical connection between the drain side select gate electrode DG and the source side select gate electrode SG in the memory cell formation part 101b causes leakage current between the drain side select gate line DGL2 and the source side select gate line SGL, which leads to increase in electric power consumption at a data reading operation.

[0026] The present invention is intended to solve the above-described problem by providing a non-volatile semiconductor memory device capable of reducing the occurrence of false reading operation due to voltage variation at a data reading operation as compared to conventional cases, and also capable of reducing increase in electric power consumption due to voltage variation.

Solution to Problem

[0027] To solve the above-described problem, a non-volatile semiconductor memory device according to the present invention includes at least a first memory cell

formation part extending in one direction and including a memory gate electrode extending in a longitudinal direction of the first memory cell formation part, and a second memory cell formation part extending in one direction and including a memory gate electrode extending in a longitudinal direction of the second memory cell formation part. The first memory cell formation part and the second memory cell formation part extend side by side on a semiconductor substrate at a predetermined distance from each other. The first memory cell formation part and the second memory cell formation part each includes: a first select gate structure including a first select gate electrode on a well of the semiconductor substrate through a first select gate insulating film; a second select gate structure including a second select gate electrode on the well through a second select gate insulating film; and a memory gate structure provided between the first select gate structure and the second select gate structure through sidewall spacers and including a lower gate insulating film, a charge storage layer, an upper gate insulating film, and the memory gate electrode stacked in this order on the well. A non-select gate electrode formation region is provided in which a memory gate electrode couples an end of the first memory cell formation part in the longitudinal direction and an end of the second memory cell formation part in the longitudinal direction between which the first select gate electrode and the second select gate electrode are not disposed. The first select gate electrode is provided on a first sidewall of the memory gate electrode in each of the first memory cell formation part and the second memory cell formation part, the first sidewall serving as an inner peripheral wall of a region enclosed by the first memory cell formation part, the second

memory cell formation part, and the non-select gate electrode formation regions.

Advantageous Effects of Invention

[0028] A non-volatile semiconductor memory device according to the present invention can electrically connect first select gate electrodes of the same kind, to which an identical voltage is likely to be applied at a data reading operation, even when manufacturing defect occurs. Accordingly, the non-volatile semiconductor memory device according to the present invention can reduce the occurrence of false reading operation due to voltage variation at a data reading operation as compared to a conventional case in which a first select gate electrode and a second select gate electrode of different kinds, to which different voltages are likely to be applied, are connected with each other, causing voltage variation in the entire non-volatile semiconductor memory device, and can also reduce increase in electric power consumption due to voltage variation.

Brief Description of Drawings

[0029] FIG. 1 is a schematic view illustrating a sectional configuration of a memory cell included in a non-volatile semiconductor memory device according to the present invention.

FIG. 2 is a schematic view illustrating a circuit configuration of the non-volatile semiconductor memory device according to the present invention.

FIG. 3 is a table listing voltage values of the non-volatile semiconductor memory device at various operations.

FIG. 4 is a schematic view illustrating a planar layout of the non-volatile semiconductor memory device according to the present invention.

FIG. 5 is a schematic view illustrating the planar layout of the non-volatile semiconductor memory device illustrated in FIG. 4 in which short-circuit defect occurs to a certain memory cell array unit.

FIG. 6 is a schematic view illustrating a circuit configuration of the non-volatile semiconductor memory device in which short-circuit defect occurs to a certain memory cell array unit.

FIG. 7 is a schematic view illustrating a planar layout of a non-volatile semiconductor memory device according to another embodiment.

FIG. 8 is a schematic view illustrating the planar layout of the non-volatile semiconductor memory device illustrated in FIG. 7 in which short-circuit defect occurs to a certain memory cell array unit.

FIG. 9 is a schematic view illustrating a circuit configuration of a conventional non-volatile semiconductor memory device.

FIG. 10A is a schematic view illustrating a planar layout of a conventional memory cell formation part; and FIG. 10B is a schematic view illustrating the planar layout of the memory cell formation part illustrated in FIG. 10A in which short-circuit defect occurs.

Description of Embodiments

[0030] Hereinafter, embodiments of the present invention will be described in the following order.

<1. First embodiment>

1-1. Configuration of memory cell

1-2. Circuit configuration of non-volatile semiconductor memory device according to the present invention

1-3. Voltages in non-volatile semiconductor memory device at various operations

1-4. Planar layout of non-volatile semiconductor memory device

1-5. Non-volatile semiconductor memory device to which short-circuit defect occurs

1-6. Operations and effects

<2. Non-volatile semiconductor memory device according to another embodiment>

2-1. Planar layout of non-volatile semiconductor memory device according to another embodiment

2-2. Non-volatile semiconductor memory device according to another embodiment to which short-circuit defect occurs

<3. Other embodiments>

[0031] (1) First embodiment

(1-1) Configuration of memory cell

The following first describes the configuration of each of memory cells arranged in a matrix of rows and columns in a non-volatile semiconductor memory device according to the present invention. As illustrated in FIG. 1, a memory cell 2a includes a memory gate structure 4a, a drain side select gate structure 5a, and a source side select gate structure 6a disposed on a well W made of, for example, P-type Si. The memory gate structure 4a is included in an N-type transistor structure. The drain side select gate structure 5a is included in an N-type metal-oxide-semiconductor (MOS) transistor structure. The source side select gate structure 6a is included in an N-type MOS transistor structure.

[0032] A drain region WD and a source region WS are spaced at a predetermined distance on a surface of the well W. The drain region WD is disposed at one end of the drain side select gate structure 5a, and the source region WS is disposed at one end of the source side select gate structure 6a. The drain region WD is connected with a bit line BL1, and the source region WS

is connected with a source line SL. A low concentration drain region WDa is disposed adjacent to the drain region WD on the surface of the well W. A sidewall structure SW along a sidewall of the drain side select gate structure 5a is disposed on the low concentration drain region WDa. A low concentration source region WSa is disposed adjacent to the source region WS on the surface of the well W. Another sidewall structure SW along a sidewall of the source side select gate structure 6a is disposed on the low concentration source region WSa.

[0033] The memory gate structure 4a includes a charge storage layer EC on the well W between the low concentration drain region WDa and the low concentration source region WSa through a lower gate insulating film 24a made of an insulation material such as SiO_2 . The charge storage layer EC is made of, for example, silicon nitride (Si_3N_4), silicon oxynitride (SiON), alumina (Al_2O_3), or hafnia (HfO_2). The memory gate structure 4a further includes a memory gate electrode MG on the charge storage layer EC through an upper gate insulating film 24b made of an insulation material. Accordingly, the memory gate structure 4a has a configuration in which the charge storage layer EC is insulated from the well W and the memory gate electrode MG through the lower gate insulating film 24a and the upper gate insulating film 24b.

[0034] In addition to this configuration, a cap film CP made of an insulation material is disposed on the memory gate electrode MG in the memory gate structure 4a. A silicide layer S1 on an upper surface of the drain side select gate structure 5a and a silicide layer S2 on an upper surface of the source side select gate structure 6a are disposed separately from an upper surface of the memory gate electrode MG by the thickness of the cap film CP. With this configuration, no silicide layer is

disposed on the upper surface of the memory gate electrode MG in a region of the memory cell 2a, and the memory gate electrode MG is covered by the cap film CP. [0035] In this case, the silicide layer S1 on the drain side select gate structure 5a and the silicide layer S2 on the source side select gate structure 6a can be each separated from the memory gate electrode MG by the thickness of the cap film CP. In the present embodiment, the cap film CP has a laminated structure in which an upper cap film CPb is stacked on a lower cap film CPa. The lower cap film CPa is made of an insulation material such as SiO₂. The upper cap film CPb is made of an insulation material such as SiN, which is different from the insulation material of the lower cap film CPa.

[0036] The memory gate electrode MG of the memory gate structure 4a is provided with a wall-shaped first sidewall 11 and a wall-shaped second sidewall 12 disposed facing the first sidewall 11. In the memory gate structure 4a, sidewalls of the lower gate insulating film 24a, the charge storage layer EC, the upper gate insulating film 24b, and the cap film CP are aligned with the first sidewall 11 and the second sidewall 12 of the memory gate electrode MG. The lower gate insulating film 24a, the charge storage layer EC, the upper gate insulating film 24b, and the cap film CP are disposed in a region between the first sidewall 11 and the second sidewall 12 of the memory gate electrode MG.

[0037] In the memory gate structure 4a, a sidewall spacer 28a made of an insulation material is disposed along the second sidewall 12 of the memory gate electrode MG and the sidewalls of the lower gate insulating film 24a, the charge storage layer EC, the upper gate insulating film 24b, and the cap film CP so that the memory gate structure 4a is disposed adjacent to the drain side select gate structure 5a through the sidewall spacer 28a.

The sidewall spacer 28a disposed between the memory gate structure 4a and the drain side select gate structure 5a has the thickness enough to insulate the memory gate structure 4a and the drain side select gate structure 5a from each other. The thickness of the sidewall spacer 28a between the memory gate structure 4a and the drain side select gate structure 5a is desirably set in the range of 5 nm to 40 nm inclusive with taken into account breakdown voltage of the sidewall spacer 28a and readout current between the memory gate structure 4a and the drain side select gate structure 5a.

[0038] The drain side select gate structure 5a includes a drain side select gate insulating film 30 on the well W between the sidewall spacer 28a and the drain region WD. The drain side select gate insulating film 30 is made of an insulation material and has the thickness less than or equal to 9 nm, preferably less than or equal to 3 nm. A drain side select gate electrode DG1 is disposed on the drain side select gate insulating film 30. The silicide layer S1 is disposed on an upper surface of the drain side select gate electrode DG1 as a second select gate electrode. The silicide layer S1 is connected with a drain side select gate line DGL1 as a second select gate line.

[0039] In the memory gate structure 4a, a sidewall spacer 28b made of an insulation material is disposed along the first sidewall 11 of the memory gate electrode MG and the sidewalls of the lower gate insulating film 24a, the charge storage layer EC, the upper gate insulating film 24b, and the cap film CP. The memory gate structure 4a is disposed adjacent to the source side select gate structure 6a through the sidewall spacer 28b. The sidewall spacer 28b disposed between the memory gate structure 4a and the source side select gate structure 6a has a thickness between 5 nm and 40 nm inclusive same as

the thickness of the sidewall spacer 28a, which is enough to insulate the memory gate structure 4a and the source side select gate structure 6a from each other.

[0040] The source side select gate structure 6a includes a source side select gate insulating film 33 on the well W between the sidewall spacer 28b and the source region WS. The source side select gate insulating film 33 is made of an insulation material and has the thickness less than or equal to 9 nm, preferably less than or equal to 3 nm. A source side select gate electrode SG1 is disposed on the source side select gate insulating film 33. The silicide layer S2 is disposed on an upper surface of the source side select gate electrode SG1 as a first select gate electrode. The silicide layer S2 is connected with a source side select gate line SGL as a first select gate line.

[0041] Additionally, in the present embodiment, the source side select gate electrode SG1 and the drain side select gate electrode DG1, which are disposed along the first sidewall 11 and the second sidewall 12 of the memory gate electrode MG through the sidewall spacers 28a and 28b, each has a sidewall shape in which the distance from the memory gate electrode MG increases such that the top portion of the select gate electrode slopes down toward the well W.

[0042] The source side select gate structure 6a and the drain side select gate structure 5a of the memory cell 2a are sidewall-shaped along the respective sidewalls (the first sidewall 11 and the second sidewall 12) of the memory gate structure 4a. With this configuration, the silicide layer S1 on the drain side select gate electrode DG1 and the silicide layer S2 on the source side select gate electrode SG1 are spaced from the memory gate electrode MG through the cap film CP on the memory gate electrode MG even when the source side select gate

structure 6a and the drain side select gate structure 5a are disposed close to the memory gate structure 4a. Accordingly, short circuit is prevented between the silicide layers S1 and S2 and the memory gate electrode MG.

[0043] (1-2) Circuit configuration of non-volatile semiconductor memory device according to the present invention

The following describes a circuit configuration of the non-volatile semiconductor memory device according to the present invention. As illustrated in FIG. 2, this non-volatile semiconductor memory device 1 includes, for example, a plurality of memory cells 2a, 2b, 2d, 2e, 2g, 2h, 2i, and 2j arranged in the matrix. The memory cells 2a, 2b, 2d, 2e, 2g, 2h, 2i, and 2j have configurations identical to the configuration of the memory cell 2a described with reference to FIG. 1, and each includes the memory gate electrode MG connected with a memory gate line MGL, the drain side select gate electrode DG1 (DG2, ...) connected with the drain side select gate line DGL1 (DGL2, DGL3, DGL4), and the source side select gate electrode SG1 (SG2, ...) connected with the source side select gate line SGL.

[0044] The non-volatile semiconductor memory device 1 includes memory cell formation parts 3a, 3b, 3c, and 3d for the memory cells 2a and 2b, the memory cells 2d and 2e, the memory cells 2g and 2h, and the memory cells 2i and 2j arranged in the row direction. One memory cell array unit 1a (1c) is provided for a pair of the memory cell formation parts 3a and 3b (3c and 3d) adjacent to each other. A predetermined substrate voltage is applied to each of the memory cell array units 1a and 1c through a substrate voltage line Back.

[0045] In the non-volatile semiconductor memory device 1, the single bit line BL1 (BL2) is shared by the memory

cells 2a, 2d, 2g, and 2i (2b, 2e, 2h, and 2j) arranged in the column direction among the memory cells 2a, 2b, 2d, 2e, 2g, 2h, 2i, and 2j. Predetermined bit voltages are evenly applied, through the bit lines BL1 and BL2, to the memory cells 2a, 2d, 2g, and 2i, and the memory cells 2b, 2e, 2h, and 2j, respectively, in the column direction. In addition, the drain side select gate lines DGL1, DGL2, DGL3, and DGL4 are shared by, for example, the memory cell formation parts 3a, 3b, 3c, and 3d in the non-volatile semiconductor memory device 1. Predetermined voltages are applied to the memory cell formation parts 3a, 3b, 3c, and 3d through the respective drain side select gate lines DGL1, DGL2, DGL3, and DGL4.

[0046] In the non-volatile semiconductor memory device 100, the single memory gate line MGL, the single source side select gate line SGL, and the single source line SL are shared by all memory cells 2a, 2b, 2d, 2e, 2g, 2h, 2i, and 2j. A predetermined memory gate voltage is applied to the memory gate line MGL, a predetermined source gate voltage is applied to the source side select gate line SGL, and a predetermined source voltage is applied to the source line SL.

[0047] (1-3) Voltages in non-volatile semiconductor memory device at various operations

The following describes various operations at the non-volatile semiconductor memory device 1. FIG. 3 is a table listing an exemplary voltage values at each site in the non-volatile semiconductor memory device 1 illustrated in FIG. 2 at a data programming operation ("Prog") to inject charge into the charge storage layer EC of, for example, the memory cell 2a, at a data reading operation ("Read") to detect whether charge is stored in the charge storage layer EC of the memory cell 2a, or at a data erasing operation ("Erase") to remove charge

inside the charge storage layer EC of, for example, the memory cell 2a.

[0048] The column "Prog" in FIG. 3 lists voltage values ("select column" and "select row") for injecting charge into the charge storage layer EC of the memory cell 2a, and voltage values ("non-select column" or "non-select row") for injecting no charge into the charge storage layer EC of the memory cell 2a.

[0049] For example, to inject charge into the charge storage layer EC of the memory cell 2a, a charge storage gate voltage of 12 V is applied from the memory gate line MGL to the memory gate electrode MG and a substrate voltage of 0 V is applied to the well W (denoted by "Back" in FIG. 3) as listed in the column "Prog" in FIG. 3. Simultaneously, a gate off voltage of 0 V is applied from the source side select gate line SGL to the source side select gate electrode SG1, and a source off voltage of 0 V is applied from the source line SL to the source region WS. Accordingly, the source side select gate structure 6a blocks electrical connection between the source region WS and a channel layer formation carrier region of the memory gate structure 4a, thereby preventing voltage application from the source line SL to the channel layer formation carrier region of the memory gate structure 4a.

[0050] Simultaneously, a drain side select gate voltage of 1.5 V is applied from the drain side select gate line DGL1 to the drain side select gate electrode DG1, and a charge storage bit voltage of 0 V is applied to the drain region WD from the bit line BL1. Accordingly, the drain side select gate structure 5a electrically connects the drain region WD and the channel layer formation carrier region of the memory gate structure 4a.

[0051] The electrical connection between the drain region WD and the channel layer formation carrier region of the

memory gate structure 4a induces carriers into the channel layer formation carrier region so that the carriers form a channel layer at 0 V, which is same as the charge storage bit voltage, in the surface of the well W. Accordingly, a large voltage difference of 12 V occurs between the memory gate electrode MG of the memory gate structure 4a and the channel layer, and causes a quantum tunneling effect by which charge is injected into the charge storage layer EC, thereby achieving a data programmed state.

[0052] To prevent charge injection into the charge storage layer EC of the memory cell 2a when a charge storage gate voltage necessary for injecting charge into the charge storage layer EC is applied to the memory gate electrode MG of the memory cell 2a, the source side select gate structure 6a blocks electrical connection between the source region WS and the well W of a region facing the memory gate electrode MG whereas the drain side select gate structure 5a blocks electrical connection between the drain region WD and the well W of the region facing the memory gate electrode MG.

[0053] Thus, in the memory cell 2a to which no data is programmed, a depleted layer is disposed in the channel layer formation carrier region, so that potential at the surface of the well W increases based on the charge storage gate voltage, and a voltage difference between the memory gate electrode MG and the surface of the well W decreases accordingly, thereby preventing charge injection into the charge storage layer EC.

[0054] At a data reading operation specified through the column "Read" in FIG. 3, for example, the bit line BL1 connected with the memory cell 2a, from which data is to be read, is precharged to an exemplary voltage of 1.5 V, and then a voltage of 0 V is applied to the source line SL. In this state, the potential of the bit line BL1,

which changes depending on whether current flows through the memory cell 2a, is detected to determine whether charge is stored in the charge storage layer EC of the memory cell 2a. Specifically, when charge is stored in the charge storage layer EC of the memory gate structure 4a (when data is programmed) at data reading from the memory cell 2a, the well W directly below the memory gate structure 4a is in a non-conductive state, blocking electrical connection between the drain region WD and the source region WS. As a result, the reading voltage of 1.5 V applied to the bit line BL1 connected with the drain region WD is maintained intactly in the memory cell 2a from which data is to be read.

[0055] When no charge is stored in the charge storage layer EC of the memory gate structure 4a (when no data is programmed) at data reading from the memory cell 2a, the well W directly below the memory gate structure 4a is in a conductive state, electrically connecting the drain region WD and the source region WS. As a result, the source line SL at 0 V and the bit line BL1 at 1.5 V are electrically connected with each other through the memory cell 2a. As a result, the reading voltage applied to the bit line BL1 is applied to the source line SL at 0 V in the memory cell 2a from which data is to be read, and the reading voltage of 1.5 V applied to the bit line BL1 decreases accordingly.

[0056] Accordingly, the non-volatile semiconductor memory device 1 enables execution of the data reading operation of determining whether charge is stored in the charge storage layer EC of the memory cell 2a by detecting whether the reading voltage applied to the bit line BL1 has changed. Simultaneously, a non-reading voltage of 0 V is applied to the bit line BL2 connected only with the memory cells 2b, 2e, 2h, and 2j from which no data is to be read.

[0057] At a data erasing operation to remove charge inside the charge storage layer EC of the memory cell 2a ("Erase" in FIG. 3), a memory gate voltage of -12 V is applied from the memory gate line MGL to the memory gate electrode MG so that charge inside the charge storage layer EC is removed toward the well W at 0 V, thereby erasing data.

[0058] (1-4) Planar layout of non-volatile semiconductor memory device

The following describes a planar layout of the non-volatile semiconductor memory device 1 described above. FIG. 4 is a schematic view illustrating the planar layout of the non-volatile semiconductor memory device 1 according to the present invention including the plurality of memory cell array units 1a and 1b, ... disposed on a semiconductor substrate, when viewed from above the semiconductor substrate. FIG. 4 illustrates a planar layout of the memory cell array unit 1a and part of a planar layout of the memory cell array unit 1b having a configuration identical to the configuration of the memory cell array unit 1a among the plurality of memory cell array units 1a, 1b, The memory cell array units 1a, 1b, ... all have identical configurations, and thus the following description will be made mainly on the memory cell array unit 1a.

[0059] The sectional configuration of the memory cell 2a illustrated in FIG. 1 is a sectional configuration along line A-A' in FIG. 4. Illustration of the sidewall spacers 28a and 28b disposed on the sidewalls of the memory gate structure 4a illustrated in FIG. 1, the sidewall structures SW and the silicide layers S1 and S2 disposed on the drain side select gate structure 5a and the source side select gate structure 6a, and other components is omitted in FIG. 4.

[0060] In the present embodiment, the memory cell array unit 1a includes the memory cell formation part 3a and the memory cell formation part 3b, and the non-select gate electrode formation regions ER1 and ER5 are provided at ends of this pair of the memory cell formation parts 3a and 3b in the longitudinal direction. This pair of the memory cell formation parts 3a and 3b is coupled with each other through the memory gate electrodes MG in the non-select gate electrode formation regions ER1 and ER5. In this case, in the memory cell array unit 1a, the memory cell formation part 3a extending in one direction (the row direction in FIG. 4) and the memory cell formation part 3b extending in the one direction extend side by side on the semiconductor substrate at a predetermined distance from each other.

[0061] The memory gate electrodes MG extend along the longitudinal direction of the memory cell formation parts 3a and 3b. The cap film CP is disposed to cover a top portion of each memory gate electrode MG so that the memory gate electrode MG is not externally exposed. Thus, in FIG. 4, which illustrates a planar layout when viewed from above the semiconductor substrate, the memory gate electrodes MG are not illustrated in the memory cell formation parts 3a and 3b, and the cap films CP are illustrated there.

[0062] The memory gate electrode MG in the memory cell formation part 3a extends from ends of the memory cell formation part 3a to the non-select gate electrode formation regions ER1 and ER5, bends in the non-select gate electrode formation regions ER1 and ER5, and is provided continuously with ends of the memory cell formation part 3b. Unlike the memory gate electrodes MG in the memory cell formation parts 3a and 3b, the memory gate electrodes MG in the non-select gate electrode

formation regions ER1 and ER5 are not covered by the cap film CP but externally exposed.

[0063] In the present embodiment, the memory gate electrodes MG in the memory cell array unit 1a are shaped in an endless rectangular ring when viewed from above the semiconductor substrate and are covered by the cap film CP in the memory cell formation parts 3a and 3b.

Accordingly, the memory gate electrodes MG in the non-select gate electrode formation regions ER1 and ER5 are each externally exposed in a C shape, in which the memory gate electrode MG is not covered by the cap film CP.

[0064] The memory cell formation part 3a (3b) includes the plurality of memory cells 2a, 2b, and 2c (2d, 2e, and 2f) disposed in the longitudinal direction in the memory cell region ER3. Although FIG. 2 only illustrates the memory cells 2a and 2b (2d and 2e) of the memory cell formation part 3a (3b), FIG. 4 additionally illustrates the memory cell 2c (2f) adjacent to the memory cell 2b (2e).

[0065] The memory cell formation part 3a (3b) includes, in addition to the memory cell region ER3 described above, the select gate contact region ER6 provided at one end of the memory cell region ER3, the select gate contact region ER7 provided at the other end of the memory cell region ER3, the insulating region ER2 provided at an end of the select gate contact region ER6, and the insulating region ER4 provided at an end of the select gate contact region ER7. In the present embodiment, the insulating regions ER2 and ER4 positioned at the ends of the memory cell formation part 3a (3b) in the longitudinal direction are adjacent to the non-select gate electrode formation regions ER1 and ER5 described above, respectively.

[0066] In the memory cell region ER3, the well W having a predetermined shape is disposed in a surface of the semiconductor substrate. For example, the memory cell

formation part 3a and 3b intersects strip-shaped memory disposition regions W1, W2, and W3 of the well W. The memory cell 2a (2b or 2c) including the memory gate structure 4a, the drain side select gate structure 5a, and the source side select gate structure 6a are disposed on the memory disposition region W1 (W2 or W3) in the memory cell region ER3 of the memory cell formation part 3a. Similarly to the memory cell formation part 3a, in the memory cell region ER3 of the memory cell formation part 3b, the memory cell 2d (2e or 2f) including a memory gate structure 4b, a drain side select gate structure 5b, and a source side select gate structure 6b is disposed on the memory disposition region W1 (W2 or W3). The memory cells 2b, 2c, 2d, 2e, and 2f in the memory cell region ER3 have configurations identical to the configuration of the memory cell 2a described with reference to FIG. 1, and thus description thereof will be omitted in the following.

[0067] The memory disposition regions W1, W2, and W3 of the well W are each divided into the source region WS and the drain region WD with the memory gate structure 4a (4b) interposed therebetween. The source regions WS of the memory disposition regions W1, W2, and W3 between the memory cell formation parts 3a and 3b are provided continuously with each other, sharing a column-shaped source contact SC provided at a predetermined position. The source contact SC is connected with the source line SL (FIG. 2) to evenly apply, to the source regions WS of the memory disposition regions W1, W2, and W3, a predetermined source voltage applied from the source line SL.

[0068] The drain regions WD of the memory disposition regions W1, W2, and W3 are separated from each other and individually provided with a column-shaped bit contact BC. The bit contacts BC are connected with the different bit

lines BL1, BL2, ... (FIG. 2), and receive predetermined bit voltages from the corresponding bit lines BL1, BL2, ... Accordingly, the drain regions WD in the memory cell formation part 3a receive predetermined bit voltages from the different bit lines BL1, BL2, ... through the bit contacts BC.

[0069] In the present embodiment, the first sidewall 11 of the memory gate electrode MG included in the memory gate structure 4a is disposed in the source region WS of the well W in the memory cell formation part 3a. The source side select gate structure 6a is disposed along the first sidewall 11 of the memory gate electrode MG. The second sidewall 12 of the memory gate electrode MG included in the memory gate structure 4a is disposed in the drain region WD of the well W in the memory cell formation part 3a. The drain side select gate structure 5a is disposed along the second sidewall 12 of the memory gate electrode MG.

[0070] In addition to this configuration, in the memory cell formation part 3b paired with the memory cell formation part 3a, the source side select gate structure 6b is disposed along the first sidewall 11 (inner peripheral wall) of the memory gate electrode MG on which the source side select gate structure 6a is disposed in the memory cell formation part 3a. Additionally, in the memory cell formation part 3b, the drain side select gate structure 5b is disposed along the second sidewall 12 (outer peripheral wall) of the memory gate electrode MG on which the drain side select gate structure 5a is disposed in the memory cell formation part 3a.

[0071] In the source side select gate structure 6a (6b), the sidewall-shaped source side select gate electrode SG1 (SG2) is disposed along the first sidewall 11 of the memory gate structure 4a (4b), and a wide select gate contact formation part Ca integrated with the source side

select gate electrode SG1 (SG2) is disposed in the select gate contact region ER6.

[0072] The select gate contact formation part Ca includes a plane portion 15a having a plane surface. The plane portion 15a is provided with a column-shaped source side select gate contact SGC connected with a source side select gate line (not illustrated). With this configuration, a predetermined voltage is applied from the source side select gate line SGL to the source side select gate electrode SG1 (SG2) having a tilted sidewall-shape with a small width through the source side select gate contact SGC and the select gate contact formation part Ca.

[0073] In the drain side select gate structure 5a (5b), the sidewall-shaped drain side select gate electrode DG1 (DG2) is disposed along the second sidewall 12 of the memory gate structure 4a (4b), and a wide select gate contact formation part Cb integrated with the drain side select gate electrode DG1 (DG2) is disposed in the select gate contact region ER7.

[0074] The select gate contact formation part Cb includes a plane portion 15b having a plane surface. The plane portion 15b is provided with a column-shaped drain side select gate contact DGC connected with the drain side select gate line DGL1 (DGL2). With this configuration, a predetermined voltage is applied from the drain side select gate line DGL1 (DGL2) to the drain side select gate electrode DG1 (DG2) having a tilted sidewall-shape with a small width through the drain side select gate contact DGC and the select gate contact formation part Cb.

[0075] The select gate contact formation parts Ca and Cb provided in the select gate contact regions ER6 and ER7 may each have such various shapes that the select gate contact formation part is provided continuously with the source side select gate electrode SG1 or the drain side

select gate electrode DG1, and the source side select gate contact SGC or the drain side select gate contact DGC is formed on the select gate contact formation part. [0076] The memory gate structure 4a (4b) extends from the memory cell region ER3 to the insulating regions ER2 and ER4 at ends of the select gate contact regions ER6 and ER7, but the source side select gate electrode SG1 (SG2) and the drain side select gate electrode DG1 (DG2) do not extend to the insulating regions ER2 and ER4 unlike the memory cell region ER3. Select gate electrode insulating portions 103 are disposed in place of the source side select gate electrode SG1 (SG2) and the drain side select gate electrode DG1 (DG2).

[0077] The select gate electrode insulating portions 103 each includes an i-type sidewall-shaped intrinsic semiconductor layer Ia, a sidewall-shaped opposite-conductivity-type semiconductor layer OC, and a sidewall-shaped intrinsic semiconductor layer Ib. The intrinsic semiconductor layer Ia, the opposite-conductivity-type semiconductor layer OC, and the intrinsic semiconductor layer Ib are arranged in this order along the first sidewall 11 and the second sidewall 12 of each memory gate electrode MG. The opposite-conductivity-type semiconductor layer OC has a conductivity type (in this case, p-type) different from a conductivity type of the source side select gate electrode SG1 (SG2) and the drain side select gate electrode DG1 (DG2).

[0078] In this manner, in the insulating regions ER2 and ER4, the i-type intrinsic semiconductor layer Ia, the p-type opposite-conductivity-type semiconductor layer OC, and the i-type intrinsic semiconductor layer Ib are arranged in this order along the first sidewalls 11 and the second sidewalls 12 of the memory gate electrodes MG from the n-type source side select gate electrode SG1 (SG2) and the n-type drain side select gate electrode DG1

(DG2) as starting points. With this configuration, in the memory cell array unit 1a, the memory cell formation part 3a (3b) provides a p-i-n junction along the first sidewall 11 of the memory gate electrode MG from the n-type source side select gate electrode SG1 (SG2) as a starting point, thereby electrically insulating the source side select gate electrodes SG1 and SG2 disposed along the same first sidewall 11 from each other. Similarly, the memory cell formation part 3a (3b) provides a p-i-n junction along the second sidewall 12 of the memory gate electrode MG from the n-type drain side select gate electrode DG1 (DG2) as a starting point, thereby electrically insulating the drain side select gate electrodes DG1 and DG2 disposed along the same second sidewall 12 from each other.

[0079] The cap film CP is disposed on the memory gate electrodes MG in the memory cell region ER3, the insulating regions ER2 and ER4, and the select gate contact regions ER6 and ER7 as described above. The cap film CP prevents salicidation of an upper surface of each memory gate electrode MG through a manufacturing process.

[0080] In the non-select gate electrode formation regions ER1 and ER5, however, no cap film CP is formed on the memory gate electrodes MG, and thus the memory gate electrodes MG are externally exposed so that the upper surfaces of the memory gate electrodes MG are salicided. A column-shaped memory gate contact MGC is provided through a silicide layer (not illustrated) disposed on each memory gate electrode MG. The memory gate contact MGC is connected with the memory gate line MGL (FIG. 2) to receive a predetermined voltage application from the memory gate line MGL. Accordingly, the voltage applied to the memory gate line MGL is applied to the memory gate electrode MG through the memory gate contact MGC.

[0081] In this manner, in the non-volatile semiconductor memory device 1, the memory gate electrodes MG are covered by the cap film CP in the memory cell region ER3, the select gate contact regions ER6 and ER7, and the insulating regions ER2 and ER4. A predetermined voltage is applied to the memory gate electrodes MG covered by the cap film CP in the memory cell region ER3 by applying the predetermined voltage through the memory gate contact MGC of the memory gate electrodes MG exposed in the non-select gate electrode formation regions ER1 and ER5.

[0082] The non-volatile semiconductor memory device 1 thus configured can be produced through a process of manufacturing a typical complementary MOS (CMOS) involving a deposition process, a resist applying process, an exposure and developing process, an etching process, an impurity injecting process, and a resist peeling process. Thus, the description of a method of manufacturing the non-volatile semiconductor memory device 1 is omitted below.

[0083] (1-5) Non-volatile semiconductor memory device to which short-circuit defect occurs

The following describes the non-volatile semiconductor memory device 1 to which short-circuit defect occurs due to a manufacturing defect. FIG. 5, in which any part corresponding to that in FIG. 4 is denoted by an identical reference sign, is a schematic diagram of a non-volatile semiconductor memory device 21 in which a semiconductor material of the intrinsic semiconductor layers Ia and Ib of the select gate electrode insulating portions 103 remains in the non-select gate electrode formation regions ER1 and ER5 through a manufacturing process of forming the select gate electrode insulating portions 103 in the insulating regions ER2 and ER4 by, for example, etching to manufacture the non-volatile semiconductor memory device 1 illustrated in FIG. 4.

[0084] In this case, the semiconductor material remaining in the non-select gate electrode formation regions ER1 and ER5 forms, for example, a sidewall-shaped intrinsic semiconductor layer Id along the first sidewall 11 of each memory gate electrode MG in the non-select gate electrode formation regions ER1 and ER5, and a sidewall-shaped intrinsic semiconductor layer Ie along the second sidewall 12 of the memory gate electrode MG.

[0085] Accordingly, in the memory cell formation part 3a, an intrinsic semiconductor layer Ia2, an opposite-conductivity-type semiconductor layer OCb, and the intrinsic semiconductor layer Id are formed in this order on the first sidewall 11 as an inner peripheral wall of the memory gate electrode MG in, for example, the insulating region ER2, whereas the intrinsic semiconductor layer Id is also formed on the first sidewall 11 in the non-select gate electrode formation region ER1 (ER5), extending to an opposite-conductivity-type semiconductor layer OCc in the memory cell formation part 3b. In the memory cell formation part 3b, an intrinsic semiconductor layer Ia3, the opposite-conductivity-type semiconductor layer OCc, and the intrinsic semiconductor layer Id are disposed in this order along the first sidewall 11 of the memory gate electrode MG in the insulating region ER2.

[0086] For example, when foreign objects generated through a manufacturing process adhere to the opposite-conductivity-type semiconductor layers OCb and OCc or formation defect occurs to the opposite-conductivity-type semiconductor layers OCb and OCc at manufacturing, the intrinsic semiconductor layers Ia2, Id, and Ia3 formed along the first sidewall 11 of the memory gate electrode MG are electrically connected with each other. Since the source side select gate electrode SG1 in the memory cell formation part 3a and the source side select gate

electrode SG2 in the memory cell formation part 3b are each disposed along the first sidewalls 11 of the memory gate electrodes MG in the non-volatile semiconductor memory device 21 according to the present invention, the electrical connection between the intrinsic semiconductor layers Ia2, Id, and Ia3 formed along the first sidewalls 11 of the memory gate electrodes MG leads to electrical connection between the source side select gate electrodes SG1 and SG2.

[0087] FIG. 6, in which any part corresponding to that in FIG. 2 is denoted by an identical reference sign, is a schematic view illustrating a circuit configuration of the non-volatile semiconductor memory device 21 when the source side select gate electrode SG1 in the memory cell formation part 3a and the source side select gate electrode SG2 in the memory cell formation part 3b are electrically connected with each other. As illustrated in FIG. 6, this configuration can be regarded as a configuration in which the source side select gate line SGL shared by the memory cell formation parts 3a and 3b is connected through a wire La in the memory cell formation parts 3a and 3b in the memory cell array unit 1a.

[0088] In this case, at a data reading operation to detect whether charge is stored in the charge storage layer EC of, for example, the memory cell 2a in the non-volatile semiconductor memory device 21, the same source side select gate line SGL is shared by the memory cell 2a from which data is to be read and the memory cell 2d and any other memory cell from which no data is to be read. Accordingly, no voltage variation occurs to the source side select gate line SGL at 1.5 V even when the source side select gate electrode SG1 in the memory cell formation part 3a and the source side select gate electrode SG2 in the memory cell formation part 3b are

electrically connected with each other, thereby preventing any false reading operation that otherwise occurs in conventional cases.

[0089] The following describes a case in which the semiconductor material remains along the second sidewall 12 of the memory gate electrode MG exposed in the non-select gate electrode formation region ER1 as illustrated in FIG. 5. As illustrated in FIG. 5, in the memory cell array unit 1a, the semiconductor material remaining in the non-select gate electrode formation regions ER1 and ER5 forms the sidewall-shaped intrinsic semiconductor layer Ie along the second sidewall 12 of each memory gate electrode MG in the non-select gate electrode formation regions ER1 and ER5 in some cases.

[0090] In such a case, for example, an opposite-conductivity-type semiconductor layer OCa in the insulating region ER2 of the memory cell formation part 3a, and an opposite-conductivity-type semiconductor layer OCd in the insulating region ER2 of the memory cell formation part 3b are continuous with each other through the intrinsic semiconductor layer Ie on the second sidewall 12 as an outer peripheral wall of the memory gate electrode MG.

[0091] For example, when foreign objects generated through a manufacturing process adhere to the opposite-conductivity-type semiconductor layers OCa and OCd or formation defect occurs to the opposite-conductivity-type semiconductor layers OCa and OCd at manufacturing, intrinsic semiconductor layers Ia1, Ie, and Ia4 formed along the second sidewall 12 of the memory gate electrode MG are electrically connected with each other. Since the drain side select gate electrode DG1 in the memory cell formation part 3a and the drain side select gate electrode DG2 in the memory cell formation part 3b are disposed along the continuous second sidewalls 12 of the

memory gate electrodes MG in the non-volatile semiconductor memory device 21 according to the present invention, the electrical connection between the intrinsic semiconductor layers Ia1, Ia2, and Ia4 formed along the second sidewalls 12 of the memory gate electrodes MG leads to electrical connection between the drain side select gate electrodes DG1 and DG2.

[0092] As illustrated in FIG. 6, this configuration can be regarded as a configuration in which the drain side select gate line DGL1, which is connected with the drain side select gate electrode DG1 in the memory cell formation part 3a, and the drain side select gate line DGL2, which is connected with the drain side select gate electrode DG2 in the memory cell formation part 3b, are connected with each other through a wire Lb in the non-volatile semiconductor memory device 21.

[0093] In this case, at a data reading operation to detect whether charge is stored in the charge storage layer EC of, for example, the memory cell 2a in the non-volatile semiconductor memory device 21, a voltage of 1.5 V is applied to the drain side select gate line DGL1 connected with the memory cell 2a from which data is to be read, and a voltage of 0 V is applied to the drain side select gate line DGL2 connected with the memory cell 2d and any other memory cell from which no data is to be read. Thus, the electrical connection between the drain side select gate electrode DG1 in the memory cell formation part 3a, and the drain side select gate electrode DG2 in the memory cell formation part 3b causes voltage variation in the drain side select gate lines DGL1 and DGL2, and thus causes any false reading operation that also occurs in conventional cases.

[0094] However, in the non-volatile semiconductor memory device 21 according to the present invention, since the drain side select gate lines DGL1, DGL2, DGL3, and DGL4

are individually provided for the respective memory cell formation parts 3a, 3b, 3c, and 3d, only the drain side select gate line DGL1 in the memory cell formation part 3a and the drain side select gate line DGL2 in the memory cell formation part 3b are connected with each other through the wire 1b in this case. Accordingly, in the non-volatile semiconductor memory device 21, voltage variation occurs only to the drain side select gate lines DGL1 and DGL2 connected with the memory cell formation parts 3a and 3b while voltage variation is prevented in the other drain side select gate lines DGL3 and DGL4.

[0095] Thus, even when the drain side select gate electrodes DG1 and DG2 in, for example, the memory cell formation parts 3a and 3b are connected with each other in the non-volatile semiconductor memory device 21, false reading operation due to voltage variation in the drain side select gate lines DGL1 and DGL2 occurs only in the memory cell formation parts 3a and 3b. With this configuration, even when short-circuit defect occurs between the memory cell formation parts 3a and 3b, false reading operation can be prevented in the other memory cell formation parts 3c and 3d.

[0096] When short-circuit defect occurs to the memory cell formation parts 3c and 3d from which no data is to be read and thus the drain side select gate lines DGL3 and DGL4 are connected with each other, no voltage variation occurs in the drain side select gate lines DGL3 and DGL4 since the voltage of 0 V is applied to both drain side select gate lines DGL3 and DGL4, thereby preventing any false reading operation that otherwise occurs in conventional cases.

[0097] (1-6) Operations and effects

With the above-described configuration, in the non-volatile semiconductor memory device 1, the same memory gate electrodes MG are shared by the memory cell

formation part 3a and the memory cell formation part 3b, and the memory cell formation part 3a and the memory cell formation part 3b are coupled with each other through the memory gate electrodes MG in the non-select gate electrode formation regions ER1 and ER5. The source side select gate electrode SG1 in the memory cell formation part 3a and the source side select gate electrode SG2 in the memory cell formation part 3b are provided along the first sidewalls 11 of the memory gate electrodes MG in the non-volatile semiconductor memory device 1.

[0098] With this configuration, even when a foreign object, a conduction material, or the like remains along the first sidewalls 11 of the memory gate electrodes MG due to manufacturing defect in the non-volatile semiconductor memory device 1, the source side select gate electrodes SG1 and SG2 of the same kind in the memory cell formation parts 3a and 3b to which an identical voltage is applied at a data reading operation can be electrically connected with each other.

Accordingly, voltage variation due to short-circuit defect at a data reading operation can be prevented in the source side select gate electrodes SG1 and SG2 and the drain side select gate electrodes DG1 and DG2.

[0099] Thus, the non-volatile semiconductor memory device 1 can reduce the occurrence of false reading operation due to voltage variation at a data reading operation as compared to a conventional case in which a drain side select gate electrode and a source side select gate electrode of different kinds, to which different voltage values are likely to be applied, are connected with each other when manufacturing defect occurs, causing voltage variation in the entire non-volatile semiconductor memory device, and can also reduce increase in electric power consumption due to unintended voltage variation.

[0100] In the non-volatile semiconductor memory device 1, the drain side select gate electrode DG1 in the memory cell formation part 3a and the drain side select gate electrode DG2 in the memory cell formation part 3b are provided along the second sidewalls 12 of the memory gate electrodes MG.

[0101] With this configuration, in the non-volatile semiconductor memory device 1, even when a foreign object, a conduction material, or the like remains along the second sidewalls 12 of the memory gate electrodes MG due to manufacturing defect, the drain side select gate electrodes DG1 and DG2 of the same kind, to which an identical voltage is likely to be applied at a data reading operation in the memory cell formation parts 3a and 3b, can be electrically connected with each other to reduce the occurrence of voltage variation in the drain side select gate electrode DG1 and SG2 at a data reading operation.

[0102] Since the different drain side select gate lines DGL1, DGL2, ... are connected with the respective memory cell formation parts 3a, 3b, ... in the non-volatile semiconductor memory device 1 even when different voltages are applied to the drain side select gate electrodes DG1 and DG2 to which short-circuit defect has occurred, only the drain side select gate electrode DG1 in the memory cell formation part 3a and the drain side select gate electrode DG2 in the memory cell formation part 3b are electrically connected with each other so that voltage variation occurs only in the memory cell formation parts 3a and 3b while voltage variation is prevented in any part other than the memory cell formation parts 3a and 3b.

[0103] Thus, the non-volatile semiconductor memory device 1 can reduce the occurrence of false reading operation due to voltage variation at a data reading operation as

compared to a conventional case in which a drain side select gate electrode and a source side select gate electrode of different kinds, to which different voltages are likely to be applied, are connected with each other when manufacturing defect occurs, causing voltage variation in the entire non-volatile semiconductor memory device, and can also reduce increase in electric power consumption due to unintended voltage variation.

[0104] (2) Non-volatile semiconductor memory device according to another embodiment

(2-1) Planar layout of non-volatile semiconductor memory device according to another embodiment

In the non-volatile semiconductor memory device 1 according to the above-described embodiment, the memory gate electrodes MG are shaped in an endless rectangular ring when viewed from above the semiconductor substrate, and the two memory cell formation parts 3a and 3b are provided in the one memory cell array unit 1a, but the present invention is not limited thereto. As illustrated in FIG. 7, in which any part corresponding to that in FIG. 4 is denoted by an identical reference sign, the present invention is applicable to a non-volatile semiconductor memory device 41 in which memory gate electrodes MG1 are shaped in endless ladder when viewed from above the semiconductor substrate, and three or more memory cell formation parts 3b, 3a, 3e, ... are provided in one memory cell array unit 41a.

[0105] In this case, in the memory cell array unit 41a, the plurality of memory cell formation parts 3b, 3a, 3e, ... extend side by side on a semiconductor substrate at a predetermined distance from each other, sharing the same memory gate electrodes MG1. The memory gate electrodes MG1 in the non-select gate electrode formation regions ER1 and ER5 extend in a direction in which the memory cell formation parts 3b, 3a, 3e, ... are arranged,

and are provided continuously with ends of the memory cell formation parts 3b, 3a, 3e,

[0106] In the present embodiment, as illustrated in FIG. 7, for example, the first sidewall 11 of the memory gate electrode MG1 in the memory cell formation part 3a on the second row is disposed in the source region WS of the well W between the memory cell formation part 3a on the second row and the memory cell formation part 3b on the third row, and the source side select gate electrode SG1 is disposed along this first sidewall 11. The second sidewall 12 of the memory gate electrode MG1 in this memory cell formation part 3a is disposed in the drain region WD of the well W between the memory cell formation part 3a and the memory cell formation part 3e on the first row, and the drain side select gate electrode DG1 is disposed along this second sidewall 12.

[0107] The first sidewall 11 of the memory gate electrode MG1 in the memory cell formation part 3a on the second row extends to the memory cell formation part 3b on the third row adjacent to the memory cell formation part 3a, serving as the first sidewall 11 of the memory gate electrode MG1 in the memory cell formation part 3b on the third row. In this manner, the first sidewalls 11 of the memory gate electrodes MG1 are disposed round through the memory cell formation parts 3a and 3b adjacent to each other, without a gap. In the memory cell formation part 3b on the third row, the source region WS is disposed in the well W on the first sidewall 11 side of the memory gate electrode MG1, and the source side select gate electrode SG2 is provided along this first sidewall 11.

[0108] Accordingly, in the memory cell formation part 3b on the third row, the source side select gate electrode SG2 is disposed along the first sidewall 11 of the memory gate electrode MG1 on which the source side select gate electrode SG1 is disposed in the memory cell formation

part 3a on the second row. In the memory cell formation part 3b on the third row, the drain region WD is disposed in the well W on the second sidewall 12 side of the memory gate electrode MG1, and the drain side select gate electrode DG2 is disposed along the second sidewall 12.

[0109] The memory cell formation part 3b on the third row is disposed at one end of the memory cell array unit 41a as illustrated in FIG. 7, and thus the second sidewall 12 of the memory gate electrode MG1 serves as an outer peripheral wall of the memory cell array unit 41a. The second sidewall 12 extends to a memory cell formation part (not illustrated) disposed at the other end of the memory cell array unit 41a through the non-select gate electrode formation regions ER1 and ER5. In the memory cell formation part at the other end of the memory cell array unit 41a, a drain side select gate electrode is disposed along the second sidewall 12 of the memory gate electrode MG1, similarly to the memory cell formation part 3b on the third row.

[0110] The second sidewalls 12 of the memory gate electrodes MG1 are disposed round through the memory cell formation part 3a on the second row and the memory cell formation part 3e on the first row adjacent to the memory cell formation part 3a, and are shared by the memory cell formation parts 3a and 3e adjacent to each other. In this case, in the memory cell formation part 3e on the first row, the drain region WD is disposed in the well W on the second sidewall 12 side of the memory gate electrode MG1, and a drain side select gate electrode DG3 is provided along this second sidewall 12.

[0111] Accordingly, in the memory cell formation part 3e on the first row, the drain side select gate electrode DG3 is disposed along the second sidewall 12 of the memory gate electrode MG1 on which the drain side select gate electrode DG1 is disposed in the memory cell

formation part 3a on the second row. In the memory cell formation part 3e on the first row, the source region WS is disposed in the well W on the first sidewall 11 side of the memory gate electrode MG1, and a source side select gate electrode SG3 is formed along the first sidewall 11.

[0112] In the non-volatile semiconductor memory device 41, a voltage value at each site at a data programming operation (Prog), a data reading operation (Read), or a data erasing operation (Erase) is same as that in "(1-3) Voltages in non-volatile semiconductor memory device at various operations" described above, and thus description thereof is omitted in the following.

[0113] (2-2) Non-volatile semiconductor memory device according to another embodiment to which short-circuit defect occurs

The following describes the non-volatile semiconductor memory device 41 to which short-circuit defect occurs due to a manufacturing defect. FIG. 8, in which any part corresponding to that in FIG. 7 is denoted by an identical reference sign, is a schematic diagram of a non-volatile semiconductor memory device 51 in which the semiconductor material of the select gate electrode insulating portions 103 remains in the non-select gate electrode formation regions ER1 and ER5 through a manufacturing process of forming the select gate electrode insulating portions 103 in the insulating regions ER2 and ER4 by, for example, etching to manufacture the non-volatile semiconductor memory device 41 illustrated in FIG. 7.

[0114] In this case, the semiconductor material remaining in the non-select gate electrode formation regions ER1 and ER5 forms the sidewall-shaped intrinsic semiconductor layer Id along the first sidewalls 11 of the memory gate electrodes MG in the non-select gate electrode formation

regions ER1 and ER5, and forms sidewall-shaped intrinsic semiconductor layers Ia and Ib along the second sidewalls 12 of the memory gate electrodes MG.

[0115] For example, in the memory cell formation part 3a on the second row, the intrinsic semiconductor layer Ia2, the opposite-conductivity-type semiconductor layer OCb, and the intrinsic semiconductor layer Id are formed in this order on the first sidewall 11 of the memory gate electrode MG in the insulating region ER2, whereas the intrinsic semiconductor layer Id is also formed in the non-select gate electrode formation region ER1 (ER5).

With this configuration, the memory cell formation part 3a is continuous, through the intrinsic semiconductor layer Id, with the opposite-conductivity-type semiconductor layer OCc in the memory cell formation part 3b on the third row sharing the first sidewall 11 of the memory gate electrode MG1 with the memory cell formation part 3a.

[0116] For example, when foreign objects generated through a manufacturing process adhere to the opposite-conductivity-type semiconductor layers OCb and OCc or formation defect occurs to the opposite-conductivity-type semiconductor layers OCb and OCc at manufacturing, the intrinsic semiconductor layers Ia2, Id, and Ia3 disposed along the first sidewalls 11 of the memory gate electrodes MG1 are electrically connected with each other. Since the source side select gate electrode SG1 in the memory cell formation part 3a on the second row and the source side select gate electrode SG2 in the memory cell formation part 3b on the third row are disposed along the continuous first sidewalls 11 of the memory gate electrodes MG1 in the non-volatile semiconductor memory device 51 according to the present invention, the electrical connection between the intrinsic semiconductor layers Ia2, Id, and Ia3 disposed along the first

sidewalls 11 of the memory gate electrodes MG1 leads to electrical connection between the source side select gate electrodes SG1 and SG2.

[0117] Similarly to the above-described embodiment, this configuration can be regarded as a configuration in which the source side select gate line SGL connected with the source side select gate electrode SG1 in the memory cell formation part 3a and the source side select gate line SGL connected with the source side select gate electrode SG2 in the memory cell formation part 3b are connected with each other through the wire La (FIG. 6) in the non-volatile semiconductor memory device 51.

[0118] In this case, at a data reading operation to detect whether charge is stored in the charge storage layer EC of, for example, the memory cell 2a provided in the memory cell formation part 3a on the second row in the non-volatile semiconductor memory device 51, the same source side select gate line SGL is shared by the memory cell 2a from which data is to be read and the memory cell 2d and any other memory cell from which no data is to be read. Accordingly, no voltage variation occurs to the source side select gate line SGL at 1.5 V even when the source side select gate electrode SG1 in the memory cell formation part 3a on the second row and the source side select gate electrode SG2 in the memory cell formation part 3b on the third row are electrically connected with each other, thereby preventing any false reading operation that otherwise occurs in conventional cases.

[0119] The following describes a case in which, as illustrated in FIG. 8, a semiconductor material remains along the second sidewalls 12 of the memory gate electrodes MG1 in the non-select gate electrode formation regions ER1 and ER5 between the memory cell formation part 3e on the first row and the memory cell formation part 3a on the second row. As illustrated in FIG. 8, the

semiconductor material remaining in the non-select gate electrode formation regions ER1 and ER5 between the memory cell formation parts 3a and 3e forms a sidewall-shaped intrinsic semiconductor layer If along the second sidewalls 12 of the memory gate electrodes MG in some cases.

[0120] In this case, for example, an opposite-conductivity-type semiconductor layer OCa in the insulating region ER2 of the memory cell formation part 3a on the second row, and an opposite-conductivity-type semiconductor layer OCe in the insulating region ER2 of the memory cell formation part 3e on the first row are continuous with each other through the intrinsic semiconductor layer If along the second sidewalls 12 of the memory gate electrodes MG between the memory cell formation parts 3a and 3e.

[0121] For example, when foreign objects generated through a manufacturing process adhere to the opposite-conductivity-type semiconductor layers OCa and OCe or formation defect occurs to the opposite-conductivity-type semiconductor layers OCa and OCe at manufacturing, the intrinsic semiconductor layers Ia1, If, and Ia4 formed along the second sidewalls 12 of the memory gate electrodes MG are electrically connected with each other.

[0122] Since the drain side select gate electrode DG1 in the memory cell formation part 3a on the second row and the drain side select gate electrode DG3 in the memory cell formation part 3e on the first row are disposed along the continuous second sidewalls 12 of the memory gate electrodes MG1 in the non-volatile semiconductor memory device 51 according to the present invention, the electrical connection between the intrinsic semiconductor layers Ia1, If, and Ia4 disposed along the second sidewalls 12 of the memory gate electrodes MG1 leads to

electrical connection between the drain side select gate electrodes DG1 and DG3.

[0123] In this case, at a data reading operation to detect whether charge is stored in the charge storage layer of, for example, the memory cell 2a disposed in the memory cell formation part 3a on the second row in the non-volatile semiconductor memory device 51, a voltage of 1.5 V is applied to the drain side select gate electrode DG1 in the memory cell formation part 3a from which data is to be read, and a voltage of 0 V is applied to the drain side select gate electrode DG3 connected with the memory cell formation part 3e from which no data is to be read. Thus, in the non-volatile semiconductor memory device 51, the electrical connection between the drain side select gate electrode DG1 in the memory cell formation part 3a on the second row and the drain side select gate electrode DG3 in the memory cell formation part 3e on the first row causes voltage variation in the drain side select gate electrodes DG1 and DG3, and thus causes any false reading operation that also occurs in conventional cases.

[0124] However, in the non-volatile semiconductor memory device 51 according to the present invention, since drain side select gate lines are individually provided for the respective memory cell formation parts 3b, 3a, 3e, ..., only a drain side select gate line connected with the memory cell formation part 3a on the second row and a drain side select gate line connected with the memory cell formation part 3e on the first row are connected with each other in this case. Accordingly, in the non-volatile semiconductor memory device 51, similarly to the above-described embodiment, voltage variation occurs only to the drain side select gate lines connected with the memory cell formation parts 3a and 3e while voltage

variation is prevented in a drain side select gate line connected with the memory cell formation part 3b.

[0125] Similarly to the above-described embodiment, with the above-described configuration, the non-volatile semiconductor memory device 41 can reduce the occurrence of false reading operation due to voltage variation at a data reading operation as compared to a conventional case in which a drain side select gate electrode and a source side select gate electrode of different kinds, to which different voltages are likely to be applied, are connected with each other when manufacturing defect occurs, causing voltage variation in the entire non-volatile semiconductor memory device, and can also reduce increase in electric power consumption due to unintended voltage variation.

[0126] (3) Other embodiments

The present invention is not limited to the present embodiments, but various kinds of modifications are possible without departing from the scope of the present invention. For example, various voltage values may be applied to each site. In the above-described embodiments, the first select gate electrode disposed on the first sidewall of a memory gate electrode is the source side select gate electrode SG1 and SG2, but the present invention is not limited thereto. A drain side select gate electrode may be disposed as the first select gate electrode on the first sidewall of a memory gate electrode. In this case, the second select gate electrode disposed on the second sidewall of the memory gate electrode is a source side select gate electrode.

[0127] In the above-described embodiment, the select gate electrode insulating portions 103 formed by p-i-n junctions are provided from the drain side select gate electrode DG1 and the source side select gate electrode SG1 as starting points, but the present invention is not

limited thereto. Select gate electrode insulating portions each forming any one of an n-i-n junction structure, a p-i-p junction structure, an n-p-n junction structure, and a p-n-p junction structure may be provided from the drain side select gate electrode DG1 and the source side select gate electrode SG1 as starting points. Specifically, an opposite-conductivity-type semiconductor layer of a conductivity type different from a conductivity type of the first select gate electrode and second select gate electrode, or an intrinsic semiconductor layer is desirably provided on the sidewalls of the memory gate electrode between a first select gate electrode in a memory cell formation part and a first select gate electrode in another memory cell formation part.

[0128] In the above-described embodiment, the insulating region ER2 (ER4) is disposed at an end of the select gate contact region ER6 (ER7), but the present invention is not limited thereto. Only the non-select gate electrode formation region ER1 (ER5) may be disposed at the end of the select gate contact region ER6 (ER7) without the insulating region ER2 (ER4) being interposed therebetween.

[0129] A select gate electrode insulating portion formed by any one of a p-i-n junction, an n-i-n junction structure, a p-i-p junction structure, an n-p-n junction structure, and a p-n-p junction structure may be provided in the non-select gate electrode formation regions ER1 and ER5 whether or not the insulating regions ER2 and ER4 are provided. In other words, an opposite-conductivity-type semiconductor layer of a conductivity type different from a conductivity type of the first select gate electrode and second select gate electrode, or an intrinsic semiconductor layer is desirably provided on the sidewalls of the memory gate electrode in the non-select gate electrode formation regions ER1 and ER5.

[0130] In the above-described embodiment, when viewed from above the semiconductor substrate, the memory gate electrodes MG (FIG. 4) are shaped in an endless rectangular ring, and the memory gate electrodes MG1 (FIG. 7) are shaped in an endless ladder, but the present invention is not limited thereto. Memory gate electrodes having various shapes are applicable as long as a source side select gate electrode (or drain side select gate electrode) in each memory cell formation part can be provided as a first select gate electrode on first sidewalls of memory gate electrodes shared by the memory cell formation parts.

[0131] In the above-described embodiments, the P-type well W is used to provide the memory gate structure 4a included in an N-type transistor structure, the drain side select gate structure 5a included in an N-type MOS transistor structure, and the source side select gate structure 6a included in an N-type MOS transistor structure, but the present invention is not limited thereto. An N-type well may be used to provide a memory gate structure included in a P-type transistor structure, a drain side select gate structure included in a P-type MOS transistor structure, and a source side select gate structure included in a P-type MOS transistor structure. In this case, the polarity of N-type or P-type is inverted in the memory cell 2a described in the above-described embodiments, and thus, for example, voltages applied to a memory gate structure, a drain side select gate structure, a source side select gate structure, a bit line, and a source line change accordingly.

[0132] In the above-described embodiments, for example, in the memory cell 2a, data is programmed by injecting charge into the charge storage layer EC and data is erased by removing charge in the charge storage layer EC, but the present invention is not limited thereto.

Contrary to the above configuration, data may be programmed by removing charge in the charge storage layer EC of the memory cell 2a, and data may be erased by injecting charge into the charge storage layer EC.

[0133] In the above-described embodiments, a cap film disposed on the top portion of the memory gate electrode MG and MG1 is the cap film CP having a laminated structure in which the upper cap layer CPb made of an insulation material, such as SiN, different from the insulation material of the lower cap film CPa is stacked on the lower cap film CPa, but the present invention is not limited thereto. The cap film may be a single-layer cap film or a cap film having a laminated structure including three or more layers.

Reference Signs List

[0134] 1, 21, 31, 41 non-volatile semiconductor memory device

2a, 2b, 2c, 2d, 2e, 2f, 2g, 2h, 2i, 2j memory cell

3a, 3b, 3c, 3d, 3e memory cell formation part

4a, 4b, 4c memory gate structure

5a, 5b, 5c drain side select gate structure (second select gate structure)

6a, 6b, 6c source side select gate structure (first select gate structure)

11 first sidewall

12 second sidewall

CP cap film

ER1, ER5 non-select gate electrode formation region

MG, MG1 memory gate electrode

DG1, DG2, DG3 drain side select gate electrode (second select gate electrode)

SG1, SG2, SG3 source side select gate electrode (first select gate electrode)

Claims

1. A non-volatile semiconductor memory device comprising:

- at least a first memory cell formation part extending in one direction and including a memory gate electrode extending in a longitudinal direction of the first memory cell formation part; and

- a second memory cell formation part extending in one direction and including a memory gate electrode extending in a longitudinal direction of the second memory cell formation part, wherein

- the first memory cell formation part and the second memory cell formation part extend side by side on a semiconductor substrate at a predetermined distance from each other,

- the first memory cell formation part and the second memory cell formation part each includes:

- a first select gate structure including a first select gate electrode on a well of the semiconductor substrate through a first select gate insulating film;

- a second select gate structure including a second select gate electrode on the well through a second select gate insulating film; and

- a memory gate structure provided between the first select gate structure and the second select gate structure through sidewall spacers and including a lower gate insulating film, a charge storage layer, an upper gate insulating film, and the memory gate electrode stacked in this order on the well,

- a non-select gate electrode formation region is provided in which a memory gate electrode couples an end of the first memory cell formation part in the longitudinal direction and an end of the second memory cell formation part in the longitudinal direction between

which the first select gate electrode and the second select gate electrode are not disposed, and

the first select gate electrode is provided on a first sidewall of the memory gate electrode in each of the first memory cell formation part and the second memory cell formation part, the first sidewall serving as an inner peripheral wall of a region enclosed by the first memory cell formation part, the second memory cell formation part, and the non-select gate electrode formation regions.

2. The non-volatile semiconductor memory device according to claim 1, wherein

the first select gate structure is a source side select gate structure disposed on the well between the memory gate structure and a source region of the well,

the second select gate structure is a drain side select gate structure disposed on the well between the memory gate structure and a drain region of the well, and

a source side select gate electrode is provided along the first sidewall of the memory gate electrode.

3. The non-volatile semiconductor memory device according to claim 1, wherein

the first select gate structure is a drain side select gate structure disposed on the well between the memory gate structure and a drain region of the well,

the second select gate structure is a source side select gate structure disposed on the well between the memory gate structure and a source region of the well, and

a drain side select gate electrode is provided along the first sidewall of the memory gate electrode.

4. The non-volatile semiconductor memory device according to claim 3, wherein
the drain side select gate electrode is connected with a drain side select gate line, and
the drain side select gate line is provided for each memory cell formation part.
5. The non-volatile semiconductor memory device according to any one of claims 1 to 4, wherein a select gate electrode insulating portion formed by any one of a p-i-n junction structure, an n-i-n junction structure, a p-i-p junction structure, an n-p-n junction structure, and a p-n-p junction structure is provided between the first select gate electrode in the first memory cell formation part and the first select gate electrode in the second memory cell formation part.
6. The non-volatile semiconductor memory device according to any one of claims 1 to 5, wherein
a cap film is provided on the memory gate electrodes in the first memory cell formation part and the second memory cell formation part,
no cap film is formed on the memory gate electrode in the non-select gate electrode formation region, and a memory gate contact is provided on the memory gate electrode.