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"Semiconductor integrated circuit device with power consumption reducing arrangement".

The present invention relates to a semiconductor integrated circuit device, and particularly to a technique that can be effectively adapted to, for instance, CMOS (complementary MOS)-type or bipolar-type static RAMs (random access memories).

It has been known to employ bipolar transistors for reading/writing circuits and digit line select circuits, in order to increase the operation speed of CMOS static RAMs. For example, such an arrangement has been disclosed in Japanese Patent Publication No. 58193/81.

In such a semiconductor memory device, since an operation (bias) current is supplied at all times to the bipolar transistor, the current consumed becomes a very large value. Therefore, there arises a serious defect directed in that it is impractical to have a battery back-up operation, even though a great merit of a CMOS static RAM is the fact that such a battery back-up operation is generally available. In the reading circuit, furthermore, a bipolar transistor is used as a column switching circuit, and a current is supplied to a memory cell that is selected via the column switching circuit to obtain a reading signal. However, the value of reading current cannot be increased since it is determined by the conductance of MOSFET in the memory cell. This is because, although the element size must be increased to increase the reading current, it is not allowed to increase the element size of the memory cells

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from the standpoint of increasing the memory capacity. Therefore, despite the fact that the bipolar transistors are employed, the reading speed of the above-mentioned conventional semiconductor memory device cannot be so
5 increased. Further, since the column switching circuit is constituted by the bipolar transistors, it becomes difficult to set the level (select/non-select levels) of output signals of the column address decoder circuit.

An object of the present invention is to
10 provide a semiconductor integrated circuit device which accomplishes a high operation speed while preventing the generation of ineffective current.

Another object of the present invention is to provide a CMOS static-type RAM which accomplishes a high
15 operation speed without impairing the advantage of low power consumption of the CMOS circuit.

A further object of the present invention is to provide a bipolar RAM which helps greatly reduce the consumption of electric power.

20 According to a first aspect of the present invention there is provided a semiconductor integrated circuit device including:

(a) a differential circuit having first and second bipolar transistors which receive at respective
25 bases thereof input signals and generate at respective collectors thereof output signals in response to the input

signals, emitters of said first and second bipolar transistors being coupled to each other to form a common emitter;

(b) a first MOSFET that serves as a current source to
5 supply an operating current to said differential circuit, said first MOSFET having a source-drain path coupled to said common emitter to form said operating current for said differential circuit; and

(c) means for generating a first control signal for
10 application to a gate of said first MOSFET so that said bipolar transistors generate said output signals only during a period when said first MOSFET is rendered conductive by said first control signal.

According to a second aspect of the present invention
15 there is provided a semiconductor memory device including:

(a) a memory array having a plurality of word lines, a plurality of data lines and a plurality of memory cells coupled to said plurality of said word and data lines so that each memory cell is coupled to a word line and at least
20 one data line, said memory array further having means for providing a pair of signals in response to data stored in a selected one of said plurality of memory cells;

(b) a read circuit coupled to receive said pair of signals of said memory array, said read circuit including a
25 pair of bipolar transistors coupled to form a differential circuit and a MOSFET to provide operating current to said differential circuit, said pair of bipolar transistors having bases coupled to receive said pair of signals and a

common emitter coupled to said MOSFET, said MOSFET having a source-drain path coupled to said common emitter to form said operating current for said differential circuit; and

5 (c) control means for providing a control signal to operate said MOSFET, which is coupled to a gate of said MOSFET, so that said control means provides said control signal for said MOSFET to provide said operating current for said differential circuit to which said MOSFET is coupled,
10 wherein said control signal is provided by said control means to read data stored in said one of said plurality of memory cells.

According to a third aspect of the present invention there is provided a semiconductor memory device including:

15 (a) a plurality of memory arrays each of which includes a plurality of word lines, a plurality of data lines and a plurality of memory cells coupled to said plurality of said word and data lines so that each memory cell is coupled to a word line and at least one data line,
20 each of said plurality of memory arrays including means for providing a pair of output signals in response to information stored in a selected one of said plurality of memory cells

(b) a plurality of read circuits each of which is

coupled to receive said pair of output signals of the
respective memory array, said plurality of read circuits
including a pair of bipolar transistors to form a
differential circuit and a MOSFET to provide operating
5 current to said differential circuit, each said pair of
bipolar transistors having bases coupled to received said
pair of output signals of the corresponding memory array
and a common emitter coupled to said MOSFET, the respective
MOSFET having a source-drain path coupled to the common
10 emitter of the corresponding pair of bipolar transistors;
and

(c) control means coupled to each of said MOSFET
to provide a control signal to a gate of said MOSFET of the
respective read circuit, said control means including means
15 for providing said control signal to said MOSFET of the
respective read circuit to which said control means is
coupled and further including means for selecting one of
said MOSFETs to provide operating current to the correspond-
ing differential circuit to which said one of said MOSFETs
20 is coupled so that a selected one of said read circuits is
operated to read information stored in said one of said
plurality of memory cells.

The present invention will now be described in
greater detail by way of example with reference to the
25 accompanying drawings, wherein:-

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Figure 1 is a circuit diagram of a first embodiment wherein the present invention is adapted to a CMOS static-type RAM;

Figure 2 is a circuit diagram of a reading
5 circuit in the embodiment of Figure 1;

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Figure 3 is a timing chart for illustrating the operation of Figure 2;

Figure 4 is a circuit diagram of another embodiment wherein the present invention is adapted
5 to a bipolar-type RAM; and

Figure 5 is a block diagram showing a further power consumption reducing arrangement in accordance with the present invention.

Figure 1 shows a circuit diagram of a first
10 embodiment in which the present invention is adapted to a CMOS static-type RAM. Though there is no particular limitation, the RAM of the same drawing is formed on a semiconductor substrate such as a single silicon crystal in accordance with well-known
15 techniques for producing bipolar (Bi) and CMOS (complementary MOS) integrated circuits (ICs).
Terminals A_x , A_y , D_{in} , D_{out} , $\overline{WE}$ and $\overline{CS}$ serve as external terminals. Incidentally, power terminals are omitted in the

drawing. Though there is no particular limitation, the CMOS static-type RAM of this embodiment has a memory capacity of about 64 kilobits. In order to reduce the stray capacitance that resides in a common data line that will be mentioned later, the memory array is divided into four blocks.

The circuit of memory cell MC is shown representatively. The memory cell consists of memory (drive) MOSFETs Q1 and Q2 of which the gates and drains are coupled in a crossing manner (in a latched form), and high resistances R1 and R2 formed by polycrystalline silicon layers for holding the data, that are provided between the drains of the MOSFETs Q1, Q2 and a power-source voltage V_{DD} . Transfer gate MOSFETs Q3 and Q4 are provided between the commonly connected points of MOSFETs Q1, Q2 and the complementary data lines (or digit lines) D0, $\overline{D0}$. Other memory cells MC have also been constructed in the same manner as above. These memory cells MC are arranged in the form of a matrix to constitute a memory array M-ARY0 that is representatively shown in Fig. 1. Namely, gates of the transfer gate MOSFETs Q3, Q4 of memory cells arranged in the same row are commonly connected to their corresponding word lines W1 and W2, and input/output terminals of memory cells arranged in the same column are connected to their corresponding pairs of complementary data lines D0, $\overline{D0}$ and D1, $\overline{D1}$.

In order to reduce the power consumption of the memory cells MC, the resistor R1 has a resistance which is as high as that necessary for the gate voltage of the MOSFET Q2 to be maintained higher than a threshold voltage thereof when the MOSFET Q1 is rendered nonconductive. Similarly, the resistor R2 also has a high resistance.

In other words, the resistor R1 has the ability to supply an electric current to such a degree that the data or electric charge stored in the gate capacity (not shown) of MOSFET Q2 is not discharged by a drain leakage current of MOSFET Q1.

5. According to this embodiment, the memory cell MC is constituted by n-channel MOSFETs and polycrystalline silicon resistance elements as described above, though the memory array is produced by the CMOS-IC technique. This helps reduce the sizes of memory cells and memory array compared with when p-channel MOSFETs are used instead of the polycrystalline silicon resistance elements. That is, the polycrystalline silicon resistors can be formed as a unitary structure together with the gate electrodes of driving MOSFETs Q1, Q2, and their sizes can be reduced, too. Unlike the case of using p-channel MOSFETs, furthermore, large spacing distances are not required from the driving MOSFETs Q1, Q2 and, hence, useless blank portions are not formed.

In the figure, the word line W1 is selected by a driving circuit DV1 which receives a select signal formed by an X-address decoder X-DCR. The same also holds true for the other word line W2.

20 The X-address decoder X-DCR is constituted by NOR gate circuits G1, G2 and so on that resemble one another. The inputs of these NOR gate circuits G1, G2 and so on receive internal complementary address signals in predetermined combinations, the internal complementary address signals being produced by the X-address buffer X-ADB that receives external address signals A_x supplied from a suitable circuit that is not shown.

Though there is no particular limitation, the pairs of data lines D_0 , $\overline{D_0}$ and D_1 , $\overline{D_1}$ in the memory array M-ARY0 are connected to common data lines CD_0 , $\overline{CD_0}$ via column switching circuits constituted by transfer gate MOSFETs Q9, Q10, Q11 and Q12 for select data lines. To the common data lines CD_0 , $\overline{CD_0}$, there are connected input terminals of a reading circuit R and output terminals of a writing circuit W. Common data lines of other memory arrays M-ARY0 to M-ARY3 that are not shown, have also been connected to their corresponding input terminals of the reading circuit R and to their corresponding output terminals of the writing circuit W. The output terminal of the reading circuit R sends a read signal to the data output terminal D_{out} , and a write data signal is applied from the data input terminal D_{in} to the input terminal of the writing circuit W.

Select signals Y1, Y2 are supplied from a Y-address decoder Y-DCR to the gates of MOSFETs Q9, Q10, Q11 and Q12 that constitute the above-mentioned column switching circuits. The Y-address decoder Y-DCR are constituted by NOR gate circuits G3, G4 and so on that resemble one another. To the input terminals of these NOR gate circuits G3, G4 are applied internal complementary address signals in predetermined combinations, the internal complementary address signals being produced by the Y-address buffer Y-ADB that receives external address signals A_y from a suitable circuit that is not shown.

A control circuit CON produces an internal control timing signal upon receipt of control signals from the external terminals WE , CS .

Though there is no particular limitation in this embodiment, an internal chip select signal $\overline{CS}$ of the non-select condition which is formed by the control circuit CON and which has the high level when the chip has not been selected is applied to the input terminals of the NOR gate circuits G1, G2 and so on constituting the X-address decoder X-DCR, so that all of the word lines are placed under the non-selected condition. This prevents a direct current from flowing through a load MOSFET Q5 of the data line, the transfer gate MOSFET Q3 of a memory cell MC connected to any word line that has been selected, and a memory MOSFET Q1 that has been rendered conductive, when the chip has not been selected.

Figure 2 is a circuit diagram of the reading circuit according to the embodiment of the present invention.

In this embodiment, use is made of bipolar transistors T1, T2 of a differential form as a sense amplifier SA0 which amplifies a read signal from the memory array M-ARY0. That is, the read voltages of a memory cell appearing on the common data lines CD0, $\overline{CD0}$ are supplied to bases of the differential transistors T1, T2. An n-channel MOSFET Q13 which receives an operation timing signal ϕ_{pa0} is connected to common emitters of the differential transistors T1, T2. Another memory array M-ARY3 which is representatively shown is also equipped with a sense amplifier SA3 that consists of similar differential transistors T3, T4, and an n-channel MOSFET Q14. The corresponding collectors of the differential transistors T1, T2, T3 and T4 and so on are commonly connected to a pair of input terminals of the main amplifier MA that will be described later.

Operation timing signals ϕ_{pa0} , ϕ_{pa3} supplied to the gates of MOSFETs Q13, Q14 connected to common emitters of the differential transistors, are formed by NOR gate circuits G5, G6 that receive a read control signal $WE + \overline{CS}$ which level is rendered to low level (logical "0") when the chip is selected and is placed under the read condition. Gates G5 and G6 also receive complementary address signals $\underline{axi}$, $\underline{ayi}$ that select the memory arrays M-ARY0 to M-ARY3. Therefore, only a MOSFET which forms an operation current for a sense amplifier SA corresponding to a memory array that is selected to effect the reading operation, is turned on, and MOSFETs of the remaining three sense amplifiers SA are turned off.

Collectors of the differential transistors T1, T2, T3 and T4 constituting the common sense amplifiers SA0 to SA3 are connected to emitters of the base-grounded amplifier transistors T5, T6 which constitute a circuit of the initial stage of a main amplifier MA. Bases of these transistors T5, T6 are served with a bias voltage formed by the next bias circuit. Namely, serially connected diodes D1, D2 for shifting the level of the power-source voltage V_{DD} , and an n-channel MOSFET Q16 for flowing a bias current, are connected in series between the power-source voltage V_{DD} and a point of ground potential. Further, an n-channel MOSFET Q23 is connected in parallel with the diode D1, and, though not specifically limited, the gate of the MOSFET Q23 is served with a read control signal $WE + \overline{CS}$ which assumes the low level during the reading operation. N-channel MOSFETs Q15, Q17 are connected to the emitters of the transistors T5, T6 to form bias currents therefor. The gates of these MOSFETs Q15, Q17 are served with a control signal $\overline{WE} \cdot CS$ which assumes the

high level during the reading operation. Therefore, the MOSFETs Q15 to Q17 are turned on only during the reading operation to form bias currents, respectively.

P-channel MOSFETs Q20, Q21 and n-channel MOSFETs Q22, Q24 are connected in parallel, as load means between the power-source voltage V_{DD} and the collectors of the transistors T5, T6. The p-channel MOSFETs Q20, Q21 are rendered conductive at all times since their gates are always served with ground potential of the circuit, and the gates of the n-channel MOSFETs Q22, Q24 are served with the read control signal $WE + \overline{CS}$.

Collector outputs of these transistors T5, T6 are transmitted to a data output buffer DOB via emitter-follower transistors T7, T8. The emitters of the transistors T7, T8 are connected to n-channel MOSFETs Q18, Q19 that form operation currents therefor, and are served with the read control signal $WE \cdot CS$.

Operation of the circuit of this embodiment will be described below with reference to a timing chart of Fig. 3.

In the reading operation, a write enable signal $\overline{WE}$ is set to the high level, and a chip select signal $\overline{CS}$ is set to the low level. Therefore, a read control signal $WE \cdot CS$ becomes the high level, and an inverted signal $WE + \overline{CS}$ thereof becomes the low level (not shown). Accordingly, if the address signals axi , ayi supplied at this time assume the low level, the NOR gate circuit G5 is opened to produce an output signal ϕ_{pa0} of the high level which renders the MOSFET Q13 conductive. An operation current flows into the differential transistors T1, T2, and the read signal from the memory array M-ARY0 is amplified and is produced through the collectors.

On the other hand, since the control signal $\overline{WE} \cdot CS$ of the main amplifier MA becomes the high level, MOSFETs Q15 to Q19 constituting the current sources are rendered conductive to flow operation currents into the transistors T5 to T8. Therefore, the output signals of the sense amplifier SA0 are supplied to a data output buffer DOB which is not shown, and a read output signal D_{out} is obtained from the external terminal.

With regard to sense amplifiers SA1 to SA3 of other memory arrays M-ARY1 to M-ARY3, the operation timing signals ϕ_{pa1} to ϕ_{pa3} become the low level, and MOSFETs Q14 and the like that form operation currents, are rendered nonconductive. Therefore, the sense amplifiers SA1 to SA3 establish the condition of high output impedance. Hence, the main amplifier MA is served with only the electric current produced by the selected memory array M-ARY0.

In the writing operation, the write enable signal $\overline{WE}$ is set to the low level as indicated by a broken line in Fig. 3, so that the control signal $\overline{WE} \cdot CS$ becomes the low level and its inverted signal $\overline{WE} + \overline{CS}$ becomes the high level. Therefore, MOSFETs Q13 to Q19 for forming operation currents for the amplifier transistors of the sense amplifiers SA0 to SA3 and of the main amplifier MA, are all rendered nonconductive to inhibit their operation. In this case, depending upon the conductive condition of MOSFET Q23, the bias voltage of the circuit of the initial stage of the main amplifier MA becomes nearly equal to $V_{DD} - V_f$ (V_f denotes a forward voltage of the diode D2). Further, n-channel MOSFETs Q22 and Q24 that serve as load means are turned on to raise the base potential of the emitter-follower transistors T7, T8, and p-channel MOSFETs (not

shown) that constitute a circuit in the input stage of the data output buffer circuit DOB are rendered nonconductive.

5 Fig. 4 is a circuit diagram of a second embodiment in which the present invention is adapted to a bipolar-type RAM. The RAM of the figure is formed on a semiconductor substrate such as a single silicon crystal by a technique for manufacturing semiconductor integrated circuits similar to that used in Fig. 1. Terminals XA0 to XAk, YA0 to YAl, D_{out}, D_{in}, CS, WE, -V_{ee} and GND serve as
10 external terminals. The figure, however, does not show power-source terminals -V_{ee} and GND. Unlike the circuit of the embodiment of Fig. 1, furthermore, transistors are denoted by Q, and MOSFETs are denoted by M.

15 Among a plurality of memory cells constituting a memory array M-ARY, a circuit of only one memory cell is shown in the figure. Though there is no particular limitation, in one memory cell, use is made of a flip-flop circuit which consists of drive npn-type transistors Q12, Q13 of which the bases and collectors are coupled in a crossing manner, and pnp-type transistors Q14, Q15
20 that are connected to their collectors. Though there is no particular limitation, the drive npn-type transistors Q12, Q13 are of the multi-emitter construction. The emitters on one side are commonly connected together, and the emitters of the other side serve as input/output terminals of a memory cell and are connected to a pair
25 of complementary data lines D0, $\overline{D0}$ that are representatively shown. The drive npn-type transistors Q12, Q13 may be constituted by two transistors of which the bases and collectors are commonly connected

together. Further, the load transistors Q14, Q15 may be replaced by load resistors and clamping diodes that are connected in parallel with each other. The common emitters of the load transistors Q14, Q15 are connected to a word line W0 which is shown representatively.

5 With the above-mentioned memory cell as a center, similar memory cells (represented by a black box) of a number of m are arranged along the laterally running row and are connected to the word line W0. The laterally stretching row is provided with a holding current line ST0 which corresponds to the word line W0, and the
10 commonly connected emitters of one side of drive transistors Q12, Q13 of the memory cell are connected thereto. Memory cells are also connected in the same manner as above with respect to another representatively shown row (word line Wn, holding current line STn). The holding current lines ST0, STn are provided with constant-current
15 sources Ist (not shown) that supply holding currents to the memory cells.

 Further, the similarly constructed memory cells are arranged in a number of n along the vertical column, and input/output terminals thereof are commonly connected to the complementary data lines D0, $\overline{D0}$.
20 Thus, memory cells are arranged in a number of m x n along the rows and columns to constitute a memory array M-ARY.

 The word lines W0, Wn which are representatively shown are selected or not selected by word line drive transistors Q16, Q17 that receive address decoded signals X0, Xn which are produced by the
25 X-address decoder X-DCR.

 Address signals supplied from a suitable circuit not shown are inputted to the address buffers XAB0 to XABk via external

terminals XA0 to XAk. These address buffers XAB0 to XABk form noninverted address signals and inverted address signals depending upon the input address signals, and send them to the X-address decoder X-DCR. Then, the X-address decoder X-DCR forms a word line select signal to select a word line.

In this embodiment, the complementary data lines D0, $\overline{D0}$ representatively shown are connected, via transistors Q18, Q20 that serve as column switches, to n-channel MOSFETs M1 and M3 that are also provided commonly for other complementary data lines not shown, and that are turned on by an internal chip select signal CS to form a read/write current I_r . An address decoded signal Y0 produced by the Y-address decoder Y-DCR is applied to the bases of the transistors Q18 and Q20 that work as column switches. Namely, address signals supplied from a suitable circuit not shown are inputted to the address buffers YAB0 to YAB ℓ via external terminals YA0 to YA ℓ . The address buffers YAB0 to YAB ℓ produce noninverted address signals and inverted address signals according to the input address signals and send them to the Y-address decoder Y-DCR. Therefore, the Y-address decoder Y-DCR forms a data line select signal to select a pair of complementary data lines. According to this embodiment, though there is no particular limitation, a bias circuit is subsequently provided to apply a predetermined bias voltage to data lines that have not been selected. That is, a diode D3 and a resistor R6 are connected in series between the base and the collector of a transistor Q21 of which the collector is served with earth potential of the circuit. The diode D3 and resistor R6 connected in series are connected, via a transistor Q19, to an n-channel MOSFET M2 that

produces a current I_r like the one mentioned above. Though there is no particular limitation, the transistor Q21 is of the multi-emitter construction, and is connected to the complementary data lines D_0 , $\overline{D_0}$.

A source of a very small constant current is coupled to the complementary data lines D_0 , $\overline{D_0}$. Namely, a very small constant current is absorbed at all times by transistors Q23, (Q24) which receive a constant voltage b_1 through the bases thereof and which have resistors connected to the emitters thereof.

Therefore, the data line which is not selected is biased by a voltage which is nearly equal to the sum of a forward voltage of the diode D3 and a voltage across the base and emitter of the transistor Q21. When the complementary data lines D_0 , $\overline{D_0}$ are selected, the current I_r produced by the MOSFET M2 that is rendered conductive flows into the resistor R6 via the transistor Q19. Therefore, the transistor Q21 is rendered nonconductive, and potentials of the complementary data lines D_0 , $\overline{D_0}$ are determined with the stored data in the selected memory cell.

Emitters of current switching transistors Q7, Q6 are coupled to the complementary data lines D_0 , $\overline{D_0}$ in order to write/read the data relative to a memory cell of a row that is shown representatively. Collector outputs of these transistors Q7, Q6 are sent to the input terminals of the main amplifier MA which effects the amplification operation and forms an output signal that meets the input level of a data output buffer DOB constituted by ECL (emitter coupled logic). The data output buffer DOB produces a read output signal that will be sent through the external terminal D_{out} . The main amplifier MA is constructed similarly to the main amplifier of the embodiment of Fig. 1.

Output voltages V1, V2 of a writing circuit WA are applied to the bases of the current switching transistors Q7, Q6. The writing circuit WA which forms the output voltages V1, V2 is constituted by differential transistors Q1 to Q3, a constant-current source provided to the common emitters thereof, resistors R1, R2 provided to the collectors of the transistors Q1, Q2, and a resistor R3 provided between earth potential and a point where the resistors R1, R2 and the collector of the transistor Q3 are commonly connected together. Bases of the transistors Q1, Q2 are served with write data signals d_{in} , $\bar{d}_{in}$ sent from a data input buffer DIB that will be described later, and base of the transistor Q3 is served with an internal write enable signal $\overline{we}$ sent from a control circuit CONT that will be described later.

According to this embodiment, though there is no particular limitation, the data input buffer DIB is constructed as described below, so that noise will not generate in the output voltages V1, V2 of the writing circuit WA according to the change of levels of the input data signals d_{in} , $\bar{d}_{in}$ during the writing operation. Namely, a transistor Q8 receives a write data signal supplied through the external terminal D_{in} , and a transistor Q9 is impressed with a reference voltage Vb2 through the base thereof to discriminate the input signal, and these transistors Q8 and Q9 are connected together in a differential manner. Resistors R4 and R5 are connected to the collectors of these differential transistors Q8 and Q9. Collector outputs of the differential transistors Q8 and Q9 are applied to bases of emitter-follower transistors Q25, Q26, and data signals d_{in} and $\bar{d}_{in}$ are sent from the emitters of these transistors Q25 and Q26 to the writing circuit WA. The collector of a differential transistor Q10 is connected to the common emitters of the

differential transistors Q8 and Q9, so that the data signals d_{in} and $\bar{d}_{in}$ will not change depending upon the signals from the external terminal D_{in} during the reading operation. A reference voltage Vb3 is applied to the base of the transistor Q10 to discriminate the internal write enable signal $\overline{we}$. The internal write enable signal $\overline{we}$ is applied to the base of the transistor Q11 which is connected in a differential manner relative to the transistor Q10. The collector of the transistor Q11 is connected to the collectors of the differential transistors Q8 and Q9 via diodes D1 and D2.

According to this embodiment, although there is no particular limitation, the operation currents I1 to I4 for the transistors Q1 to Q5 and for the transistors Q8, Q11, Q25 and Q26 are formed by n-channel MOSFETs M4 to M9 that are rendered conductive by an internal chip select signal cs, in order to reduce the ineffective current when the chip is not being selected.

The control circuit CONT which receives control signals supplied via the external terminals $\overline{WE}$ and $\overline{CS}$, produces an operation control signal for the data output buffer DOB, the internal write enable signal $\overline{we}$ that will be supplied to the writing circuit WA and to the data input buffer DIB, and the internal chip select signal cs. Internal circuitry for forming these signals can be constructed utilizing well-established principles for making such control circuitry.

When the control signal $\overline{CS}$ is set to the low level in order to select the chip, the control circuit CONT produces an internal chip select signal cs of the high level. On the other hand, when the control signal $\overline{CS}$ is set to the high level to place the chip under the

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nonselected condition, the control circuit CONT produces an internal chip select signal cs of the low level.

5 The reading operation is performed when the terminal $\overline{WE}$ is set to the high level and the terminal $\overline{CS}$ is set to the low level. In the data input buffer DIB in this case, the write enable signal $\overline{we}$ assumes the high level since the terminal $\overline{WE}$ assumes the high level. Therefore, the transistor Q10 is rendered nonconductive, the transistor Q11 is rendered conductive, and the electric current I4 flows being divided into one-half into the resistors R4 and R5 via diodes D1, D2. 10 Therefore, irrespective of the signals from the external terminal D_{in} , the output level is fixed to the intermediate level, and noise caused by the change of level at the external terminal D_{in} is prevented from appearing in the read reference voltages V1, V2 (V_{refc}) in the reading operation.

15 According to this embodiment, the read/write current I_r for the memory array M-ARY, and operation current for the writing circuit WA that is representatively shown, are produced by the MOSFETs which are operated by the internal chip select signal cs. Therefore, the ineffective current is prevented from flowing wastefully 20 when the chip is not selected. Current-source circuits for producing operation currents for the peripheral circuits, i.e., for the address decoders X-DCR, Y-DCR, are also constituted by the same MOSFETs that will be rendered conductive upon receipt of the internal chip select signal cs, in order to reduce the ineffective current. When 25 the MOSFETs for producing operation currents for the address decoders X-DCR, Y-DCR are rendered nonconductive under the condition where the chip is not selected, the output signals thereof take a non-select level.

According to this embodiment, the MOSFETs for producing operation currents for the transistors are turned on or off responsive to a chip select signal depending upon whether the chip is selected or not selected, thereby to reduce the current from wastefully flowing under the condition in which the chip is not selected. Furthermore, as shown in Figure 5, provision may be made of a circuit 100 for detecting the change of address signals, and a circuit 200 which, responsive to the detection outputs thereof, produces timing signals to time-serially operate the address buffer, address decoder, memory array M-ARY, reading circuit and writing circuit in the order mentioned, so that each of the circuit blocks is time-serially operated only at required timings by the operating timing signals, under the condition where the chip is selected. In this case, the consumption of current can be reduced even under the condition where the chip is selected. With regard to such an arrangement, it is noted that construction of the circuit 100 for detecting the change of address signals is well known, and its details are not described here. Similarly,

construction of a timing signal generator 200 to produce time-serial timing signals can be done according to well-known design principles for making timer circuitry. For instance, the timing
5 signal generator 200 is comprised in combination of CMOS static inverters for producing delay signals and CMOS static gate circuits for producing the timing signals.

In the two above described embodiments,
10 when the operation currents of the bipolar transistors are to be formed, the MOSFETs are operated in the saturated region. Therefore, the MOSFETs produce a nearly constant operation current for the bipolar transistors.

15 In the first embodiment, furthermore, when the address buffer ADB and the address decoder DCR are constituted by MOSFETS and bipolar transistors in order to increase the operation speed (e.g., when

a required logic circuit is constituted by the MOSFETs, and a driver circuit constituted by bipolar transistors is provided to receive the output signal of the logic circuit, so that the subsequent stage can be driven at a high speed), operation currents for the bipolar transistors are produced by the MOSFETs, and these MOSFETs are further controlled in the same manner as mentioned earlier, such that the RAM consumes reduced amounts of electric power while still featuring an increased operation speed. In this case, furthermore, provision may be made of a circuit for detecting the change of address signals like the aforementioned circuit 100 for detecting the change of address signals, as well as a timing signal-forming circuit like the aforementioned circuit 200 for forming timing signals, in order to time-serially operate the address buffer, decoder, sense amplifier, writing circuit and the reading circuit in the order mentioned only at required timings, in the same manner as mentioned earlier. This makes it possible to reduce the consumption of electric power even under the condition where the chip is selected. Preferably, the time-series outputs of the circuit 200 are coupled to the MOSFETs of the various peripheral circuits (i.e., address buffers, decoders, etc.) to provide the time-series operation by controlling the turn-on and turn-off time of the MOSFETs which serve as current sources for the bipolar transistor.

By virtue of the construction set forth above, the following advantages can be achieved:

(a) MOSFETS that will be turned on only during the periods of operation are used to produce operation currents for the bipolar transistors that require relatively large operation currents. Therefore, wasteful consumption of electric current is reduced, and the consumption of electric power is greatly reduced.

(b) Since differential transistors consisting of bipolar transistors are used as a sense amplifier in a CMOS static RAM, only a very small electric current is allowed to flow into the data lines in reverse proportion to the current amplification factor. In other words, operation current of the sense amplifier can be increased even when the size of the memory cells is reduced to decrease the current driving ability. This makes it possible to accomplish a high reading operation.

(c) Since MOSFETs that will be turned on only during the reading operation are employed to produce operation currents for the differential transistors that constitute a sense amplifier, wasteful consumption of electric current is reduced. This helps maintain the advantage of low power consumption inherent in the CMOS static RAM, and a device employing bipolar transistor circuits can be realized which is powered by batteries and the like.

(d) The memory array M-ARY is divided into a plurality of blocks, and the sense amplifier is provided with an address decoder function, such that the consumption of electric power is further reduced and the operation speed is further increased.

(e) Since MOSFETs that will be turned on only when the chip is selected are used to produce reading and writing currents for the memory array M-ARY in the bipolar RAM and to produce currents for such peripheral circuits as the writing circuit and the reading circuit, it is made possible to greatly reduce the wasteful consumption of electric current when the chip is not being selected.

(f) MOSFETs are used to produce operation currents for the circuit blocks in the RAM, and the circuit blocks are time-serially

operated at required timings responsive to change detection signals of address signals. Therefore, wasteful consumption of electric current can be reduced under the condition in which the chip is selected.

5 A number of modifications of the invention described in the above two embodiments are possible. For instance, the resistors for holding data in the memory cells of the embodiment of Figure 1 may be replaced by p-channel MOSFETs. In place of the CMOS
10 circuit, furthermore, either the n-channel MOSFETs or p-channel MOSFETs may be employed. Further, the peripheral circuits and the timing control can be realized in a variety of other ways.

Moreover, the gates of p-channel MOSFETs which
15 produce operation currents for the bipolar transistors may be served with a predetermined constant voltage at the timings of operation.

The foregoing description has dealt with the case in which the invention was adapted to the CMOS
20 static RAM and the bipolar RAM that served as the background of the invention. The invention, however, should in no way be limited thereto only, but can be widely adapted to semiconductor integrated circuit devices that include bipolar transistors for amplifying
25 and transmitting signals and a circuit that produces operation currents for the bipolar transistors.

35 (39)

CLAIMS:-



1. A semiconductor integrated circuit device including:

(a) a differential circuit having first and second bipolar transistors which receive at respective bases thereof input signals and generate at respective collectors thereof output signals in response to the input signals, emitters of said first and second bipolar transistors being coupled to each other to form a common emitter;

(b) a first MOSFET that serves as a current source to supply an operating current to said differential circuit, said first MOSFET having a source-drain path coupled to said common emitter to form said operating current for said differential circuit; and

(c) means for generating a first control signal for application to a gate of said first MOSFET so that said bipolar transistors generate said output signals only during a period when said first MOSFET is rendered conductive by said first control signal.

2. A semiconductor integrated circuit device according to claim 1, wherein the input signals include complementary signals that have opposite phases to each other.

3. A semiconductor integrated circuit device according to claim 1, further including storage means for storing data therein and coupled to said first and second bipolar transistors to supply said input signals in response to the

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data stored in said storage means to the bases of said first and second bipolar transistors, respectively.

4. A semiconductor integrated circuit device according to claim 3, wherein said storage means includes a memory cell constructed of at least one MOSFET.

5. A semiconductor integrated circuit device according to claim 3, wherein said storage means includes a static memory cell constructed of a plurality of MOSFETs.

10 6. A semiconductor integrated circuit device according to claim 5, further including a pair of complementary data lines coupled to said respective bases of said first and second bipolar transistors for outputting signals in response to the input signals, wherein said static memory
15 cell comprises of a pair of MOSFETs having their gates and drains mutually cross-connected, high resistance elements being connected to the drains of the pair of MOSFETs, and a pair of transfer gate MOSFETs coupled between the drains of the pair of MOSFETs and said pair of complementary data
20 lines.

7. A semiconductor integrated circuit device according to claim 3, wherein said differential circuit is a sense circuit for sensing said input signals and wherein said



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generating means provides said first control signal for the gate of said first MOSFET to operate said sense circuit when said storage means is selected for a read operation.

- 5 8. A semiconductor integrated circuit device according to claim 7, wherein said generating means provides said first control signal when a write enable signal indicates a read condition to read the data stored in said storage means by said sense circuit.
- 10 9. A semiconductor integrated circuit device according to claim 7, wherein said generating means provides said first control signal when a chip select signal indicates a chip select condition to read the data stored in said storage means by said sense circuit.
- 15 10. A semiconductor integrated circuit device according to claim 7, wherein said generating means provides said first control signal when a chip is selected for a read operation.
- 20 11. A semiconductor integrated circuit device according to claim 1, wherein said output signals of said differential transistors are amplified by an amplifier circuit which consists of a bipolar transistor operating as an amplifier element and a second MOSFET which constitutes a current source for said amplifier circuit bipolar transistor, said second MOSFET receiving a second control signal whereby the



bipolar transistor of the amplifier circuit generates an output signal only during a period when said second MOSFET is rendered conductive by said second control signal.

5 12. A semiconductor memory device including:

(a) a memory array having a plurality of word lines, a plurality of data lines and a plurality of memory cells coupled to said plurality of said word and data lines so that each memory cell is coupled to a word line and at least
10 one data line, said memory array further having means for providing a pair of signals in response to data stored in a selected one of said plurality of memory cells;

(b) a read circuit coupled to receive a pair of signals of said memory array, said read circuit including a
15 pair of bipolar transistors coupled to form a differential circuit and a MOSFET to provide operating current to said differential circuit, said pair of bipolar transistors having bases coupled to receive said pair of signals and a common emitter coupled to said MOSFET, said MOSFET having a
20 source-drain path coupled to said common emitter to form said operating current for said differential circuit; and

(c) control means for providing a control signal to operate said MOSFET, which is coupled to a gate of said MOSFET, so that said control means provides said control
25 signal for said MOSFET to provide said operating current for said differential circuit to which said MOSFET is coupled, wherein said control signal is provided by said control



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means to read data stored in said one of said plurality of memory cells.

13. A semiconductor memory device according to claim 12,
5 further including address circuit means for selecting one of said plurality of memory cells, which is coupled to said memory array and which is coupled to receive address signals that indicate an address of said one of said plurality of memory cells in said memory array.

10 14. A semiconductor memory device according to claim 12, wherein said plurality of memory cells include static memory cells constructed of MOSFETs.

15 15. A semiconductor memory device according to claim 14, wherein said plurality of data lines are a plurality of pairs of complementary data lines, wherein each static memory cell is coupled to a pair of complementary data lines, and wherein each of said static memory cells comprises of a pair of MOSFETs having their gates and drains mutually cross-connected, high resistance elements being
20 connected to the drains of the pair of said MOSFETs, and a transfer gate MOSFET being coupled between the drains of the pair of said MOSFETs and said pair of complementary data lines.

16. A semiconductor memory device according to claim 12,

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wherein said differential circuit is a sense circuit.

17. A semiconductor memory device according to claim 12,
wherein said pair of signals generated from said memory
5 array include complementary signals that have opposite
phases to one another.

18. A semiconductor memory device according to claim 12,
wherein said MOSFET is turned on in accordance with said
control signal only when said memory array is selected for a
10 read operation.

19. A semiconductor memory device according to claim 12,
wherein said control signal includes a timing signal for
operating said differential circuit.

20. A semiconductor memory device according to claim 12,
15 wherein said control signal includes a pulse signal.

21. A semiconductor memory device according to claim 12,
wherein said control means includes a gate circuit.

22. A semiconductor memory device according to claim 12,
wherein said control means is coupled to receive at least
20 one internal control signal in accordance with at least one
external control signal applied from the outside of said
semiconductor memory and wherein control means provides said



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control signal for said MOSFET in accordance with said internal control signal indicating that said memory array is selected for a read operation.

5 23. A semiconductor memory device according to claim 12, wherein said control signal includes a predetermined voltage which is provided by said control means.

24. A semiconductor memory device according to claim 12, wherein further including a main amplifier coupled to
10 receive collector outputs of said differential circuit bipolar transistors, said main amplifier comprising a plurality of main amplifier bipolar transistors coupled to receive said collector outputs of said differential circuit bipolar transistors and at least one second MOSFET coupled
15 to provide operating current to said main amplifier bipolar transistors only when a second control signal has been received by said second MOSFET indicating that said memory array has been selected.

25. A semiconductor memory device according to claim 12,
20 further including a writing circuit having a plurality of bipolar transistors coupled to data lines of said memory array and a third MOSFET coupled to said writing circuit bipolar transistors to provide an operating current to said writing circuit bipolar transistors only when said first
25 control signal is received by said third MOSFET.



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26. A semiconductor memory device according to claim 12,
wherein a pair of bipolar transistors forms a sense
amplifier coupled to said data lines of said memory array to
5 receive output signals of said memory array.

27. A semiconductor memory device according to any one of
the preceding claims 12 to 26, wherein said control means
includes means for operating said first MOSFET in a
saturated region.

10 28. A semiconductor memory device according to claim 12,
wherein there are provided a plurality of memory arrays,
each coupled to a sense amplifier, further including a gate
circuit coupled to each of said sense amplifiers to provide
a control signal to said gate of a MOSFET of the respective
15 sense amplifier to which said gate circuit is coupled, each
gate circuit including means for providing said control
signal to said MOSFET of the respective sense amplifier to
which said gate circuit is coupled when one of the
respective memory array to which said respective sense
20 amplifier is coupled has been selected for operation.

29. A semiconductor memory including:

(a) a plurality of memory arrays each of which
includes a plurality of word lines, a plurality of data
lines and a plurality of memory cells coupled to said
25 plurality of said word and data lines so that each memory



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cell is coupled to a word line and at least one data line each of said plurality of memory arrays including means for providing a pair of output signals in response to

5 information stored in a selected one of said plurality of memory cells.

(b) a plurality of read circuits each of which is coupled to receive said pair of output signals of the respective memory array, said plurality of read circuits
10 including a pair of bipolar transistors to form a differential circuit and a MOSFET to provide operating current to said differential circuit, each said pair of bipolar transistors having bases coupled to receive said pair of output signals of the corresponding memory array and
15 a common emitter coupled to said MOSFET, the respective MOSFET having a source-drain path coupled to the common emitter of the corresponding pair of bipolar transistors;
and

(c) control means coupled to each of said MOSFETs to
20 provide a control signal to a gate of said MOSFET of the respective read circuit, said control means including means for providing said control signal to said MOSFET to the respective read circuit to which said control means is coupled and further including means for selecting one of
25 said MOSFETs to provide operating current to the corresponding differential circuit to which said one of said MOSFETs is coupled so that a selected one of said read circuits is operated to read information stored in said one



of said plurality of memory cells.

30. A semiconductor memory according to claim 29, wherein the collectors of the bipolar transistors in one of the read
5 circuits are coupled to the collectors of the bipolar transistors of all the other read circuits thereby forming common collectors which are coupled to a main amplifier for forming an output in response to input signals.

31. A semiconductor integrated circuit device according to
10 claim 1, wherein said bipolar transistors are of the NPN conductivity type and said MOSFET is an N-channel MOSFET.

32. A semiconductor memory device according to claim 12, or a semiconductor memory according to claim 29, wherein said bipolar transistors are of the NPN conductivity type and
15 said MOSFET is an N-channel MOSFET.

33. A semiconductor integrated circuit device constructed substantially as herein described with reference to and as illustrated in the accompanying drawings.
