CLAIMS

1. A circuit, comprising: a first layer, wherein the first layer includes two-dimensional (2D) shapes; a second layer coupled adjacent to the first layer through at least one via hole, wherein the second layer includes only one-dimensional (1D) shapes; a shared drain terminal; a source terminal termination; at least one continuous diffusion path placed between at least two positive channel metal oxide semiconductor (PMOS) transistors on either the first layer or the second layer; and a shallow trench isolation (STI) layer adjacent to a negative channel metal oxide semiconductor (NMOS) transistor.

2. The circuit of claim 1, further comprising a plurality of metal oxide semiconductor (MOS) transistors.

3. The circuit of claim 2, wherein at least two of the plurality of MOS transistors are associated with the shared drain terminal.

4. The circuit of claim 2, wherein at least one of the plurality of MOS transistors is associated with the source terminal termination.

5. The circuit of claim 2, wherein the plurality of MOS transistors includes at least two NMOS transistors.

6. The circuit of claim 5, wherein the plurality of MOS transistors includes at least two PMOS transistors.

7. The circuit of claim 2, wherein the plurality of MOS transistors includes at least two PMOS transistors.

8. The circuit of claim 1, wherein the first layer is a metal routing layer.

9. The circuit of claim 8, wherein the metal routing layer is a copper layer.

10. The circuit of claim 9, wherein the second layer is an interface layer made of cobalt or tungsten.

11. The circuit of claim 10, wherein the circuit is one of the following: a NAND gate, a NOR gate, an AND gate, a OR gate or an XOR gate.

12. The circuit of claim 10, wherein the circuit is a two-input NAND gate or a two-input NOR gate.

13. The circuit of claim 9, wherein the second layer is a local interconnect layer.

14. A method for fabricating an integrated circuit, the method comprising: configuring a first layer of the integrated circuit, wherein the first layer includes at least one two-dimensional (2D) shape; configuring a second layer of the integrated circuit adjacent to the first layer, wherein the second layer includes only one-dimensional (1D) shapes; configuring a shared drain terminal between two transistors in the integrated circuit, wherein a portion of the shared drain terminal resides within the second layer; configuring at least one continuous diffusion path placed between at least two positive channel metal oxide semiconductor (PMOS) transistors on either the first layer or the second layer; and configuring a shallow trench isolation (STI) layer adjacent to a negative channel metal oxide semiconductor (NMOS) transistor.

15. The method of claim 14, further comprising configuring a source terminal termination for the two transistors in the integrated circuit, wherein a portion of the source terminal termination resides within the second layer.

16. The method of claim 15, further comprising configuring the two transistors onto the integrated circuit.

17. The method of claim 15, wherein the first layer comprises at least one one-dimensional (1D) shape.

18. The method of claim 15, wherein the first layer is a metal routing layer.

19. The method of claim 18, wherein the metal routing layer is a copper layer.

20. The method of claim 15, wherein configuring the first layer is based in part on extreme ultraviolet (EUV) technology.

21. The method of claim 15, wherein the second layer is coupled adjacent to the first layer through at least one via hole.

22. The method of claim 15, wherein the second layer is an interface layer made of cobalt or tungsten.

23. The method of claim 22, wherein configuring the second layer is based in part on extreme ultraviolet (EUV) technology.

24. A method for fabricating an integrated circuit, the method comprising: configuring at least two negative channel metal oxide semiconductor (NMOS) transistors onto the integrated circuit; configuring a shallow trench isolation (STI) adjacent to the at least two NMOS transistors; configuring a first layer of the integrated circuit, wherein the first layer includes only one-dimensional (1D) shapes; configuring a second layer of the integrated circuit, wherein the second layer includes at least one two-dimensional (2D) shape; and configuring at least one continuous diffusion path placed between at least two positive channel metal oxide semiconductor (PMOS) transistors on either the first layer or the second layer.

25. The method of claim 24, wherein the first layer is adjacent to the second layer.

26. The method of claim 25, wherein the first layer is a contact merge (CM) layer made of cobalt or tungsten.

27. The method of claim 26, wherein the second layer is a metal layer made of copper.

28. The method of claim 27, wherein the at least two negative channel metal oxide semiconductor (NMOS) transistors include a shared drain terminal or the at least two positive channel metal oxide semiconductor (PMOS) transistors include a shared drain terminal.