

ABSTRACT OF THE DISCLOSURE

A three-dimensional semiconductor memory device includes first semiconductor patterns, which are vertically spaced apart from each other on a substrate, each of which includes first and second end portions spaced apart from each other, and first and second side surfaces spaced apart from each other to connect the first and second end portions, first and second source/drain regions disposed in each of the first semiconductor patterns and adjacent to the first and second end portions, respectively, a channel region in each of the first semiconductor patterns and between the first and second source/drain regions, a first word line adjacent to the first side surfaces and the channel regions and vertically extended, and a gate insulating layer interposed between the first word line and the first side surfaces. The gate insulating layer may be extended to be interposed between the first source/drain regions.

FIG. 3C