

STRUCTURE FOR RF USE

FIELD OF THE INVENTION

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The present invention relates to structures for RF uses. It relates in particular to a silicon-on-insulator structure comprising a trapping layer and a buried electrode.

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TECHNOLOGICAL BACKGROUND OF THE INVENTION

Integrated devices are usually produced on substrates in wafer form, which mainly serve as a mounting for the manufacture thereof. The increase in the degree of integration and expected performance of these devices has led to ever greater coupling between their performance and the characteristics of the substrate on which they are formed. This is particularly the case of radiofrequency (RF) devices that process signals with a frequency of around 3 kHz to 300 GHz, which are used in particular in the field of telecommunications (cellular telephones, Wi-Fi, Bluetooth, etc.).

As an example of device/substrate coupling, the electromagnetic fields from high-frequency signals propagating in the devices penetrate into the depth of the substrate and interact with any charge carriers that may be contained therein. This leads to problems of non-linear distortion of the signal (harmonics), unnecessary consumption of a part of the energy from the signal due to insertion loss, and possible influences between components.

Among the substrates suited to the production of RF devices, high-resistivity silicon substrates are known which comprise a support substrate, a trapping layer arranged on the support substrate, a dielectric layer arranged on the trapping layer, and a semiconductor layer arranged on the dielectric layer. The support substrate usually has a resistivity higher

than 1 kOhm.cm. The trapping layer can comprise non-doped polycrystalline silicon. The combination of a high-resistivity support substrate and a trapping layer according to the prior art makes it possible to reduce the aforementioned device/substrate coupling, and thus to ensure good performance of the RF devices. In this regard, a person skilled in the art would find a review of the performance of RF devices manufactured on the high-resistivity semiconductor substrate known from the prior art in "Silicon-on-insulator (SOI) Technology, manufacture and applications", points 10.7 and 10.8, Oleg Kononchuk and Bich-Yen Nguyen, Woodhead Publishing.

Furthermore, for the production of RF devices such as, for example, antenna switching units, contained in particular in mobile telephones, it is common to connect a plurality of transistors (for example, field effect transistors "FET") in series so as to maintain the maximum voltage applied to the terminals of the switching unit, said voltage being higher than the breakdown voltage of each individual transistor. However, the serial arrangement of a plurality of transistors has the drawback of increasing the serial resistance of the RF device, which can, in particular, degrade the linearity performance of the RF device.

SUBJECT OF THE INVENTION

The present invention aims to solve all or part of the aforementioned drawbacks. One particular aim of the invention is to propose a structure for RF use which allows the production of RF devices with enhanced performance.

BRIEF DESCRIPTION OF THE INVENTION

The present invention relates to a structure for RF use comprising:

- a high-resistivity support substrate in which a front surface defines a main plane,
- a charge trapping layer arranged on the front surface of the support substrate,
- 5 • a first dielectric layer arranged on the trapping layer,
- an active layer arranged on the first dielectric layer.

The structure is characterised in that it comprises at least one buried electrode arranged above or inside the trapping layer, the electrode comprising a conductive layer
10 and a second dielectric layer.

According to other advantageous and non-restrictive characteristics of the invention, taken either separately or in any technically feasible combination:

- 15 • the conductive layer has two surfaces according to the main plane: one surface in contact with the first dielectric layer and another surface in contact with the second dielectric layer;
- the electrode comprises a plurality of insulating walls
20 extending between the first and second dielectric layers and segmenting the conductive layer into a plurality of conductive blocks, said blocks being insulated from one another by the insulating walls;
- the electrode is arranged between the active layer and
25 the first dielectric layer, the second dielectric layer being in contact with the active layer, according to the main plane;
- the electrode is arranged between the first dielectric
30 layer and the charge trapping layer, the second dielectric layer being in contact with the trapping layer, according to the main plane;
- the buried electrode is discontinuous in the main plane and a plurality of charge trapping areas extend between the first dielectric layer and the charge trapping layer,

the trapping areas being insulated from the conductive blocks by the insulating walls;

- the structure comprises a third dielectric layer, between the charge trapping layer and the front surface of the support substrate;
- the electrode is arranged in the charge trapping layer, the second dielectric layer being in contact with the front surface of the support substrate according to the main plane, and wherein the electrode comprises a plurality of insulating walls extending between the first and second dielectric layers and defining a plurality of conductive blocks of the conductive layer, each conductive block being insulated from at least one trapping area forming the trapping layer, by the insulating walls;
- at least one conductive block is electrically connected to a contact pad arranged on a free surface of the active layer, by a conductive via passing through a portion of the structure from the conductive block to the contact pad;
- the structure also comprises a device in and/or on the active layer, including at least one transistor in which a gate electrode arranged on the free surface of the active layer is placed opposite at least one conductive block of the buried electrode;
- the second dielectric layer has a thickness of 5 nm to 100 nm;
- the conductive layer comprises a material selected among monocrystalline silicon, polycrystalline silicon and amorphous silicon;
- the conductive layer has a resistivity of several ohms.cm to several thousand ohms.cm;
- the conductive layer has a thickness of 50 nm to 500 nm;

- the conductive layer is formed by a material compatible with high-temperature treatments.

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BRIEF DESCRIPTION OF THE DRAWINGS

Further characteristics and advantages of the invention will be clear from the detailed description, made in reference to the appended figures, among which:

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- figures 1a and 1b show structures according to a first embodiment of the invention;
- figures 2a and 2b show structures according to a second embodiment of the invention;
- 15 - figure 3 shows a structure according to a third embodiment of the invention;
- figure 4 shows structures according to a fourth embodiment of the invention;
- figures 5a and 5b show structures according to the
20 invention.

DETAILED DESCRIPTION OF THE INVENTION

In the descriptive part, the same references in the figures can be used for elements of the same type.

5 The figures are diagrammatic representations which, for the sake of readability, are not to scale. In particular, the thicknesses of the layers according to the Z axis are not to scale relative to the lateral dimensions according to the X and Y axes.

10 The invention relates to a structure 100 for RF use comprising a high-resistivity support substrate 1. High resistivity is understood to mean a resistivity higher than 1000 ohm.cm, advantageously comprised between 4 and 10
15 kOhm.cm. The support substrate 1 can be made of materials commonly used in the microelectronic, optic, optoelectronic or photovoltaic industries. In particular, the support substrate 1 can comprise at least one material selected from the following group: silicon, silicon-germanium, silicon carbide,
20 etc.

The front surface 1a of the support substrate 1 defines a main plane (x,y) as shown in figure 1a. Advantageously, the support substrate 1 is in the shape of a circular wafer, with a diameter of 150, 200, 300 or 450 mm.

25 The structure 100 likewise comprises a charge trapping layer 2 arranged on the front surface 1a of the support substrate 1. Arranged is understood to mean that the trapping layer 2 can be either directly in contact with the front surface 1a of the support substrate 1 or rigidly connected to
30 same via one or more intermediate layers. The term "arranged" used hereinafter can be interpreted in a similar manner.

Advantageously, the trapping layer 2 comprises a polycrystalline silicon material, with a defect density that is favourable for trapping free electric charges that are

capable of developing in the support substrate 1. Evidently, the trapping layer 2 can likewise comprise other types of materials capable of providing the trapping function and compatible with the structure 100 and the use thereof. The trapping layer 2 has a thickness of several tens of nanometres to several microns, for example 50 nm to 3 microns.

The structure 100 also comprises a first dielectric layer 3 arranged on the trapping layer 2. In certain embodiments according to the invention, the first dielectric layer 3 will constitute the buried insulating layer of the structure 100, which in particular will electrically insulate the active layer 4 from the support substrate 1. Advantageously, without this having any limiting effect, the first dielectric layer 3 will comprise at least one of the materials chosen among: silicon dioxide, silicon nitride, aluminium oxide, etc. The thickness thereof can range, for example, from 10 nm to 3 μm .

The structure 100 likewise comprises an active layer 4 arranged on the first dielectric layer 3. The active layer 4 corresponds to the layer in and/or on which RF components can be produced. It includes a free surface or front surface 4a and a back surface 4b rigidly connected to the underlying layers. The active layer 4 can advantageously be made from semiconductor materials and/or piezoelectric materials. Advantageously, without this having any limiting effect, the active layer 4 comprises at least one of the materials chosen among: silicon, silicon carbide, silicon-germanium, lithium niobate, lithium tantalate, quartz, aluminium nitride, etc. The active layer 4 can have a thickness of several nanometres (for example 10 nm) to several microns, or even several tens of microns (for example 50 μm), according to the components to be manufactured.

Finally, the structure 100 according to the invention comprises at least one buried electrode 10 arranged above or

inside the trapping layer 2: figure 1a depicts an embodiment in which the buried electrode 10 is located above the trapping layer 2; in particular, it is located immediately below the active layer 4.

5 The buried electrode 10 comprises an electrically conductive layer 11 and a dielectric layer 13 (hereinafter referred to as second dielectric layer 13). The buried electrode 10 is intended for being biased by applying a voltage to the conductive layer 11, and for generating an
10 effect on the electrical carriers of the active layer 4.

 Preferably, without this having any limiting effect, the conductive layer 11 comprises a material selected among monocrystalline silicon, polycrystalline silicon, amorphous silicon, etc. or other materials commonly used for the
15 production of gate electrodes or microelectronic resistors. The material forming the conductive layer 11 advantageously has a resistivity of several ohms.cm to several thousand ohms.cm. It is preferably chosen to be compatible with high-temperature treatments, the structure 100 being likely to be
20 subjected to such treatments for the production of RF components. The conductive layer 11 has a typical thickness of 50 nm to 500 nm.

 The second dielectric layer 13 can preferably comprise at least one of the following materials: silicon dioxide,
25 silicon nitride, aluminium oxide, etc. It advantageously has a thickness of 5 nm to 100 nm. Nevertheless, its thickness may vary between 1 nm and 3 μm , according to the embodiments of the invention.

30 The conductive layer 11 has two surfaces 11a, 11b according to the main plane (x,y): in the example of figure 1a, the first surface 11a is in contact with the second dielectric layer 13 and the second surface 11b is in contact with the first dielectric layer 3.

Advantageously, the electrode 10 comprises a plurality of electrically insulating walls 14, extending between the first dielectric layer 3 and the second dielectric layer 13 (figures 1b and 2b). Said insulating walls 14 segment the conductive layer 11 into a plurality of conductive blocks 12, insulated from one another by said insulating walls 14.

According to the invention, it would thus be possible to apply an electric voltage to at least one conductive block 12 of the buried electrode 10, which is electrically insulated from the other layers of the structure 100, and in particular from the active layer 4 and from the support substrate 1. The conductive block 12 is advantageously located at least opposite the active region of a transistor which will be produced in the active layer 4: said transistor can then benefit from bias on the back surface 4b of the active layer 4, in addition to the usual bias thereof by a gate electrode. The use of back bias makes it possible to increase the breakdown voltage of the transistor and thus limits the number of transistors to be placed in series in order to withstand the voltage applied to the terminals of the RF device (switching unit for example). The serial resistance of the device can be reduced and the linearity thereof is improved.

According to a first embodiment, shown in figures 1a and 1b, the electrode 10 is arranged between the active layer 4 and the first dielectric layer 3, the second dielectric layer 13 being in contact with the active layer 4, according to the main plane (x,y).

In this case, the second dielectric layer 13 has a thickness of less than 400 nm, preferably of the order of 50 - 100 nm, so that the voltage applied to the conductive layer 11

of the buried electrode 10 can have an effect on the electrical carriers of the active layer 4.

5 The structure 100 presented in figure 1a can be produced using various methods. Some of these manufacturing variants are described hereunder.

10 The charge trapping layer 2 is first deposited on the support substrate 1. For example, a layer of polycrystalline silicon constituting the trapping layer 2 may be deposited by a chemical vapour or liquid deposition technique or else by epitaxy on a support substrate 1 made of silicon. The trapping layer 2 has a thickness comprised in the aforementioned range, for example of the order of 2 microns.

15 The active layer 4 is added to the support substrate 1 including the trapping layer 2 by one of the thin layer transfer techniques based on adhesion by molecular bonding: indeed, such direct adhesion has the advantage of being perfectly compatible with high-temperature treatments. These thin layer transfer techniques can include, in particular, the following:

- the Smart CutTM method, which is based on implanting light hydrogen and/or helium ions in a donor substrate (from which the active layer 4 is made), and assembling said donor substrate by molecular bonding with the support substrate 1; a detachment step then makes it possible to separate a surface thin layer from the donor substrate (the active layer 4), at the embrittlement plane defined by the ion implantation depth. Finishing steps, possibly including high-temperature thermal treatments, finally grant the crystalline quality and surface quality required for the active layer 4. This method is particularly well suited to the production of active thin layers, with a thickness of

several nanometres to around 1.5 μm , for example, for the silicon layers;

- the Smart Cut method followed by an epitaxy step, which makes it possible to obtain thicker active layers, for example of several tens of nm to 20 μm ;
- the methods for direct adhesion and mechanical, chemical and/or mechanical-chemical thinning consist of assembling the donor substrate (from which the active layer 4 is made) by molecular bonding with the support substrate 1, and then thinning the donor substrate until the desired thickness of the active layer 4, for example by grinding and polishing (CMP, or chemical mechanical polishing). These methods are suitable in particular for the transfer of thick layers, for example from several microns to a plurality of tens of microns, and up to several hundred microns.

Considering the aforementioned layer transfer techniques, it is convenient to define the substrate, between the donor substrate (from which the active layer 4 is made) or the support substrate 1 (on which the trapping layer 2 is deposited), on which the intermediate layers such as the first dielectric layer 3, the conductive layer 11 and the second dielectric layer 13 of the electrode 10 (figure 1a) will be formed, prior to assembling the two substrates by molecular bonding at a bonding interface.

According to a first assembly option, the bonding interface is located between the second dielectric layer 13 and the conductive layer 11. This means that the second dielectric layer 13 has been formed on the donor substrate; for example, this layer is made up of a layer of silicon oxide, grown thermally on the donor substrate. In addition, the first dielectric layer 3, and then the conductive layer 11, are deposited in series on the trapping layer 2. The first dielectric layer 3 consists, for example, in a layer of

silicon oxide grown thermally on the trapping layer 2 or deposited by chemical deposition; the conductive layer 11 is made up of a layer of polycrystalline silicon with a resistivity of several ohms.cm to several kOhms.cm. In the configuration depicted in figure 1b, the conductive layer 11 comprises insulating walls 14, which define a plurality of conductive blocks 12. As is generally known for a person skilled in the art, the formation of the conductive layer 11 then requires at least one step of lithography and etching in order to define the distribution of the conductive blocks 12 and the insulating walls 14 in the plane (x,y) and to form them in series.

According to a second assembly option, the bonding interface is located between the conductive layer 11 and the first dielectric layer 3. In this case, the second dielectric layer 13 is formed on the donor substrate, since the conductive layer 11 is formed on the second dielectric layer 13. Furthermore, the first dielectric layer 3 is deposited on the trapping layer 2 rigidly connected to the support substrate 1.

According to a third assembly option, the bonding interface is located between the first dielectric layer 3 and the trapping layer 2. In this case, the second dielectric layer 13 is first formed on the donor substrate, then the conductive layer 11 is formed on the second dielectric layer 13, and finally the first dielectric layer 3 is formed on the conductive layer 11.

Other assembly options obviously exist, for which in particular the adhesion interface can be placed in one of the intermediate layers, for example at the middle of the first dielectric layer 3. For example, a first portion of the first dielectric layer 3 is formed on the donor substrate (from which the active layer 4 is made); a second portion of the

first dielectric layer 3 is formed on the side of the support substrate 1, after the formation of the underlying layers.

In each of the aforementioned assembly options, the donor and support substrates, provided with the respective layers thereof, are assembled by molecular bonding. The implementation of either of the preceding layer transfer techniques then leads to the formation of the active layer 4.

According to a second embodiment shown in figures 2a and 2b, the electrode 10 is deposited between the first dielectric layer 3 and the charge trapping layer 2, the second dielectric layer 13 being in contact with the trapping layer, according to the main plane (x,y). The first surface 11a of the conductive layer 11 is in contact with the first dielectric layer 3 and the second surface 11b thereof is in contact with the second dielectric layer 13.

In this case, the first dielectric layer 3 has a thickness of less than 400 nm, preferably less than 200 nm, so that the voltage applied to the conductive layer 11 of the buried electrode 10 can have an effect on the electrical carriers of the active layer 4. The second dielectric layer 13, on the other hand, can have a thickness of up to several microns, if this is required for the application.

The techniques for transferring layers and manufacturing insulating walls 14 in the conductive layer 11 mentioned in the first embodiment likewise apply to this second embodiment. Different assembly options can be implemented, according to whether the formation of intermediate layers of the structure 100 (first dielectric layer 3, conductive layer 11 and second dielectric layer 13) is carried out on the donor substrate or the support substrate 1.

According to a third embodiment, depicted in figure 3, the electrode 10 is arranged as above between the first dielectric layer 3 and the charge trapping layer 2 and it includes conductive blocks 12 electrically insulated from one another by insulating walls 14; furthermore, the buried electrode 10 is discontinuous in the main plane (x,y) and a plurality of charge trapping areas 22 extend between the first dielectric layer 3 and the charge trapping layer 2. The trapping areas 22 are insulated from the conductive blocks 12 by the insulating walls 14.

The trapping areas 22 can be made from the same material as the trapping layer 2 or from a different material, having electric charge trapping properties.

In this third embodiment of the invention, the first dielectric layer 3 has a thickness of less than 400 nm, preferably less than 200 nm, so that the voltage applied to the conductive layer 11 of the buried electrode 10 can have an effect on the electrical carriers of the active layer 4.

The layer transfer techniques described for the first embodiment also apply to this third embodiment. Advantageously, an assembly option which consists of placing the adhesion interface in the first dielectric layer 3 would be implemented. A first portion of the first dielectric layer 3 is formed on the donor substrate (from which the active layer 4 is made); a second portion of the first dielectric layer 3 is formed from the side of the support substrate 1, after the formation of the underlying layers. The trapping layer 2 is first produced on the support substrate 1. The second dielectric layer 13 is then deposited (chemical deposition or thermal growth). A lithography and etching step makes it possible to remove the second dielectric layer 13 from the future trapping areas 22. Other consecutive steps of

masking, depositing and etching then make it possible to form the conductive blocks 12, the insulating walls 14 and the trapping areas 22. The second portion of the first dielectric layer 3 is then deposited above the conductive blocks 12, the insulating walls 14 and the trapping areas 22. A step of planarising said second portion of the first dielectric layer 3 then makes it possible to obtain a good surface condition with a view to direct adhesion.

The donor and support substrates, provided with their respective layers, are then assembled by molecular bonding. The implementation of either of the aforementioned layer transfer techniques then leads to the formation of the active layer 4.

According to a fourth embodiment shown in figure 4, the electrode 10 is arranged in the charge trapping layer 2. The second dielectric layer 13 is in contact with the front surface 1a of the support substrate 1 according to the main plane (x,y). The electrode 10 comprises a plurality of insulating walls 14 extending between the first 3 and second 13 dielectric layers and defining a plurality of conductive blocks 12 of the conductive layer 11, insulated from one another by said insulating walls 14. Each conductive plate 12 is electrically insulated from at least one charge trapping area 23 forming the trapping layer 2, by the insulating walls 14. The charge trapping area 23 extends between the first dielectric layer 3 and the support substrate 1.

According to a variant which can be applied to the various aforementioned embodiments, the structure 100 can comprise a third dielectric layer 30, arranged between the trapping layer 2 (or the charge trapping areas 23) and the

support substrate 1. It can comprise at least one of the following materials: silicon dioxide, silicon nitride, aluminium oxide, etc. It is advantageous in particular in that it prevents or at least considerably limits the recrystallisation of the trapping layer 2 (when the latter is made of, for example, polycrystalline silicon) during high-temperature thermal treatments likely to be used for manufacturing the structure according to the invention.

In the structure 100 according to any of the mentioned embodiments, at least one conductive block 12 can be electrically connected to a contact pad 40 by a conductive via 41. The latter passes through a portion of the structure 100 to run from the conductive block 12 to said contact pad 40; in the example of figure 5a, the conductive via 41 passes in particular through the active layer 4 and the second dielectric layer 13. The contact pad 40 is arranged on a free surface 4a of the active layer 4, electrically insulated from same.

The contact pad 40 is formed by an electrically conductive material by means of which a voltage can be applied to the conductive block 12 of the buried electrode 10. The conductive via 41 is formed, using techniques that are known to a person skilled in the art, by making a trench in which the walls are electrically insulated from the layers through which it passes, which is filled with a conductive material, for example doped polycrystalline silicon.

A plurality of conductive vias 41 can be made to connect each embedded conductive block 12 independently to a contact pad 40.

Alignment marks would have advantageously been formed on the support substrate 1 (or on the donor substrate from which the active layer 4 is made) during the production of conductive blocks 12. These alignment marks are used during

the steps of producing conductive vias 41, in order to form the vias vertically in line with the conductive blocks 12.

5 The structure 100 can likewise comprise a device in and/or on the active layer 4, including at least one transistor 50 in which a gate electrode 51 arranged on the free surface 4a of the active layer 4 is opposite at least one conductive block 12 of the buried electrode 10 (figure 5b). The alignment marks formed during the production of the
10 conductive blocks 12 of the buried electrode 10 are likewise used during steps for manufacturing the electronic device on the active layer 4.

15 The structure 100 according to the invention is particularly suitable for RF devices, in particular such as antenna adapters or switching units for mobile telephones. The integration of the buried electrode 10 in the structure 100 allows for easier manufacturing of devices comprising
20 transistors with back bias. The use of a buried electrode 10 to bias the active region 52 of a transistor 50 by the back surface (back bias) makes it possible to increase the breakdown voltage of the transistor and thus to limit the number of transistors to be arranged in parallel in each
25 device. Finally, the presence of the charge trapping layer 2 in the structure 100 ensures that a high resistivity of the support substrate 1 is maintained.

The structure 100 according to the invention thus makes it possible to achieve high performance in the field of high-
30 frequency applications.

The invention is obviously not limited to the described embodiments, and alternative embodiments can be provided

without departing from the context of the invention as defined by the claims.

CLAIMS

1. Structure (100) for RF use comprising:

- 5 • a high-resistivity support substrate (1), of which a front surface (1a) defines a main plane,
- a charge trapping layer (2) arranged on the front surface (1a) of the support substrate (1),
- 10 • a first dielectric layer (3) arranged on the trapping layer (2),
- an active layer (4) arranged on the first dielectric layer (3),

 the structure (100) being characterised in that it comprises at least one buried electrode (10) arranged

15 above or inside the trapping layer (2), the electrode (10) comprising a conductive layer (11) and a second dielectric layer (13).

2. Structure (100) for RF use according to the preceding

20 claim, wherein the conductive layer (11) has two surfaces (11a, 11b) according to the main plane: one surface in contact with the first dielectric layer (3) and another surface in contact with the second dielectric layer (13).

25 3. Structure (100) for RF use according to the preceding claim, wherein the electrode (100) comprises a plurality of insulating walls (14) extending between the first (3) and second (13) dielectric layers and segmenting the conductive layer (11) into a plurality of conductive

30 blocks (12), said blocks (12) being insulated from one another by the insulating walls (14).

4. Structure (100) for RF use according to any of the three preceding claims, wherein the electrode (10) is arranged

between the active layer (4) and the first dielectric layer (3), the second dielectric layer (13) being in contact with the active layer (4), according to the main plane.

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5. Structure (100) for RF use according to any claim 1 to 3, wherein the electrode (10) is arranged between the first dielectric layer (3) and the charge trapping layer (2), the second dielectric layer (13) being in contact with the trapping layer (2), according to the main plane.

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6. Structure (100) for RF use according to the preceding claim taken in combination with claim 3, wherein the electrode (10) is discontinuous in the main plane and a plurality of charge trapping areas (22) extend between the first dielectric layer (3) and the charge trapping layer (2), the trapping areas (22) being insulated from the conductive blocks (12) by the insulating walls (14).

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7. Structure (100) for RF use according to any claim 1 and 2, wherein the electrode (10) is arranged in the charge trapping layer (2), the second dielectric layer (13) being in contact with the front surface (1a) of the support substrate (1) according to the main plane, and wherein the electrode (10) comprises a plurality of insulating walls (14) extending between the first (3) and second (13) dielectric layers and defining a plurality of conductive blocks (12) of the conductive layer (11), each conductive block (12) being insulated from at least one trapping area (23) forming the trapping layer (2), by the insulating walls (14).

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8. Structure (100) for RF use according to any claim 3 or 7, wherein at least one conductive block (12) is

electrically connected to a contact pad (40) arranged on a free surface (4a) of the active layer (4), by a conductive via (41) passing through a portion of the structure (100) from the conductive block (12) to the contact pad (40).

9. Structure (100) for RF use according to the preceding claim, also comprising a device in and/or on the active layer (4), including at least one transistor (50) of which a gate electrode (51) arranged on the free surface (4a) of the active layer (4) is placed opposite at least one conductive block (12) of the buried electrode (10).

10. Structure (100) for RF use according to any preceding claim, wherein the second dielectric layer (13) has a thickness of 5 nm to 100 nm.

11. Structure (100) for RF use according to any preceding claim, wherein the conductive layer (11) comprises a material selected among monocrystalline silicon, polycrystalline silicon and amorphous silicon.

12. Structure (100) for RF use according to any preceding claim, wherein the conductive layer (11) has a thickness of 50 nm to 500 nm.

13. Structure (100) for RF use according to any preceding claim, wherein the conductive layer has a resistivity of several ohms.cm to several thousand ohms.cm.