

ABSTRACT

A memory device according to an aspect may include a memory cell array including a first bank region and a second bank region each including a plurality of banks; an operation logic including one or more first processing elements (PEs) corresponding to the first bank region and one or more second PEs corresponding to the second bank region; a control logic configured to control modes of the first bank region and the second bank region based on externally sourced setting information; first and second mode signal generators configured to control enabling the first PEs, wherein the first mode signal generator is configured to output the first mode signal to enable the first PEs and the second mode signal generator is configured to output the second mode signal to disable the second PEs responsive to the first bank region being set to an operation mode and the second bank region being set to a normal mode.

FIG. 1