Description

This invention relates to improvement of a signal electrode drive apparatus which is contained in the display-drive circuit for use in a liquid crystal display device.

A portable television employs a liquid crystal display device to provide its picture. An example of this known type of TV set is disclosed in U.S. Pat. No. US-A-4,581,654. The display-drive circuit of this prior art TV set is configured as shown in Figs. 1 through 3. Fig. 1 shows a configuration of the overall displaydrive circuit. In the figure, reference numeral 1 designates a simple matrix liquid crystal display panel of, for example, 120 x 160 dots. Numeral 2 designates a scanning electrode drive circuit, and 3a and 3b denotes signal electrode drive circuits. Scanning electrode drive circuit 2 sequentially drives scanning electrodes X1 to X120 of display panel 1. The sequential drive operation is timed by a timing signal from a controller (not shown). Signal electrode drive circuits 3a and 3b drive groups of signal electrodes Y1 to Y80 and Y81 to Y160, respectively. The drive operation is performed using an n-bit digital signal, passed through an A/D converter, and a timing signal from the controller. More specifically, circuit 3a fetches the data of 80 lines, which comprise the left-hand portion of the input data record during the effective horizontal scanning period. Electrode drive circuit 3b fetches the data of 80 lines in the right-hand portion. On the basis of the fetched data, drive circuits 3a and 3b drive the respective groups of electrodes Y1 to Y80 and Y81 to Y160, in synchronism with the driving of scanning electrodes X1 to X120.

Fig. 2 shows in block diagraph the details of the prior art signal electrode drive circuit 3a. In the figure, shift register 11 is provided in each stage of 80 stages, and which consists of a 4-bit register. The 4-bit video data coming from an A/D converter (not shown) is sequentially stored in the the shift register, in synchronization with sampling clock ϕs. The data loaded is transferred to graduation signal-forming circuit 13, via buffer 12 which consists of 80 stages, each stage including 4-bit buffer registers, and which operates in synchronism with a latch pulse ϕL.

Intensity modulation pulse-generating circuit 15 responds to latch pulse ϕL and counts clock pulse ϕ2, to form intensity modulation pulses P1 to P4. These pulses P1 to P4 are input to graduation signal-forming circuit 13. Circuit 15 contains a counter, which is reset by latch pulse ϕL, and which frequency-divides, by 2, the frequency of clock pulse ϕ2, to form intensity modulation pulses P1 to P4. Clock pulse ϕ2 is a fundamental clock signal with a frequency of 3 MHz. Graduation signal-forming circuit 13 appropriately processes the 4-bit video data latched in buffer 12, and the intensity modulation pulses P1 to P4 generated by intensity modulation pulse-generating circuit 15, and forms 16 types of graduation signals S1 to S80 with different time widths. These graduation signals are transferred to 2-channel analog multiplexer 14. Multiplexer 14 also appropriately processes graduation signals S1 to S80 from graduation signal-forming circuit 13 and field-select signal ϕf, and forms signal electrode drive signals Y1 to Y80, to drive liquid crystal display panel 1.

Fig. 3 shows in detail one stage of the signal electrode drive circuit of Fig. 2 which consists of 80 stages, as previously stated. As is shown in shift register 11, each stage is made up of one register 111 of 4 bits, which is operated in response to sampling clock pulse ϕs. Data of 4 bits D1 to D4 coming from the A/D converter (not shown) are loaded into register 111, and then transferred to register 112, at the next stage. Buffer 12 includes a 4-bit buffer register 121 in each stage of 80 stages. The data from register 111 is loaded into buffer register 121 in synchronism with latch pulse ϕL. The data is then transferred to graduation signal-forming circuit 13. Graduation signal-forming circuit 13 consists of OR circuits 131 to 134, AND circuit 135, and flip-flops 136 to 138. The data from buffer register 121, together with intensity-modulation pulses P1 to P4 from modulation pulse-generating circuit 25, is input to AND circuit 135, via OR circuits 131 to 134. The output data from AND circuit 135 is input to flip-flop 136, in synchronism with clock pulse ϕ2. The output data of flip-flop 136 is input to the reset terminal R of flip-flop 137. Flip-flop 137 is set by latch pulse ϕL. Flip-flop 136 is reset by latch pulse ϕL. The output signal of flip-flop 137 is loaded into flip-flop 138, in synchronism with clock pulse ϕ2. The output signal from flip-flop 138 is transferred, as a graduation signal Si, to analog multiplexer 14. Multiplexer 14 is made up of decoder 141, and transfer gates 142 to 145. Multiplexer 14 receives a graduation signal Si and a frame-select signal ϕf. Transfer gates 142 to 145 are coupled with V5, V2, V3, and V0, respectively. These gates are gate-controlled by the output signal from decoder 141. By way of this gate control, one of voltages V5, V2, V3, and V0 is selected and output as a signal electrode drive signal Yi.

As can be seen from the foregoing, the signal electrode drive circuit is arranged such that each stage of shift register 11 is made up of a register 111. Shift register 11 in each stage of 80 stages contains register 111, 112,..., respectively, each of which transfers the video data of 4-bits. Register 111 is comprised of, for example, inverter including two transistors, and a clocked inverter including four transistors. The fact that the signal electrode drive

circuit requires 80 stages for transferring video data at high speed, for example, 3 MHz which is the frequency of the fundamental clock signal, implies an increase in current dissipation in that drive circuit.

GB-A-2155221 discloses an LCD drive circuit including a plurality of latch circuits to latch video signals simultaneously under the control of multiphase clock signals derived from a counter/decoder circuit.

Accordingly, an object of this invention is to provide a signal electrode drive apparatus for use in a liquid crystal display, which requires a relatively small number of circuit elements for its circuit construction, and therefore consumes less current.

According to this invention, a signal electrode drive apparatus for use in a liquid crystal display comprises latch circuit means including m stages of shift registers and m buffer registers, one shift register in each stage successively shifting a latch pulse ϕM in synchronism with fundamental clocks, to generate m latch clocks ϕT1 to ϕTm with different phases, and each of the buffer registers latching in parallel fashion the n-bit video data in synchronism with the latch clocks ϕT1 to ϕTm output from the shift registers, the buffer registers of each stage being coupled with the video data, and means for generating signal electrode drive signals for a liquid crystal panel, by using the video data, latched in the buffer register at each stage.

With such an arrangement, the signal electrode drive apparatus according to this invention uses a latch circuit for transferring the high-speed data as the video data, in place of the shift register as employed by the prior art. The buffer register in this latch circuit latches the 4-bit video data once, in one horizontal scanning period, and holds it until the next latch pulse is generated. This feature reduces the current dissipation remarkably. The shift register, which is used in the latch circuit and which generates m latch clocks ϕT1 to ϕTm with different phases, by sequentially shifting the latch pulse M in synchronism with the fundamental clock pulse ϕ2, need only be capable of shifting one bit at each stage. This feature also further reduces the power dissipation from that of the prior art. Furthermore, the number of circuit elements used for forming the latch circuit is less than that for the prior art.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 shows a block diagram of a display drive circuit for use in a prior liquid crystal display, for example, a liquid crystal TV set;

Fig. 2 shows a block diagram of a signal electrode drive circuit used in the display drive circuit of Fig. 1;

Fig. 3 shows a circuit diagram of one stage of the signal electrode drive circuit of Fig. 2;

Fig. 4 is a block diagram of a signal electrode drive circuit according to one embodiment of this invention;

Fig. 5 is a circuit diagram of a latch circuit and a buffer used in the circuit of Fig. 4;

Fig. 6 shows a timing chart for help in explaining the operation of the circuits of Figs. 4 and 5;

Figs. 7A and 7B show a symbol of a circuit element used by the signal element drive circuit according to this invention, and its circuit diagram; and

Fig. 8 shows a circuit diagram showing how to combine the circuit elements used in the circuit of Fig. 5.

An embodiment of a signal electrode drive apparatus for use in a liquid crystal display according to this invention will now be described with reference to the accompanying drawings.

Fig. 4 shows a circuit configuration of the signal electrode drive circuit in a display drive circuit of the liquid crystal display. When this signal electrode drive circuit is applied to the display drive circuit shown in Fig. 1, it is used as the signal electrode drive circuit 3a. Reference numeral 21 designates a latch circuit made up of 80 stages. Applied to latch circuit 21 are 4-bit video data coming from an A/D converter (not shown) and latch pulse ϕM. Latch circuit 21 includes a shift register, which sequentially shifts latch pulse ϕM from the timing signal-generating circuit. In synchronism with the latch pulse as shifted by the shift register, the latch circuit latches the 4-bit video data, and outputs it to buffer 22. Latch circuit 21 shifts latch pulse ϕM from the right stage to the left stage as shown in the drawing, i.e. from the portion connected to signal electrode drive signal Y80 to the portion connected to signal Y1. Latch circuit 21 will now be described in detail. In the description to follow, graduation signal-forming circuit 23 and analog multiplexer 24, succeeding buffer 22, will not be described in detail, since each of these circuits may have the same construction as those of the Fig. 3 circuit.

Referring now to Fig. 5, the circuitry shown in this figure corresponds to latch circuit 21 and buffer 22, which correspond to the signal electrode drive signal Y80. In latch circuit 21, reference numeral 211 indicates a 4-bit buffer register, and numeral 212 denotes a shift register. The buffer register 211 provided in each stage of latch circuit 21 is coupled with the 4-bit video data D1 to D4 coming from the A/D converter in parallel fashion. The video data are then loaded into the shift register 212 in buffer

22. Shift register 212 is also coupled with latch pulse ϕM. As shown in Fig. 6, shift register 212 fetches latch pulse ϕM in synchronism with clock pulse ϕ2, and outputs it to the next shift register 212. More specifically, shift regis-ter 212 first fetches latch pulse ϕM in synchronism with clock pulse ϕ2. Subsequently, the shift registers 212 in the subsequent stages successively produce latch clocks ϕT80 to ϕTI in synchronism with clock pulse ϕ2. By means of these latch clocks, the 4-bit video data are successively latched into the buffer registers 2II in the respective stages. After these latching operations for the shift registers at all stages, latch pulse ϕL is generated, and the video data held by buffer register 2II is transferred to buffer 22. The video data is then transferred to analog multiplexer 24 via graduation signal-forming circuit 23. Multiplexer 24 forms signal electrode drive signals YI to Y80, by using the graduation signal from circuit 23 and frame-select signal ϕf.

A typical example of the circuit element of latch circuit 2I is symbolically illustrated in Fig. 7A. This circuit element of Fig. 7A is a NOR gate 70, which can be comprised of, for example, 4 MOS transistors combined, as shown in Fig. 7B. A CMOS inverter, which contains transistors combined, as shown in Fig. 8, may be used as shift register 212, buffer register 2II and shift register 212 in buffer 22. Using this arrangement, the number of inverters, particularly in buffer register 2II, may be I2 for the 4-bit video data, while it is 24 in the prior device. As a result, power dissipation can also be reduced remarkably. Incidentally, latch pulses M and L and clock pulse ϕ2 shown in Figs. 4 and 5, may be generated by the controller, as disclosed in USP No. US-A-4,58I,654.

Claims

1. A signal electrode drive apparatus for use in a liquid crystal display, characterized by comprising:

   latch circuit means (2I) including m stages of shift registers and m buffer registers (22), one shift register in each stage successively shifting a latch pulse M in synchronism with fundamental clocks, to generate m latch clocks TI to Tm with different phases, and each of said buffer registers latching in parallel fashion the n-bit video data in synchronism with the latch clocks ϕTI to ϕTm output from said shift registers, the buffer registers of each stage being coupled with said video data; and means (23) for generating signal electrode drive signals for a liquid crystal panel, by using the video data latched in the buffer register at each stage.

Revendications

1. Dispositif de commande d'électrodes de signaux pour dispositif de visualisation à cristaux liquides, caractérisé en ce qu'il comprend:

   un moyen de circuit de verrouillage (21) incluant m étages de registres à décalage et m registres-tampons (22), un registre à décalage de chaque étage décalant successivement une impulsion de verrouillage M en synchronisme avec des signaux d'horloge fondamentaux,pour engendrer m signaux d'horloge de verrouillage T1 à Tm de différentes phases, et chacun desdits registres - tampons verrouillant en parallèle les n bits de données vidéo en synchronisme avec les signaux d'horloge de verrouillage ϕT1 à ϕTm en sortie desdits registres à décalage, les registres-tampons de chaque étage étant couplés pour recevoir lesdites données vidéo; et un moyen (23) pour engendrer des signaux de commande d'électrodes de signaux pour un panneau à cristaux liquides, par la mise en oeuvre des données vidéo verrouillées dans le registre-tampon de chaque étage.

Patentansprüche

1. Steuervorrichtung für eine Signalelektrode zur Verwendung in einer Flüssigkristallanzeige, gekennzeichnet durch:
   eine Raster-Schaltungs-Vorrichtung (21) mit m-Stufen von Schieberegistern und M-Pufferregister (22), wobei ein Schieberegister in jeder Stufe nacheinander einen Raster-Impuls M synchron mit Grundtakten verschiebt, um m-Raster-Takte T1 bis Tm mit unterschiedlichen Phasenlagen zu erzeugen, und jedes der Pufferregister die n-Bit Videodaten in paralleler Weise synchron mit den Raster-Takten ϕT1 bis ϕTm, wie sie von den Schieberegistern ausgegeben werden, zusammenrastet, wobei die Pufferregister jeder Stufe mit den Videodaten gekoppelt sind; sowie eine Vorrichtung (23) zur Erzeugung von Signalelektroden-Steuersignalen für eine Flüssigkristalltafel durch Verwendung der in jeder Stufe im Pufferregister zusammengerasteten Videodaten.

22. Shift register 212 is also coupled with latch pulse ϕM. As shown in Fig. 6, shift register 212 fetches latch pulse ϕM in synchronism with clock pulse ϕ2, and outputs it to the next shift register 212. More specifically, shift regis-ter 212 first fetches latch pulse ϕM in synchronism with clock pulse ϕ2. Subsequently, the shift registers 212 in the subsequent stages successively produce latch clocks ϕT80 to ϕTI in synchronism with clock pulse ϕ2. By means of these latch clocks, the 4-bit video data are successively latched into the buffer registers 2II in the respective stages. After these latching operations for the shift registers at all stages, latch pulse ϕL is generated, and the video data held by buffer register 2II is transferred to buffer 22. The video data is then transferred to analog multiplexer 24 via graduation signal-forming circuit 23. Multiplexer 24 forms signal electrode drive signals YI to Y80, by using the graduation signal from circuit 23 and frame-select signal ϕf.

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