

SURGE-VOLTAGE ABSORBING APPARATUS

TECHNICAL FIELD

[0001] The present invention relates to a surge-voltage absorbing apparatus.

BACKGROUND ART

5 **[0002]** As a technique for protecting a variety of electrical equipment from surge voltage, Patent Document 1 cited below describes in paragraph 0004: "if a varistor has short-circuited, for example, due to aging, the varistor is heated by a short-circuit current flowing through the varistor to cause a thermal separation mechanism to react to turn off a contact portion, and then the varistor is disconnected from a DC
10 power supply line C. This allows for preventing the varistor itself or peripheral circuits from burning out."

PRIOR ART DOCUMENTS

Patent Documents

[0003] Patent Document 1: Japanese Patent Application Publication No. 2014-
15 155339

SUMMARY OF THE INVENTION

Problems to be solved

[0004] Incidentally, a "short mode" and an "open mode" have been known as modes of a surge protective element, such as a varistor, being exhausted or failing.
20 The "short mode" indicates a mode in which a leakage current increases, for example, due to aging of the surge protective element, to cause the varistor or the like to generate more heat. To cope with this, a thermal separation mechanism such as a thermal fuse may be arranged to separate the varistor or the like from the circuit. On the other hand, the "open mode" indicates a mode in which, when a very large
25 surge current flows in a varistor or the like momentarily such as when subjected to direct lightning strikes, the varistor or the like bursts before the thermal separation mechanism such as a thermal fuse reacts, to cause the varistor or the like to be in an open state. Currently, there is no method known that can detect a failure in the open mode inexpensively from a remote location, and therefore a failure in the open mode
30 is determined, for example, by way of visual check or the like in many cases to make the maintenance troublesome.

The present invention has been made in view of the circumstances as described above to provide a surge-voltage absorbing apparatus that allows for high maintainability.

Solution to resolve Problems

- 5 **[0005]** In order to solve the problem as described above, a surge-voltage absorbing apparatus according to the present invention includes:
- a) a group of surge absorbing units having at least three surge absorbing units for use in a three-phase voltage system, each of the surge absorbing units having:
- 10 a first surge-voltage absorbing circuit that includes a first voltage absorbing element which is in a conducting state when a voltage across both ends of the first surge-voltage absorbing element is equal to or higher than a predetermined voltage, and is inserted between two lines where a surge voltage can occur;
- a second surge-voltage absorbing circuit that includes a second surge-voltage absorbing element which is in a conducting state when a voltage across both ends of
- 15 the second surge-voltage absorbing element is equal to or higher than a predetermined voltage, and is inserted between the two lines;
- a first relay contact that inserts the first surge-voltage absorbing circuit between the two lines when the first relay contact is in an ON-state; and
- a second relay contact that inserts the second surge-voltage absorbing circuit
- 20 between the two lines when the second relay contact is in an ON-state; and
- b) a control circuit that sets the second relay contact in each of the surge absorbing units to an OFF-state until detecting the first surge absorbing circuit being in an exhausted condition, and sets the second relay contact in each of the surge absorbing units to an ON-state upon detecting the first surge absorbing circuit being
- 25 in an exhausted condition.

Advantageous Effects of the Invention

[0006] A surge-voltage absorbing apparatus according to the present invention allows for high maintainability.

BRIEF DESCRIPTION OF DRAWINGS

- 30 **[0007]** FIG.1 is a block diagram of a surge protective apparatus according to an embodiment of the present invention.
- FIGS. 2A and 2B are circuit diagrams of a surge absorbing unit.
- FIG. 3 is a waveform chart of components in the surge protective apparatus.

FIG. 4 is a state transition diagram of the surge protective apparatus.

FIG. 5 is a circuit diagram of a modification of a surge protective device (SPD).

EMBODIMENTS OF THE INVENTION

<Overall Configuration >

5 [0008] If lightning strikes around a power line, lightning-induced surge voltage is applied to the power line. The lightning-induced surge voltage generates a voltage of several thousand volts, a current of several hundred to several thousand amperes within a time of several microseconds to 20 microseconds or so, having larger energy than noises or surge voltages generated by other causes. A surge protective
10 apparatus is used for protecting a variety of electrical equipment from the surge voltage. A description will be given hereinbelow of a configuration of a surge protective apparatus according to an embodiment of the present invention, with reference to FIG. 1.

[0009] In FIG. 1, a three-phase four-wire external power supply system 3 includes
15 voltage lines 3R, 3S, 3T for phases R, S, T, respectively, and a neutral line 3N. Note that the nominal phase voltage of "200 V" is assumed in the present embodiment for the external power supply system 3. In a surge protective apparatus 5, voltage lines 2R, 2S, 2T for phases R, S, T, respectively, and a neutral line 2N are arranged, and these are respectively connected to power lines (the voltage lines and the neutral
20 line) 3R, 3S, 3T, 3N in the external power supply system 3. In addition, a ground line 2G in the surge protective apparatus 5 is grounded. A protected device 4 is equipment to be protected from a surge voltage generated in the external power supply system 3, and is connected to power lines 2R, 2S, 2T, 2N in the surge protective apparatus 5. Further, a housing of the protected device 4 is grounded.

25 [0010] In the surge protective apparatus 5, surge absorbing units 60RN, 60SN, 60TN are respectively inserted between the voltage lines 2R, 2S, 2T and the neutral line 2N. In addition, surge absorbing units 60RG, 60SG, 60TG are respectively inserted between the voltage lines 2R, 2S, 2T and the ground line 2G. These surge absorbing units 60RN, 60SN, 60TN, 60RG, 60SG, 60TG have the same circuit
30 configuration, and then are collectively referred to as "surge absorbing units 60." Further, a surge absorbing unit 80 is inserted between the neutral line 2N and the ground line 2G. The surge absorption units 60, 80 are arranged to absorb surge

voltages generated on the power lines 2R, 2S, 2T, 2N to protect the protected equipment 4.

[0011] Modes of the surge voltage can be roughly classified into a "common mode" and a "normal mode." The common mode is a mode in which a surge voltage is generated on the voltage lines 3R, 3S, 3T and the neutral line 3N with comparable waveforms, while the normal mode is a mode in which a particularly high surge voltage is generated only on some of the voltage lines 3R, 3S, 3T and the neutral line 3N. The surge absorbing units 60RG, 60SG, 60TG, 80 are intended to primarily absorb surge voltages in the common mode, while the surge absorbing units 60RN, 60SN, 60TN are intended to primarily absorb surge voltages in the normal mode.

[0012] Additionally, the surge protective apparatus 5 is arranged with a control circuit 50 and a power supply circuit 54 in the control unit supplies power to respective components of the control circuit 50. In addition, a voltage detecting circuit 55 detects phase voltages between the voltage lines 2R, 2S, 2T and neutral 2N, respectively. A logic circuit 56 drives relays arranged in the surge absorbing units 60, 80 (to be described later in detail) via a relay driving circuit 57 according to states of the surge absorbing units 60, 80, to switch ON or OFF-states of respective relay contacts. An external interface 58 outputs a state of the surge protective apparatus 5, for example, to an external monitor device.

[0013] The logic circuit 56 can be configured with a microcomputer inclusive of a CPU (Central Processing Unit) and a memory, however is desirably configured with a logic IC such as a Transistor-Transistor Logic (TTL) or an integrated circuit such as a Field Programmable Gate Array (FPGA) from the viewpoint of preventing runaway, for example, caused by lightning surges.

<Configuration of Surge absorbing unit 60>

[0014] Next, a description will be given of the configuration of the surge absorbing unit 60, with reference to FIG. 2A.

A terminal 60a of the surge absorbing unit 60 is connected to one of the voltage lines 2R, 2S, 2T, and a terminal 60b is connected to the neutral line 2N or the ground line 2G. The surge absorbing unit 60 is arranged with six surge protective devices (SPD). Here, the structure of the SPD 71 will particularly be described in detail. In the SPD71, a thermal fuse 101 and a metal oxide varistor (MOV) 102 are connected in series.

[0015] A photo coupler 104 encloses an LED 104a and a phototransistor 104b. A resistor 103 is connected in series with the LED 104a, and a series circuit composed of the LED104a and the resistor 103 is connected in parallel to MOV 102. Here, when a certain level of voltage is applied to the SPD 71 which is in a normal state, a current flows to the LED 104a via the thermal fuse 101 and the resistor 103 to turn on the LED104a. Thus, the phototransistor 104b is turned on.

[0016] Here, if the MOV 102 has a terminal voltage greater than or equal to its clamping voltage (maximum breakdown voltage), for example, due to a surge voltage, a large current flows through the MOV 102. If such a situation is repeated several times, the MOV 102 will be degraded to have a leakage current gradually increased, and therefore the MOV 102 will generate more heat. Eventually, if the surface temperature of the MOV 102 reaches a reaction temperature of the thermal fuse 101, the thermal fuse 101 fuses. This makes the LED 104a be turned off and the phototransistor 104b be in an OFF-state.

[0017] If the phototransistor 104b is in a OFF-state even when a certain level of voltage is applied to the SPD 71, it means that the MOV 102 has been exhausted and then the thermal fuse 101 has fused. An ON or OFF-state of the phototransistor 104b is outputted as a state signal S71 to the outside. Monitoring the status signal S71 allows for externally detecting that "the SPD 71 has been exhausted and then the thermal fuse 101 has fused."

[0018] Hereinabove, a description has been given in detail of the configuration of the SPD 71, and the other SPDs 72 to 76 are similarly configured. Now, an ON or OFF-state of the phototransistor 104b arranged in the SPDs 72 to 76 will be referred to as "state signals S72 to S76." Here, a relay contact 21 is connected in series with the SPD 71, and a relay contact 20 is connected in parallel to a series circuit composed of the SPD 71 and the relay contact 21. In addition, a relay contact 22 is connected in series with the SPD 72, and this series circuit is connected in parallel to the relay contact 20. Relay contacts 23 to 26 are connected in series with the SPDs 73 to 76, respectively, and these series circuits are mutually connected in parallel.

[0019] ON or OFF-states of the relay contacts 20 to 26 in FIG. 2A are those in the initial state. That is, the relay contacts 20, 21, 23 are in an ON-state, and all the other relay contacts 22, 24 to 26 are in an OFF-state. Accordingly, in the initial state, a voltage across the terminals 60a, 60b is applied only across both ends of the SPD

73, and not applied to the other SPDs 71, 72, 74 to 76. As described above, the nominal phase voltage of the external power supply system 3 is "200 V" and, assuming that the voltage variation in the normal state is within a range of $\pm 10\%$, the maximum voltage in the normal state is "220 V." As this "220 V" is the effective value, the peak wave-height value of the voltage is $\sqrt{2}$ times the value: i.e., "311 V."

[0020] The MOV 102 built in the SPD 73 has a clamping voltage V_{C1} that allows a slight margin for this wave-height value of "311V" (i.e., 340 V), and then a breakdown does not occur within a range of normal voltage variations. The SPD 74, 75, or 76 is intended to be used in place of the SPD 73 when the SPD 73 is exhausted (details will be described later), and therefore the clamping voltage of the MOV 102 built in them is equally V_{C1} (i.e., 340 V).

[0021] Further, the SPDs 71, 72 are connected in series with one of the SPDs 73 to 76 when an overvoltage exceeding the normal range of voltage variations ($\pm 10\%$) occurs. A voltage across the terminals 60a, 60b is detected by the voltage detecting circuit 55 (see FIG. 1) for determining in the logic circuit 56 whether the overvoltage has occurred, and if it is determined that the overvoltage has occurred, the relay contact 20 is turned off. This causes a state in which the SPD 71 and one of the SPDs 73 to 76 are connected in series.

[0022] Furthermore, if the SPD 71 has been exhausted, the relay contact 22 is made in an ON-state, and the SPD 72 is used in place of the SPD 71. The MOVs 102 having a clamp voltage V_{C2} (i.e., 150 V) are used in the SPDs 71, 72, and then the total clamping voltage ($V_{C1} + V_{C2}$) amounts to "490 V" because one of the SPD 71, 72 are connected in series with one of the SPDs 73 to 76.

<Configuration of Surge absorbing unit 80>

[0023] Next, a description will be given of a configuration of the surge absorbing unit 80 that is connected between the neutral line 2N and the ground line 2G, with reference to FIG. 2B. A terminal 80a of the surge absorbing unit 80 is connected to the neutral line 2N, and a terminal 80b is connected to the ground line 2G. An SPD 83 is connected between the terminals 80a, 80b. Additionally, relay contacts 43 to 46 are connected in series with SPDs 83 to 86, respectively, and these series circuits are mutually connected in parallel. The MOVs 102 having the clamping voltage V_{C1} (i.e., 340 V) are used in the SPDs 83 to 86, as is the case with the SPDs 73 to 76 described above. In the initial state (the state shown in the drawing), only the relay

contact 43 is in an ON-state, and the other relay contacts 44 to 46 are in an OFF-state.

<Switching operation in SPD>

[0024] In each of the surge absorbing units 60, 80, if a state of the internal SPDs 71 to 76, 83 to 86 (state signals S71 to S76, S83 to S86) is detected, an ON or OFF state of the relay contacts 22 to 26, 43 to 46 in each of the surge absorbing units 60, 80 is switched under the control of the logic circuit 56 and the relay driving circuit 57. This process will be described below with reference to FIG. 3.

[0025] In FIG. 3, for the surge absorbing units 60, state signals S71 to S76 in 60RN, 60SN are shown, but state signals S71 to S76 in the other surge absorbing units 60TN, 60RG, 60SG, 60TG are not shown because they have the same waveforms. States of the relay contacts 22 to 26 in each of the surge absorbing units 60 is also made to be in common, and states of the relay contacts 43 to 46 in the surge absorbing unit 80 is also made to be in common with the states of the relay contacts 23 to 26.

[0026] Prior to time t41, the state signals S73, S83 in all the surge absorbing units 60, 80 are in an ON-state. On the other hand, at time t41, the state signal S73 is in an OFF-state, because the SPD 73 for the normal voltage in the surge absorbing unit 60RN has been exhausted and then the thermal fuse 101 therein has fused.

Upon detecting that the state signals S73, S83 in some of the surge absorbing units 60, 80 has been changed to an OFF-state, the logic circuit 56, via the relay driving circuit 57, sets the relay contacts 23, 43 in all the surge absorbing units 60, 80 to an OFF-state, and sets the relay contacts 24, 44 in all the surge absorbing units 60, 80 to an ON-state.

[0027] If the relay contacts 23, 43 are made to be in an OFF-state, the LEDs 104a in the SPDs 73, 83 are turned off to make the state signals S73, S83 be turned off in all the surge absorbing units 60, 80. This causes all the status signals S73, S83 to have the same waveform, as shown in FIG. 3. Note that there is some delay in time after the state signal S73 of the surge absorbing unit 60RN has first been made to be in an OFF-state due to the exhaustion of the MOV 102 until the state signals S73, S83 in the other surge absorbing units 60, 80 are made to be in an OFF-state, however this delay in time is not shown in FIG. 3. In addition, at time t41, the relay contacts 24, 44 are made to be in an ON-state to allow the SPDs 74, 84 to be ready

to absorb a surge voltage. Further, a certain level of voltage is applied across both ends of the SPDs 74, 84 to make the LEDs 104a in the SPDs 74, 84 light and to make the state signals S74, S84 be in an ON-state.

[0028] Next, at time t42, the state signal S74 is made to be in an OFF-state

5 because the SPD 74 for the normal voltage in the surge absorbing unit 60SN has been exhausted and then the thermal fuse 101 therein has fused. Upon detecting that the state signals S74, S84 has been made to be in an OFF state in some of the surge absorbing units 60, 80, the logic circuit 56, via the relay driving circuit 57, sets the relay contacts 24, 44 in all the surge absorbing units 60, 80 to an OFF-state and

10 sets the relay contacts 25, 45 in all the surge absorbing units 60, 80 to an ON-state.

[0029] If the relay contacts 24, 44 are made to be in an OFF-state, the LEDs 104a in the SPDs 74,84 are turned off to make the state signals S74, S84 in all the surge absorbing units 60, 80 be in an OFF-state. In addition, if the relay contacts 25, 45 are made to be in an ON-state, the SPDs 75, 85 are made to be ready to absorb a surge

15 voltage in all the surge absorbing units 60, 80 to make the status signals S75, S85 be in an ON-state.

[0030] Next, at time t43, the SPD 71 is in an OFF-state because the SPD 71 for overvoltage in the surge absorbing unit 60SN has been exhausted and then the thermal fuse 101 therein has fused. Upon detecting that the state signal S71 in some

20 of the surge absorbing units 60 being in an OFF-state, the logic circuit 56 sets the relay contacts 21 in all the surge absorbing units 60 in an OFF-state via the relay driving circuit 57, as well as sets the relay contacts 22 in all the surge absorbing units 60 to an ON-state.

[0031] If the relay contact 21 is in an OFF-state, the LED 104a in the SPD 71 is

25 turned off to make the state signal S71 be in an OFF-state. In addition, if the relay contact 22 is set to the ON-state, the SPD 72 becomes ready to absorb a surge voltage in each of the surge absorbing units 60 to make the state signal S72 be in an ON-state. Note that the values of the status signals S71, S72 in FIG. 3 indicate those when assumed that the overvoltage condition has occurred (the relay contact 20 is

30 in an OFF-state and a certain level of voltage is applied across the SPDs 71, 72). If no overvoltage has occurred, the relay contact 20 is in an ON-state to make the state signals S71, S72 be always in an OFF-state, regardless of the state of the relay contacts 21, 22.

[0032] Next, at time t44, the SPD 85 in the surge absorbing unit 80 has been exhausted and then the thermal fuse 101 therein has fused to make the state signal S85 be in an OFF-state. Upon detecting that the state signals S75, S85 in some of the surge absorbing units 60, 80 is in an OFF-state, the logic circuit 56 sets the relay contacts 25, 45 in all the surge absorbing units 60, 80 to an OFF-state via the relay driving circuit 57, as well as sets the relay contacts 26, 46 in all the surge absorbing units 60, 80 to an ON-state.

[0033] If the relay contacts 25, 45 are in an OFF-state, the LEDs 104a in the SPDs 75, 85 are turned off to make the state signals S75, S85 be in an OFF-state in all the surge absorbing units 60, 80. In addition, if the relay contacts 26, 46 are set to the ON-state, the SPDs 76, 86 become ready to absorb a surge voltage in all the surge absorbing units 60, 80 to make the status signals S76, S86 be in an ON-state.

[0034] Next, at time t45, the SPD 76 in the surge absorbing unit 60SN and the surge absorbing unit 80 have been exhausted and the thermal fuse 101 therein has fused to make the state signal S76 be in an OFF-state. However, at this stage, the last SPDs 76, 86 for a normal voltage are used in all the surge absorbing units 60, 80, to keep the state of the relay contacts 21 to 26, 43 to 46 unchanged and the state signal S76, S86 in the ON-state in the surge absorbing units 60, 80 other than the surge absorbing unit 60SN.

[0035] In the lower part of FIG. 3, status signals ST21 to ST24 are those outputted, based on the state signals S71 to S76 described above, from the logic circuit 56 (see FIG. 1) via an external interface 58 to an external monitor device or the like as alarm signals or pilot lamp signals. First, the status signal ST21 is a signal to be in an ON-state on the condition that the status signals S73, S83 of the SPDs 73, 83 for the normal voltage to be used in the initial stage are in an ON-state in all the surge absorbing units 60, 80 and no exhaustion of the SPD 71 for overvoltage is detected in any of the surge absorbing units 60. Therefore, the status signal ST21 being in the ON-state means that all the SPDs in all the surge absorbing units 60, 80 are normal. In the example in FIG. 3, the states prior to time t41 fall into this status.

[0036] In addition, the status signal ST22 is a signal to be in an ON-state when both the condition "exhaustion of the SPD 71 has been detected in some of the surge absorbing units 60, or the state signal S73 has been in an OFF-state" and the condition "no error of the SPD 72 is detected in any of the surge absorbing units 60,

and the state signals S74, S84 or S75, S85 are in an ON-state" are satisfied.

Therefore, the status signal ST22 being in the ON-state means that some of the SPDs are exhausted, but at least "two" SPDs for the normal voltage and at least "one" SPD for overvoltage remain normal.

5 **[0037]** This means that there is enough life remaining for all the surge absorbing units 60, 80, and if a user of the surge protective apparatus 5 requests a supplier of the surge protective apparatus 5 at that point in time for taking an action, the supplier can replace or maintain the surge absorbing units 60, 80 in a planned manner with a temporal margin. In the example in FIG. 3, the states between time t41 and t44 fall
10 into this status.

[0038] Further, the status signal ST23 is in an ON-state when the condition "the state signals S75, S85 are in an OFF-state and the state signals S76, S86 are in an ON-state in all the surge absorbing units 60, 80, and no error of the SPD 72 is detected in any of the surge absorbing units 60" is satisfied. The status signal ST23
15 being in an ON-state means "three of the four SPDs 73 to 76 for the normal voltage have been exhausted," and the remaining life of the surge absorbing units 60, 80 has been reduced to "1/4" of that in the initial stage. This indicates that the surge absorbing units 60, 80 are desired to be quickly exchanged or repaired. In the example in FIG. 3, the states between time t44 and t45 fall into this status.

20 **[0039]** Furthermore, the status signals ST24 is in an ON-state if exhaustion of any of the SPDs 72, 76, 86 is detected in any of the surge absorption section 60, 80. This state means that the last SPD 72 for overvoltage or the last SPD 76 for the normal voltage is exhausted in one of the surge absorbing units 60, 80, and indicates that the subject surge absorbing unit 60 or 80 is functionally in significant degradation, or
25 not functioning at all. This is a situation where the subject surge absorbing unit 60 or 80 is desired to be urgently exchanged or repaired, and the states after time t45 fall into this status in FIG. 3. Note that even if one of the surge absorbing units 60 does not function at all, it does not mean that the surge protective apparatus 5 does "not function at all." That is, even if one of the surge absorbing units 60 has lost its
30 function at all, the other surge absorbing unit 60 can compensate for the function to some extent.

<State transition of Logic circuit 56>

[0040] The logic circuit 56 transitions its internal state in order to achieve the switching operation of the SPD as described above. The state transition of the logic circuit 56 will be explained in detail with reference to FIG. 4.

In FIG. 4, the current internal state is assumed to be an idle/initial state SS00.

Here, if power-on operation or reset operation is made, all the surge absorbing units 60, 80 are checked whether all the SPDs therein are normal. That is, when the relay contacts 21 to 26, 43 to 46 are switched as appropriate to apply a certain level of voltage across both ends of a SPD, and if the SPD outputs a state signal of an ON-state, the SPD is determined to be normal.

[0041] In this way, if all the SPDs in all the surge absorbing units 60, 80 are determined to be normal, the internal state of the logic circuit 56 transitions to a first-bank operating state SS10. Here, a "first bank" collectively refers to the SPDs 73, 83 for the normal voltage to be used in the first sequence in each of the surge absorbing units 60, 80. In the first-bank operating state SS10, if no exhaustion of the SPD 71 for overvoltage is detected, the status signal ST21 in the ON-state is outputted to the external monitor device or the like, as described above. In the first-bank operating state SS10, the state signals S73, S83 of the SPDs 73, 83 are normally in an ON-state, but if any of the state signals S73, S83 is in an OFF-state, the logic circuit 56 determines that this indicates a "failure in the first bank," to make the internal state transition to a "waiting-for-stabilization-of-second-bank state SS21."

[0042] A "second bank" collectively refers to the SPDs 74, 84 for the normal voltage to be used in the second sequence in each of the surge absorbing units 60, 80. The waiting-for-stabilization-of-second-bank state SS21 corresponds to the state of various relay contacts being switched at time t41 in FIG. 3. Switching a relay contact requires a certain amount of time. In addition, even if a voltage is applied across both ends of an SPD as a result of switching the relay contact, a certain amount of time is again required until the LED 104a in the SPD emits light to output a state signal of an ON-state.

[0043] For this reason, the logic circuit 56 uses a timer to hold the determination of the state signal until a predetermined time elapses, and after then to make the internal state transition to a "second-bank operating state SS22." In the second-bank operating state SS22, the status signals S74, S84 of each of the SPDs 74, 84 are normally in an ON-state, but if any of the state signals S74, S84 is in an OFF-state,

the logic circuit 56 determines that this indicates a "failure in the second bank," to make the internal state transition to a "waiting-for-stabilization-of-third-bank state SS31."

[0044] A "third bank" collectively refers to the SPDs 75, 85 for the normal voltage to be used in the third sequence in each of the surge absorbing units 60, 80. The waiting-for-stabilization-of-third-bank state SS31 corresponds to the state of various relay contacts being switched at time t42 in FIG. 3. After a predetermined time has elapsed, the logic circuit 56 makes the internal state transition to a "third-bank operating state SS32." In the second-bank operating state SS22 or the third-bank operating state SS32, the status signal ST22 of an ON-state is outputted to the external monitor device or the like as described above, as long as the exhaustion of the last SPD 72 for overvoltage has not been detected.

[0045] In the third-bank operating state SS32, the status signals S75, S85 of the SPDs 75, 85 are normally in an ON-state, but if one of the status signals S75, S85 is in an OFF-state, the logic circuit 56 determines that this indicates a "failure in the third bank," to make the internal state transition to a "waiting-for-stabilization-of-fourth-bank state SS41."

[0046] A "fourth bank" collectively refers to the SPDs 76, 86 for the normal voltage to be used last in each of the surge absorbing units 60, 80. The waiting-for-stabilization-of-fourth-bank state SS41 corresponds to the state of various relay contacts being switched at time t44 in FIG. 3. After a predetermined time has elapsed, the logic circuit 56 makes the internal state transition to a "fourth-bank operating state SS42." Here, the status signal ST23 of an ON-state is outputted to the external monitor device or the like, as described above, as long as the exhaustion of the last SPD 72 for overvoltage has not been detected.

[0047] In the fourth-bank operating state SS42, the state signals S76, S86 of the SPDs 76, 86 are normally in an ON-state, but if one of the state signals S76, S86 is in an OFF-state, the logic circuit 56 determines that this indicates a "failure in the fourth bank," to make the internal state transition to a "all-banks-in-failure state SS50." This corresponds to the state after time t45 in FIG. 3, and the status signal ST24 of an ON-state is outputted to the external monitor device or the like, as described above.

[0048] If the surge protective apparatus 5 is powered off in the all-banks-in-failure state SS50 or in the preceding state, the surge absorbing units 60, 80 can be exchanged or repaired. Powering on or resetting the surge protective apparatus 5 after the maintenance causes the internal state to return to the idle/initial state SS00.

5 <Comparative Example>

[0049] For describing advantageous effects of the present embodiment, a reference will be made to a comparative example and its configuration is as follows.

The comparative example described herein is configured to add a means for directly detecting a failure in an open mode into the configuration of the embodiment
10 described above. As described in the "Summary of the Invention," an exhausted condition that can be detected from the outside through a state signal (e.g., S71) is referred to as the "short mode." On the other hand, a failure in the "open mode" may occur if an immense surge current momentarily flows in the MOV 102. That is, if the MOV 102 bursts to be in an open state before the thermal fuse 101 fuses, the LED
15 104a continues to light and this inhibits a failure in the open mode from being detected through the state signal (e.g., S71).

[0050] One of possible ways of detecting a failure in the open mode is to connect a shunt resistor in series with MOV 102. As a leakage current of several milliamperes to several ten milliamperes flows through the MOV 102, even if it is a new one, a
20 failure in the open mode can be detected through the terminal voltage of the shunt resistor. However, a surge current of several thousand amperes may momentarily flow in the MOV 102 in some cases, and this causes a problem that a voltage drop across the shunt resistor may degrade surge protection capability.

[0051] On the other hand, a shunt resistor having a very low resistance value (e.g.,
25 0.01 Ω or less) has been put to practical use, but, when used in an environment for controlling an AC voltage of several hundred volts, as is the case with the present embodiment, noises can easily be superimposed onto a voltage to be detected. With a remedy additionally included for eliminating the noises, using a shunt resistor leads to cost increase.

30 **[0052]** Alternatively, a Hall element or the like may be used to measure a leakage current flowing through the MOV 102 in a contactless manner. However, as the Hall element or the like is expensive, this also leads to cost increase. As discussed above, an attempt to directly detect a failure in the open mode using techniques currently

available inevitably leads to cost increase, and therefore employing such a technique on an inexpensive product has less feasibility.

<Advantageous Effects of Embodiment>

[0053] As described above, the surge protective apparatus (surge-voltage

5 absorbing apparatus) 5 of the present embodiment includes:

a) a group of surge absorbing units (60RN, 60SN, 60TN, 60RG, 60SG, 60TG, 80) having at least three surge absorbing units (60, 80) for use in a three-phase voltage system, each of the surge absorbing units (60, 80) having:

10 a first surge-voltage absorbing circuit (73 or 83) that includes a first surge-voltage absorbing element (102 in the SPDs 73, 83) which is in a conducting state when a voltage across both ends of the first surge-voltage absorbing element is equal to or higher than a predetermined voltage, and is inserted between two lines where a surge voltage can occur;

15 a second surge-voltage absorbing circuit (74 or 84) that includes a second surge-voltage absorbing element (102 in the SPD 74, 84) which is in a conducting state when a voltage across both ends of the second surge-voltage absorbing element is equal to or higher than a predetermined voltage, and is inserted between the two lines;

20 a first relay contact (23 or 43) that inserts the first surge-voltage absorbing circuit (73 or 83) between the two lines when the first relay contact is in an ON-state; and

a second relay contact (24 or 44) that inserts the second surge-voltage absorbing circuit (74 or 84) between the two lines when the second relay contact is in an ON-state; and

25 b) a control circuit (50) that sets the second relay contact (24 or 44) in each of the surge absorbing units (60, 80) to an OFF-state until detecting the first surge-voltage absorbing circuit (73 or 83) being in an exhausted condition, and sets the second relay contact (24 or 44) in each of the surge absorbing units (60, 80) to an ON-state upon detecting the first surge-voltage absorbing circuit (73 or 83) being in an exhausted condition.

30 **[0054]** In addition, the control circuit (50) sets the first relay contact (23 or 43) in each of the surge absorbing units (60, 80) to an ON-state until detecting the first surge-voltage absorbing circuit (73 or 83) being in an exhausted condition, and sets the first relay contact (23 or 43) in each of the surge absorbing units (60, 80) to an

OFF-state upon detecting an exhausted condition in the first surge-voltage absorbing circuit (73 or 83).

[0055] Further, the surge protective apparatus 5 further includes voltage lines for three phases (2R, 2S, 2T) and a neutral line (2N), wherein the group of surge absorbing units (60RN, 60SN, 60TN, 60RG, 60SG, 60TG, 80) includes three voltage-line-to-neutral-line surge absorbing units (60RN, 60SN, 60TN) that are respectively inserted between the voltage lines for three phases (2R, 2S, 2T) and the neutral line (2N).

[0056] Furthermore, the group of surge absorbing units (60RN, 60SN, 60TN, 60RG, 60SG, 60TG, 80) includes a neutral-line-to-ground-potential surge absorbing unit (80) that is inserted between the neutral line (2N) and a ground potential conductor (2G).

[0057] Moreover, the group of surge absorbing units (60RN, 60SN, 60TN, 60RG, 60SG, 60TG, 80) includes three voltage-line-to-ground-potential surge absorbing units (60RG, 60SG, 60TG) that are respectively inserted between the voltage lines for three-phases (2R, 2S, 2T) and the ground potential conductor (2G).

[0058] Still moreover, the first and second surge-voltage absorbing circuits (73, 74, 83, 84) respectively output state signals (S73, S74, S83, S84), each indicating whether or not each of the surge absorbing units (73, 74, 83, 84) is exhausted, and the control circuit (50) outputs status signals (ST21 to ST24), as monitoring signals, which are combinations of the state signals (S73, S74, S83, S84) that are outputted from each surge absorbing unit constituting the group of surge absorbing units (60RN, 60SN, 60TN, 60RG, 60SG, 60TG, 80).

[0059] With this configuration, the present embodiment allows for reacting to a failure in the open mode, without directly detecting the failure in the open mode. The reason will be described below.

As described above, modes of the surge voltage is roughly classified into the “common mode” (where a surge voltage is generated on the voltage lines 3R, 3S, 3T and the neutral line 3N with the comparable waveforms) and the “normal mode” (where a particularly high surge voltage is generated only on some of the voltage lines 3R, 3S, 3T and the neutral line 3N).

[0060] A failure in the open mode is caused, for example, by lightning directly striking equipment or by induced lightning around the equipment, and a surge

voltage in such a case is often generated in the "normal mode." That is, a particularly high surge voltage is generated in some of the phases to cause one or more MOVs 102 in charge burst instantaneously. On the other hand, a fairly high surge voltage may often be generated in other phases due to induced lightning, even though it may not be high enough to cause the MOV(s) 102 to burst instantaneously. Then, the deterioration of the MOV(s) 102 is accelerated to cause the MOV(s) 102 to more likely be exhausted in a short mode within a relatively short time.

[0061] In the present embodiment, the SPDs are switched bank by bank and then, if one of the SPDs belonging to a certain bank is exhausted, the other SPDs belonging to the same bank are also disconnected from the circuit at the same time. Therefore, under a situation where one or more SPDs fail in the open mode, if other SPD(s) belonging to the same bank is/are exhausted in the short mode, the one or more SPDs that have failed in the open mode are also disconnected from the circuit. In this way, even if a failure in the open mode has not directly been detected, detecting the other phases being exhausted in the short mode consequently allows for effectively reacting to a failure in the open mode.

[0062] Note that the probability of surge voltages at a level of causing a failure in the open mode being generated on the voltage lines 3R, 3S, 3T and the neutral line 3N at the same time may not be zero. Also, it is not safe to say that there is no case where a surge voltage is generated in one phase at a level of causing a failure in the open mode while it gives almost no damage to the MOVs 102 for the other phases. However, the probability of having such a situation is very low to allow the present embodiment to effectively react to a failure in the open mode in the majority of cases.

<Modifications>

[0063] The present invention is not limited to the embodiments described above, and various modifications are possible. The embodiments described above are those shown as examples for comprehensibly describing the present invention and the present invention is not necessarily limited to those including all configurations as described above. In addition, a part of the configuration of an embodiment can be replaced with the configuration of another embodiment, and also the configuration of one embodiment can be added to the configuration of the other embodiment. Further, a part of the configuration of each embodiment can be deleted, or added/replaced

with other configuration. Possible modifications with respect to the above-mentioned embodiment are, for example, as follows.

[Modification of SPD]

[0064] 1) In the embodiment described above, the SPDs 71 to 76, 83 to 86 shown in FIGS. 2A, 2B are used, but an SPD 11 shown in FIG. 5 may be used instead of them.

In FIG. 5, a micro switch 110 is a switch that switches according to the state of the thermal fuse 101, and includes a common terminal 110b, a terminal 110a that is connected to the common terminal 110b when the thermal fuse 101 does not fuse, and a terminal 110c that is connected to the common terminal 110b when the thermal fuse 101 has fused. Assuming that a contact signal indicative of a connection state between the terminal 110a and the common terminal 110b is outputted as a state signal S11, the state signal S11 is in an ON-state in the initial state, as shown in the figure.

[0065] The state signal S11 is outputted regardless of whether a voltage is applied across both ends of the SPD 11, and this point is different from the state signals (e.g., S71) in the embodiment described above. However, the state signals S11 can be used in place of the state signal S71 to S76, S83 to S86 by accommodating the configuration of the logic circuit 56 thereto.

[0066] 2) The SPD 71 or the like in the embodiment described above includes therein the photo coupler 104, but an SPD is also popular that does not include the photo coupler 104 but uses a connection point between the MOV 102 and the thermal fuse 101 as an intermediate terminal for monitoring to output a state signal. Such kind of SPDs may be used instead of the SPD71 to 76, 83 to 86 in the embodiment described above to separately connect photo couplers to the intermediate terminal for monitoring.

[Modification on number of surge absorbing units 60, 80]

[0067] In the embodiment described above, the surge absorbing units 60RG, 60SG, 60TG, 80, which primarily react to a surge voltage in the common mode, and the surge absorbing units 60RN, 60SN, 60TN, which primarily react to a surge voltage in the normal mode, are arranged to have seven surge absorbing units 60, 80 in total, but some of these surge absorbing units may be omitted to reduce a cost.

[0068] For example, if the neutral line 3N in the external power supply system 3 is grounded in the vicinity of the surge protective apparatus 5, a surge voltage applied to the neutral line 3N, 2N can be expected to be small. In such a case, the surge absorbing unit 80 may be omitted. In addition, if the apparatus is intended in particular to react to surge voltages in the “normal mode”, the surge absorbing units 60RG, 60SG, 60TG may be omitted. Conversely, if the apparatus is intended in particular to react to surge voltages in the “common mode”, the surge absorbing units 60RN, 60SN, 60TN may be omitted.

[Modification of power distribution system]

[0069] In the embodiment described above, a description has been given of an example that uses the three-phase four-wire power distribution system, but other distribution systems may also be employed. For example, in Japan, a three-phase three-wire system having the S-phase grounded is frequently used. In this case, a surge absorbing unit between the R-phase and the S-phase (ground) and a surge absorbing unit between the T-phase and the S-phase (ground) may be provided.

[Modification of status signal]

[0070] In the embodiment described above, the state signals S71 to S76, S83 to S86 outputted from the SPDs 71 to 76, 83 to 86 are combined to output status signals ST21 to ST24 to an external monitor device or the like. However, the way of combining the state signals is not limited to that used in the embodiment described above, and a variety of ways can be used. For example, in the embodiment described above, the second-bank operating state SS22 and the third-bank operating state SS32 are expressed by using the same status signal (ST22 in an ON-state), but status signals may be outputted that allow for distinguishing the two.

[Modification of arrangement of surge protective apparatus 5]

[0071] In the embodiment described above, the surge protective apparatus 5 is inserted between the external power supply system 3 and the protected device 4, but if the protected device 4 consumes large amount of power, the surge protective apparatus 5 may sometimes lead to a larger size and a higher cost. In such a case, the protected device 4 and the surge protective apparatus 5 may be connected in parallel with respect to the external power supply system 3. In particular, in a case where the protected device 4 is an existing facility and the surge protective apparatus 5 is to be added, connecting them in parallel is often desirable.

DESCRIPTION OF REFERENCE SIGNS

- [0072]** 2R, 2S, 2T Voltage line
- 2G Ground line
- 2N Neutral line
- 5 3 External power supply system
- 3R, 3S, 3T Voltage line
- 3N Neutral line
- 4 Protected device
- 5 Surge protective apparatus (Surge voltage absorbing apparatus)
- 10 11 SPD
- 23, 43 Relay contact (First relay contact)
- 24, 44 Relay contact (Second relay contact)
- 22, 25, 26, 45, 46 Relay contact
- 60, 80 Surge absorbing unit (Group of surge absorbing unit)
- 15 60RG, 60SG, 60TG Surge absorbing unit (Voltage-line-to-ground-potential surge absorbing portion)
- 60RN, 60SN, 60TN Surge absorbing unit (Voltage-line-to-neutral-line surge absorbing unit)
- 73, 83 SPD (First surge-voltage absorbing circuit)
- 20 74, 84 SPD (Second surge-voltage absorbing circuit)
- 71, 72, 75, 76, 85, 86 SPD
- 50 Control circuit
- 54 Power supply circuit
- 55 Voltage detecting circuit
- 25 56 Logic circuit
- 57 Relay driving circuit
- 58 External interface
- 80 Surge absorbing unit (Neutral-line-to-ground-potential surge absorbing unit)
- 101 Thermal fuse
- 30 102 MOV
- 103 Resistor
- 104 Photo coupler
- 104a LED

104b Phototransistor

110 Micro switch

S71to S76 State signal

S83 to S86 State signal

5 ST21 to ST24 Status signal

CLAIMS

1. A surge voltage absorbing apparatus comprising:

a) a group of surge absorbing units having at least three surge absorbing units for use in a three-phase voltage system, each of the surge absorbing units including:

a first surge-voltage absorbing circuit that includes a first surge-voltage absorbing element which is in a conducting state when a voltage across both ends of the first surge-voltage absorbing element is equal to or higher than a predetermined voltage, and is inserted between two lines where a surge voltage can occur;

a second surge-voltage absorbing circuit that includes a second surge-voltage absorbing element which is in a conducting state when a voltage across both ends of the second surge-voltage absorbing element is equal to or higher than the predetermined voltage, and is inserted between the two lines;

a first relay contact that inserts the first surge-voltage absorbing circuit between the two lines when the first relay contact is in an ON-state; and

a second relay contact that inserts the second surge-voltage absorbing circuit between the two lines when the second relay contact is in an ON-state; and

b) a control circuit that sets the second relay contact in each of the surge absorbing units to an OFF-state until detecting the first surge-voltage absorbing circuit being in an exhausted condition, and sets the second relay contact in each of the surge absorbing units to an ON-state upon detecting the first surge-voltage absorbing circuit being in an exhausted condition.

2. The surge voltage absorbing apparatus according to claim 1,

wherein the control circuit sets the first relay contact in each of the surge absorbing units to an ON-state until detecting the first surge-voltage absorbing circuit being in an exhausted condition, and sets the first relay contact in each of the surge absorbing units to an OFF-state upon detecting an exhausted condition in the first surge-voltage absorbing circuit.

3. The surge voltage absorbing apparatus according to claim 1 or 2, further comprising:

voltage lines for three phases; and
a neutral line,

5 wherein the group of surge absorbing units includes three voltage-line-to-neutral-line surge absorbing units that are respectively inserted between the voltage lines for three phases and the neutral line.

4. The surge voltage absorbing apparatus according to claim 3,

10 wherein the group of surge absorbing units includes a neutral-line-to-ground-potential surge absorbing unit that is inserted between the neutral line and a ground potential conductor.

5. The surge voltage absorbing apparatus according to claim 3 or 4,

15 wherein the group of surge absorbing units includes three voltage-line-to-ground-potential surge absorbing units that are respectively inserted between the voltage lines for three phases and the ground potential conductor.

6. The surge voltage absorbing apparatus according to any one of claims 1 to 5,

20 wherein the first and second surge-voltage absorbing circuits respectively output state signals, each indicating whether or not each of the surge absorbing units is exhausted, and the control circuit outputs status signals, as monitoring signals, which are combinations of the state signals that are outputted from each surge absorbing unit constituting the group of surge absorbing units.