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(54) SEMICONDUCTOR STRUCTURES AND METHODS OF MAKING THEM

(71) We, WESTERN ELECTRIC COMPANY, Incorporated of 222 Broadway, New York City, New York State, United States of America, a Corporation organized and existing under the laws of the State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:–

This invention relates to semiconductor structures, to methods of manufacture thereof and to integrated logic circuits incorporating them.

According to one aspect of the present invention, a semiconductor structure includes a semiconductor substrate having an epitaxial layer of one conductivity type thereon, the substrate, or a portion of the substrate adjacent the layer, being of the said one conductivity type but being more heavily doped than the layer, a first region of a conductivity type opposite to that of the layer extending substantially through the layer to the substrate or the said portion thereof and shaped to surround a portion of the layer, another region of the said opposite conductivity type implanted within the surrounded portion of the layer extending laterally to contact the said first region and spaced apart from the surfaces of the layer and at least one metallized contact at the exposed surface of the layer overlying a part of the surrounded region, the surrounded portion forming a transistor.

The vertical three-element semiconductor device formed in the epitaxial layer which preferably overlies a relatively low resistance region of a substrate, is therefore such that the collector and emitter regions thereof extend to respective surfaces of the epitaxial layer and the base region thereof is intermediate the said emitter and collector regions and does not extend to the exposed surface of the epitaxial layer.

Advantageously, pluralities of such devices may be disposed in spaced apart relationship to form logical circuit complexes, and the low resistance region of the substrate can be advantageously utilized to distribute power to the vertical structures. Further, three-element lateral devices, also in the epitaxial layer, can be utilized to connect power to the intermediate elements of the vertical structures without a requirement for metal surface interconnections.

An integrated circuit arrangement may comprise a semiconductor body including a plurality of vertical and lateral transistors serially connected, each of these having the lateral transistor connected to the base of the vertical transistor, an input terminal connected to the lateral transistor and an output terminal connected to a Schottky diode.

According to another aspect of the invention a method of making a semiconductor structure in a semiconductor body formed by an epitaxial layer of one conductivity type upon a substrate or substrate region of the same conductivity type but more heavily doped than the layer comprises forming in the layer a region of opposite conductivity type extending substantially through the layer and surrounding a selected portion of the layer, implanting in said surrounded portion a second region of the said opposite conductivity type spaced apart from the surfaces of the layer but extending laterally to contact said first region so as to form a transistor with the surrounded portion of the layer, and forming a metallized contact on the exposed surface of the layer overlying a part of the surrounded portion.

Advantageously, semiconductor device formed by these steps exhibit a high degree of symmetry of electrical performance because of the symmetry of the impurity

profile of the implanted base region. Accordingly, in the semi-conductor devices so formed, the elements which are at the exposed surface of the epitaxial layer may be utilized as collectors or emitters without penalty of electrical performance. In the event that asymmetry of electrical performance is desirable, it is theoretically possible through successive implants to create the desired asymmetry. However, with successive implants there is a broadening of the base region which may be undesirable.

Because of the symmetry of these vertical three-element devices, it is advantageously possible to create complex logical circuit arrangements wherein the collectors of the devices may be either at the exposed surface of the epitaxial layer or at the surface of the epitaxial layer which lies adjacent to the substrate. Thus, efficient logical circuit arrangements may be fabricated.

In one illustrative embodiment of the invention, an N-type epitaxial layer overlays an N+ substrate and the vertical structures comprising NPN devices are surrounded by corresponding low resistance P-type regions which serve to interconnect the P elements of the vertical structures one to the other and to a signal source.

Advantageously, the three-element vertical structures as described above permit the application of metallized contacts at the surface of the epitaxial layer such that low resistance, ohmic contacts and Schottky diode contacts can be selectively formed.

These vertical three-element semiconductor devices exhibit an improved response time as compared to prior art three-element vertical devices which have their collectors at the exposed epitaxial surfaces. Their response time is improved without an increase in power of the applied signal and their ultimate response time with increased power is less than the response time of prior devices. Furthermore, the possibility of the inclusion of Schottky diode devices at the collectors of these vertical devices reduces the requirement for interconnections in logic circuit complexes and provides for reduced logic signal levels.

The response time of the vertical devices of this invention is improved as a direct result of the impurity profiles of such devices as compared to priorly known double diffused vertical structures. The implanted base of the present invention has a symmetrical impurity profile relative to the emitter and collector regions and this symmetry tends to eliminate the retarding field encountered in double diffused vertical structures which utilize the exposed epitaxial layer as the collector region. Furthermore, the charge in the emitter region of priorly known double diffused vertical structures is substantially higher than the charge in the emitter region of devices, in accordance with the present invention. This reduction in charge also tends to improve the response time of these devices. The collector regions of vertical devices produced by the priorly known double diffusion process have lower resistivity than the collector regions of the vertical devices produced in accordance with the present invention and therefore these prior devices have higher collector to base capacitance which tends to increase their response time.

Although the present invention is illustrated by means of an N-type epitaxial layer overlying an N+ substrate, it should be noted that it is possible to practice this invention through the use of a P-type epitaxial layer overlying a P+ substrate. The resulting PNP vertical structures exhibit longer response times than the corresponding NPN devices of the illustrative example set forth herein because of the inherent lower mobility of holes compared to electrons. Furthermore, the range of metals suitable for producing Schottky diodes at the exposed surface of PNP devices is far more limited.

Figure 1 is a schematic diagram of a prior art device which comprises a multicollector transistor and a three-element lateral current source connected to the base;

Figure 2 is a cross section of a physical embodiment of the prior art circuit of Figure 1;

Figure 3 shows two of the circuit arrangements of Figure 1 in cascade with the addition of a Schottky diode in each of the collectors;

Figure 4 is a cross section of a physical embodiment of the circuit of Figure 3;

Figure 5 shows a layout of a plurality of devices such as shown in Figure 3 and 4 along with the arrangements for the distribution of power and signals;

Figure 6 is a schematic diagram of a variant of the circuit of Figure 3 wherein a single collector is associated with three Schottky barrier diodes;

Figure 7 is a cross section of a physical embodiment of the circuit of Figure 6; and

Figure 8 and 9 are cross sections of a variant of part of the structure of Figure 4 to form isolated transistors.

Logic circuits such as the prior art circuit of Figure 1 and circuits in accordance with the present invention such as those shown in Figure 3 and 6 are typically cascaded in complex arrangements to achieve desired logic functions. Typically, a collector, e.g., A_1 of the circuit of Figure 1, is connected to an input or base terminal A' of a succeeding circuit. The state of conduction of the multiple collector transistor 102 which has the emitter connected to ground, the base connected to the terminal A, and the three col-

lectors connected to the terminals A_1, A_2, and A_3, respectively, is controlled by the state of the circuit or transistor which drives the base of transistor 102 and which would normally be a similar circuit to Figure 1 arranged in cascade. The current source comprises the potential +V and the transistor 101 which is continuously in the conducting state. The current at the collector of the transistor 101 serves to turn on the transistor 102 unless this current is diverted through a lower impedance path so that the potential at the base of the transistor 102 is less than the turnon voltage. Typically, the turnon voltage of the transistor 102 is 0.6 to 0.7 volts. If the driving transistor connected to terminal A in Figure 1 is in the conducting state, the current from the collector of the current source 101 will be diverted through a path which includes the collector to base and base to emitter junctions of the driving transistor to ground. In the conducting state the potential at the collector of the driving transistor would be in the order of 0.05 to 0.1 volts. The magnitude of the voltage drop depends on device construction and can be controlled within reasonable limits during manufacture. Accordingly, the current from the current source 101 will be diverted to ground through the driving transistor and the transistor 102 will be held in the OFF state of conduction.

If the driving transistor is in the nonconducting state, the impedance of the path to ground via the collector to base and base to emitter junctions of that transistor will be extremely high and very little of the current from the current source 101 will be diverted to ground via that path. Accordingly, the current from the current source transistor 101 will flow into the base to emitter junction of the transistor 102 to establish the ON state of conduction of the transistor 102.

In this prior art circuit arrangement which, as stated, may comprise two circuits or stages such as shown in Figure 1 in cascade, the voltage at the node A of the driven transistor varies between approximately 0.05 volts and approximately 0.7 volts. The control which is exerted on the driven transistor 102 is accomplished primarily by steering current between the base to emitter junction of the driven transistor and the collector circuit of the driving transistor. Since it is contemplated that the driving and the driven transistors exist on a single chip wherein there is no significant source of noise, the above-described variation in signal of approximately 600 millivolts at node A is excessive and is incompatible with fast turnon and, to a lesser degree, fast turnoff of the driven transistor.

The time delay in the turnon of the driven transistor is directly proportional to the magnitude of voltage swing at the input, e.g., base of the driven transistor. As explained earlier herein, the speed of operation of devices constructed in accordance with the present invention is a significant improvement over the prior art structures. This, as explained earlier, is because of the improved impurity profiles. An additional improvement in circuit performance can be attributed to the presence of Schottky diodes as shown in the circuit arrangement of Figure 3. In Figure 3 there is shown a driven transistor 302, the current source 301 for the transistor 302, a driving transistor 312, a current source 311 for the driving transistor 312, and a plurality of Schottky diodes, e.g., 313 and 303, disposed in the collector circuits of both the driving and the driven transistors 312 and 302, respectively. As shown in Figure 3, the collector terminal A_1 of the driving transistor 312 is connected to the node A' which is the base terminal of the driven transistor 302. The Schottky diode, 315, typically has a forward threshold voltage drop in the order of 0.4 to 0.5 volts. The magnitude of the voltage drop can be determined and controlled in manufacture. The forward voltage drop of the diode 315, when added to the voltage drop of the driving transistor 312 in the ON state, results in a potential between 0.45 and 0.6 volts. As explained above, the actual voltage drops of the diode and the transistor are controlled by design and through manufacturing control. The maximum potential at node A' is determined by the base to emitter drop of the driven transistor 302 and, as previously indicated, this voltage drop is in the order of 0.7 volts. Accordingly, it is possible that the voltage at node A' can be varied between 0.45 and 0.7 volts to define the OFF and ON states of the driven transistor 302. This swing from 0.45 to 0.7 volts or 250 millivolts is substantially lower than the signal swing in circuits of the prior art shown in Figure 1. Accordingly, the turnon times of driven transistors of the circuit configuration of Figure 3 are substantially lower than the turnon times of circuits of Figure 1. The swing on 250 millivolts is calculated on the basis of minimum voltage drop in the collector circuit of the driving transistor and minimum forward voltage drop of the Schottky diode in the collector of the driving transistor. It is reasonable to expect that in an actual situation the voltage at node A of a driven transistor will be design swing approximately 100 millivolts between an OFF voltage of 0.6 volts and an ON voltage of approximately 0.7 volts. This swing results in a very significant reduction in response time. Accordingly, the circuit arrangement of Figure 3 provides a substantial increase in speed of operation for a given power level and for a given transistor structure.

Logic functions can be implemented by connecting together the collector terminals of two independent stages. Such interconnected transistors serve to provide an AND function. If the two (or more) transistors whose collectors are so connected are both in the nonconducting state, the current from the current source of the driven stage will be steered to turn ON the transistor of the driven stage. However, if either driving transistor is conducting, the driven transistor will be held in the OFF state. As is well known in the prior art, other logic functions, e.g., OR, can be implement through the use of inversion and this basic tying together of collector terminals to form an AND function.

In the circuit arrangement of Figure 3 the transistor 302 is never in the fully nonconducting state. That is, if the voltage at the base terminal thereof is varied typically between 0.6 and 0.7 volts the collector current will vary between a low level of conduction, e.g., 1 or 2 per cent of saturation and a relatively high level current, e.g., one milliamp. Accordingly, s Schottky diode in a collector circuit of the transistor 302, e.g., the diode 305, will for all states of conduction of the transistor be forward biased and there will not be large signal swings at the collector.

The voltage drops associated with the transistors, e.g., 302 and 312, and associated with the Schottky diodes, e.g., 303, 304 and 305, are typical for a particular value of current supplied by the current source transistor 301. The voltage drops in the transistors, e.g., 312, and in the Schottky diodes, e.g., 315, are both related in a similar manner to the magnitude of the current supplied by the transistor 301. If the current from the source 301 is by design or by other circumstances varied within reasonable limits, the voltage drops contributed by the transistor and by the Schottky diodes follow substantially parallel scaling paths. Accordingly, the magnitude of the difference between the ON and OFF voltages at the base of the driven transistor tend to remain constant independently of magnitude of the current supplied by the source 301. Similarly, the voltage drops in the transistor, e.g., 312, and the Schottky diode, e.g., 315, follow substantially parallel scaling paths as a function of change of terperature within reasonable limits. Therefore, for changes of temperature within reasonable limits the circuit arrangement of Figure 3 tends to maintain a constant difference between ON and OFF voltages at the base of transistor 302. As a result, the circuit arrangement of Figure 3 is self-compensating in the presence of reasonable variations in magnitude of current supplied by the current source 301 and compensating for reasonable variations in temperature of the devices.

A physical embodiment of the arrangement of Figure 1 is shown in Figure 2. An N-type epitaxial layer 201 is carried by a lower-resistivity N-type substrate 203. In the epitaxial layer 201 are P-type surface zones 204 and 208 forming respectively the emitter and the collector of transistor 101, the intervening portion of the epitaxial layer forming the base. Diffused N-type zones 205, 206 and 207 within the P-zones 204, form the several collectors of transistor 102, the base and emitter thereof being constituted by P-zone 208 and epitaxial layer 201, respectively. The surface is covered with the usual insulating coating 209 of silicon dioxide, for example, through apertures in which contacts 210, 211, 212, 213 and 214 are made to the various underlying zones.

The elements of a three-element semiconductor device are usually arbitrarily termed the emitter, base and collector in accordance with the best mode of operation of the device. This is in recognition of the fact that three-element semiconductor devices are generally not symmetrical in structure and in electrical behaviour. The usual asymmetry present in a three-element semiconductor device is in the base region of the device and relative doping of collector and emitter. For example, in the prior art structure of Figure 2 the base region 204 is more heavily doped in the portions which are closer to the exposed surface of the epitaxial layer than the portion which lies closer to the substrate 203. Since in the prior art arrangement of Figure 2 the gradient of the impurity in the base region 204 is in the direction of the emitter which is formed of the epitaxial layer 201, this device from a standpoint of accepted terminology is operated in the inverse mode. That is, the geometry of the above-identified regions of Figure 2 and the impurity profiles in those identified regions in Figure 2 are such that electrical performance is better when one of the elements 205, 206, 207 is utilized as an emitter and the portion of the epitaxial layer 201 which forms an active element of the three-element device is utilized as a collector. Thus, in the forward mode of operation of the device of Figure 2, it is possible to have multiple emitters but not multiple collectors as is a requirement for the logic circuits of Figure 1 and 3. Since the device of Figure 2 must be operated in the inverse mode to achieve the circuit arrangement of Figure 1, the electrical performance of that circuit arrangement suffers with respect to gain and response time.

The current source transistor 101 of Figure 1 is comprised in Figure 2 of the P-type emitter region 208, an active base portion of the N-type epitaxial layer 201, and an active collector portion of the P-type region 204.

A side view of a physical realisation of the

current source transistor 301 and the driven transistor 302 of Figure 3, is shown in Figure 4. The embodiment illustrated in Figure 4 utilizes an N-type epitaxial layer 401 overlying an N+ substrate 402. The elements of the side view of Figure 4 can beat be understood by reference to the corresponding top view of Figure 5 and the circuit of Figure 3. The letter labels utilized in the circuit of Figure 3 are consistent with those used in the apparatus drawings of Figure 4 and 5.

In Figure 4, the lateral transistor 311 forming the current source is composed of P-type region 404 forming the emitter, epitaxial region 406 forming the base and P-type region 407 forming the collector. The driven transistor 302 is constituted by the epitaxial region 401 forming emitter regions 402, implanted base regions 408 and N-type collector regions 409 to which metallic contacts are made forming the Schottky diodes.

In the structure of Figure 2, the emitter region 208 of the current source transistor 101 of Figure 1 is surrounded completely by N-type epitaxial material while in the structure of Figure 4 the emitter region 404 of the lateral current source transistor 311 of Figure 3 adjoins the resistive substrate. Since the emitter region 404 is surrounded by N+ material at the substrate and at the upper surface of the epitaxial layer, injection is limited to the lateral N region 406 of the epitaxial layer. This reduces the stored charge in the lateral PNP transistor. Furthermore, the resistive N+ region 405 as shown in Figure 4 enhances the electrical performance of the lateral current source transistor 311 as it tends to prevent recombination of minority carriers at the upper surface and thus increases the gain of the lateral current source transistor.

One possible physical arrangement of a number of multiple collector transistors is shown in Figure 5. In Figure 5 power (+V) is applied at the exposed surface of the epitaxial layer and is distributed by means of P+ channels which are through-extending from the surface of the epitaxial layer to the substrate. Accordingly, the emitters of the lateral current source transistors, e.g., 301 and 311, are interconnected by the P+ channels and a single metallized contact is sufficient for applying power except where additional connections are employed to reduce circuit resistance. Similarly, ground is distributed by means of the N+ substrate which adjoins the emitters, e.g., 402 of Figure 4. As shown in Figure 4 and 5, the base regions of the three vertical transistors of Figure 4 are interconnected by the through-extending P+ channels which surround the vertical transistors. An active portion of this P+ channel comprises the collector of the lateral current transistor and the remainder of the P+ channel serves to interconnect that collector with the base regions of the three vertical transistors of Figure 4 and 5. The transistor configuration shown in Figure 4 may be connected one to the other through metallized surface connections overlying a nonconducting layer, e.g., an oxide layer or may be connected to other devices on or off the chip.

A possible variation of the physical structure of Figure 3, 4 and 5 is shown in Figure 6 and 7. In Figure 6 there is shown a circuit which utilizes a vertical transistor having a single emitter, a single base and a single collector with a plurality of Schottky diodes connected thereto. The transistors 302 and 312 shown in Figure 3 are illustrated as comprising a single emitter and a single base and multiple collectors; however, as shown in Figure 4 there are, in fact, three separate vertical transistors having their emitters and bases interconnected so that these three vertical transistors tend to operate as one. As shown in Figure 7, the circuit of Figure 6 is achieved by means of a single vertical NPN structure having three metallized Schottky contacts to the collector region thereof. In Figure 7 there is shown a lateral current source transistor comprising the emitter 704, the base 706 and a collector which comprises an active portion of the P+ region 717 along with a vertical transistor which comprises collector region 718, implanted base region 719, and emitter region 720. The structure of Figure 7 corresponds to the structure of Figure 4 except for the omission of two of the three vertical structures of Figure 4 and the inclusion of three metallized contacts at the collector region 718. The circuit of Figure 6 exhibits electrical characteristics similar to those of Figure 3.

One possible variation of the basic structure of Figure 4 is illustrated in Figure 8 and 9. In Figure 8 and 9 the three-element vertical transistor is formed over an N+ region which was established in a P-type substrate. An N+ region 830 can be formed in the P-type substrate prior to the time the epitaxial layer is established thereon. For the purpose of this invention, the N+ region 830 performs in the same manner that an N+ substrate such as 403 of Figure 4 performs. In Figure 8 there is shown a single vertical three-element transistor with a Schottky diode contact at the collector while in Figure 9 there is similarly shown a single three-element vertical transistor with an ohmic connection at the surface. In Figure 8 and 9 connection to the emitter is via an ohmic connection at the surface of the epitaxial layer and connection to the base is by an ohmic connection to the through-extending P+ trough surrounding the vertical transistor.

Figure 8 and 9 show that it is possible to

provide isolated devices within a single chip and that connection to such devices can be made through ohmic contacts at the surface of the epitaxial layer.

The structure and the method of this invention can be achieved through readily available technology. That is, standard semiconductor processing steps, e.g., masking, etching, diffusing and ion implantation, are utilized to produce the structures. The method of manufacture set forth herein has been in terms of effect rather than in terms of specific techniques except where the technique is essential to the practice of the invention. For example the base regions of the vertical transistors are formed by ion implantation. The following is a brief discussion of typical steps utilized in the manufacture of the structure of this invention and in the practice of the method of this invention.

The body comprises an N+ substrate (or a P substrate with one or more N+ regions priorly diffused into the P type substrate) and a conventional N-type epitaxial layer overlying the substrate. Conventional masking techniques are utilized to define the locations of the through-extending P+ regions which are subsequently established through standard diffusion techniques. A second masking step is utilized to define the regions where the P-type base zones are to be implanted. Again, conventional methods of masking and of ion implantation are utilized at this point in the process. Following production of the base zones in the vertical transistors a third masking operation is utilized to produce a pattern for a thin N+ layer at selected locations of the surface at which ohmic contact to N-type regions is desired. This thin N+ region can be produced by diffusion or by ion implantation. Subsequently a pattern of contact windows is produced to define the locations at which Schottky diode contacts are to be formed. The devices on the body are subsequently interconnected by a metallization process, (e.g., with aluminium) which is suitable for both the ohmic and the Schottky diode contacts.

WHAT WE CLAIM IS:–

1. A semiconductor structure including a semiconductor substrate having an epitaxial layer of one conductivity type thereon, the substrate, or a portion of the substrate adjacent the layer, being of the said one conductivity type but being more heavily doped than the layer, a first region of a conductivity type opposite to that of the layer extending substantially through the layer to the substrate or the said portion thereof and shaped to surround a portion of the layer, another region of the said opposite conductivity type implanted within the surrounded portion of the layer, extending laterally to contact the said first region and spaced apart from the surfaces of the layer and at least one metallized contact at the exposed surface of the layer overlying a part of the surrounded region, the surrounded portion forming a transistor.

2. A structure according to claim 1 wherein the impurity profile of the said other region is substantially symmetrical relative to the surfaces of the epitaxial layer.

3. A structure according to claim 1 or 2 including a further region of opposite conductivity type extending substantially through the said layer, spaced apart from the said first region and forming with that region and the intervening portion of the layer a lateral transistor.

4. A structure according to claim 3 including an ohmic region of said one conductivity type at the exposed surface of the layer between first and said further regions.

5. A structure according to any one of claims 1 to 4 wherein the metallized contact or contacts form Schottky barrier contacts.

6. A structure according to any preceding claim wherein the epitaxial layer is of N-type conductivity.

7. A semiconductor integrated circuit arrangement comprising a semiconductor body including a plurality of structures according to claim 5 when appended to claim 3 or 4 connected in series, each of these structures thus comprising a vertical transistor with a lateral current source transistor connected to its base, an input terminal connected to the lateral current source transistor and an output terminal connected to a Schottky diode.

8. A semiconductor integrated circuit arrangement according to claim 7 wherein each vertical transistor is formed from a plurality of three element surrounded portions having their base regions connected together, their emitter regions connected together and individual Schottky diode connections.

9. A method of making a semiconductor structure in a semiconductor body formed by an epitaxial layer of one conductivity type upon a substrate or substrate region of the same conductivity type but more heavily doped than the layer comprising forming in the layer a region of opposite conductivity type extending substantially through the layer and surrounding a selected portion of the layer, implanting in said surrounded portion a second region of the said opposite conductivity type spaced apart from the surfaces of the layer but extending laterally to contact said first region so as to form a transistor with the surrounded portion of the layer, and forming a metallized contact on the exposed surface of the layer overlying a part of the surrounded portion.

10. A method according to claim 9 including forming in the layer a further region of said opposite conductivity type

provide isolated devices within a single chip and that connection to such devices can be made through ohmic contacts at the surface of the epitaxial layer.

The structure and the method of this invention can be achieved through readily available technology. That is, standard semiconductor processing steps, e.g., masking, etching, diffusing and ion implantation, are utilized to produce the structures. The method of manufacture set forth herein has been in terms of effect rather than in terms of specific techniques except where the technique is essential to the practice of the invention. For example the base regions of the vertical transistors are formed by ion implantation. The following is a brief discussion of typical steps utilized in the manufacture of the structure of this invention and in the practice of the method of this invention.

The body comprises an N+ substrate (or a P substrate with one or more N+ regions priorly diffused into the P type substrate) and a conventional N-type epitaxial layer overlying the substrate. Conventional masking techniques are utilized to define the locations of the through-extending P+ regions which are subsequently established through standard diffusion techniques. A second masking step is utilized to define the regions where the P-type base zones are to be implanted. Again, conventional methods of masking and of ion implantation are utilized at this point in the process. Following production of the base zones in the vertical transistors a third masking operation is utilized to produce a pattern for a thin N+ layer at selected locations of the surface at which ohmic contact to N-type regions is desired. This thin N+ region can be produced by diffusion or by ion implantation. Subsequently a pattern of contact windows is produced to define the locations at which Schottky diode contacts are to be formed. The devices on the body are subsequently interconnected by a metallization process, (e.g., with aluminium) which is suitable for both the ohmic and the Schottky diode contacts.

WHAT WE CLAIM IS:–

1. A semiconductor structure including a semiconductor substrate having an epitaxial layer of one conductivity type thereon, the substrate, or a portion of the substrate adjacent the layer, being of the said one conductivity type but being more heavily doped than the layer, a first region of a conductivity type opposite to that of the layer extending substantially through the layer to the substrate or the said portion thereof and shaped to surround a portion of the layer, another region of the said opposite conductivity type implanted within the surrounded portion of the layer, extending laterally to contact the said first region and spaced apart from the surfaces of the layer and at least one metallized contact at the exposed surface of the layer overlying a part of the surrounded region, the surrounded portion forming a transistor.

2. A structure according to claim 1 wherein the impurity profile of the said other region is substantially symmetrical relative to the surfaces of the epitaxial layer.

3. A structure according to claim 1 or 2 including a further region of opposite conductivity type extending substantially through the said layer, spaced apart from the said first region and forming with that region and the intervening portion of the layer a lateral transistor.

4. A structure according to claim 3 including an ohmic region of said one conductivity type at the exposed surface of the layer between first and said further regions.

5. A structure according to any one of claims 1 to 4 wherein the metallized contact or contacts form Schottky barrier contacts.

6. A structure according to any preceding claim wherein the epitaxial layer is of N-type conductivity.

7. A semiconductor integrated circuit arrangement comprising a semiconductor body including a plurality of structures according to claim 5 when appended to claim 3 or 4 connected in series, each of these structures thus comprising a vertical transistor with a lateral current source transistor connected to its base, an input terminal connected to the lateral current source transistor and an output terminal connected to a Schottky diode.

8. A semiconductor integrated circuit arrangement according to claim 7 wherein each vertical transistor is formed from a plurality of three element surrounded portions having their base regions connected together, their emitter regions connected together and individual Schottky diode connections.

9. A method of making a semiconductor structure in a semiconductor body formed by an epitaxial layer of one conductivity type upon a substrate or substrate region of the same conductivity type but more heavily doped than the layer comprising forming in the layer a region of opposite conductivity type extending substantially through the layer and surrounding a selected portion of the layer, implanting in said surrounded portion a second region of the said opposite conductivity type spaced apart from the surfaces of the layer but extending laterally to contact said first region so as to form a transistor with the surrounded portion of the layer, and forming a metallized contact on the exposed surface of the layer overlying a part of the surrounded portion.

10. A method according to claim 9 including forming in the layer a further region of said opposite conductivity type

extending substantially through the layer spaced apart from said first region and forming with that region and the intervening portion of the layer a laterally arranged three-zone semiconductor device.

11. A method according to claim 10 including forming an ohmic region of the said one conductivity type at the exposed surface of the layer between the first and further regions.

12. A method according to claim 9, 10 or 11 wherein the epitaxial layer is of N type material and the substrate region is of N+ material.

13. A method according to any one of claims 9 to 12 including forming the metallized contact so as to make a Schottky barrier contact.

14. A method according to claim 9 or 10 including forming a plurality of surrounded regions so that the semiconductor devices have their second regions interconnected, their regions adjacent the substrate interconnected and individual metallized contacts each of which forms a Schottky barrier contact.

15. A semiconductor structure arranged and adapted to operate substantially as herein described with reference to and as shown in Figures 4 and 5 of Figure 7 or Figure 8 or Figure 9 of the drawings.

16. A method of making a semiconductor structure substantially as described with reference to Figures 4 and 5, or Figure 7 or Figure 8 or Figure 9 of the drawings.

17. A semiconductor integrated circuit arrangement substantially as herein described with reference to Figure 3 or Figure 6 of the drawings.

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