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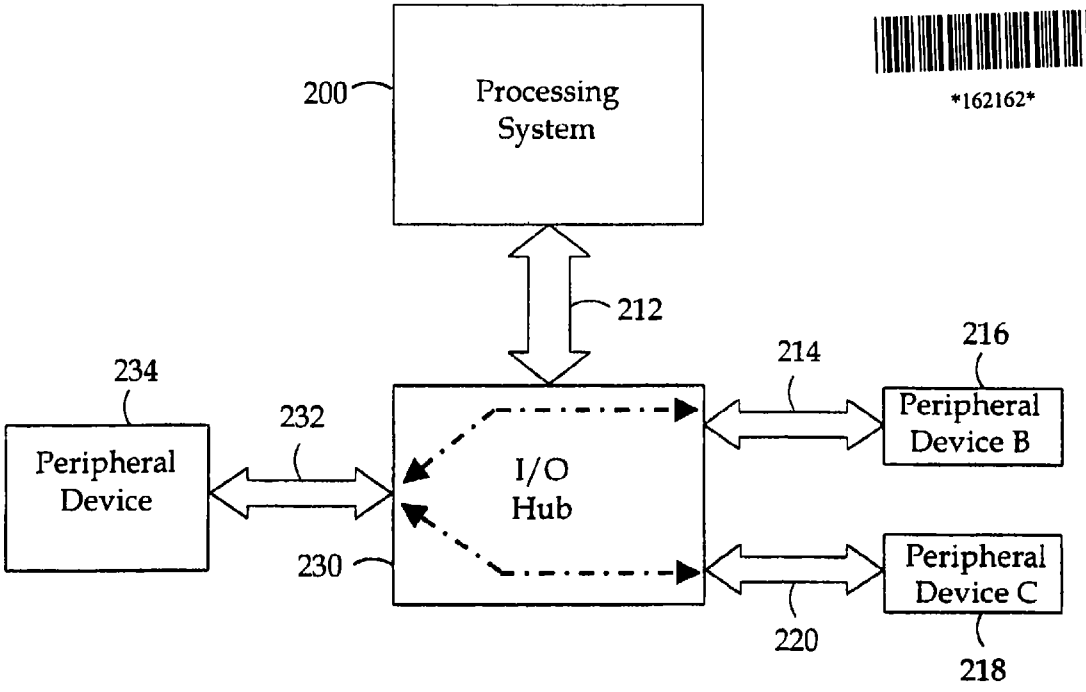
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(54) Title: COMPUTER PERIPHERAL DEVICE THAT REMAINS OPERABLE WHEN CENTRAL PROCESSOR OPERATIONS ARE SUSPENDED



(57) Abstract: A peripheral device having a circuit to detect the power management state of a central processor, a first interface to receive data, and a second interface to couple the peripheral device to the central processor. The peripheral device prevents data transfers that would cause the central processor to change from a second power management state to a first power management state if the central processor is in the second power management state.

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