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Semi-Insulating Diffusion Barrier for Low-Resistivity Gate Conductors

Abstract

A gate structure (10) for a semiconductor device, and particularly a MOSFET for such applications as CMOS technology is provided. The gate structure (10) entails an electrical insulating layer (14) on a semiconductor substrate (12), over which a polysilicon gate electrode (16) is formed. The gate structure (10) further includes a gate conductor (18) that is electrically connected with the gate electrode (16) through a diffusion barrier layer (20) having semi-insulating properties. The composition and thickness of the diffusion barrier layer (20) are tailored so that the barrier layer (20) is effective to block diffusion and intermixing between the gate conductor (18) and polysilicon gate electrode (16), yet provides sufficient capacitive coupling and/or current leakage so as not to significantly increase the gate propagation delay of the gate structure (10).

Figure 1

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