WHAT IS CLAIMED IS:

1. A vertical memory device, comprising:

a substrate including a first region and a second region at least partially surrounding the first region;

gate electrodes at a plurality of levels, the gate electrodes spaced apart from each other in a first direction substantially perpendicular to an upper surface of the substrate, each of the gate electrodes extending in a second direction substantially parallel to the upper surface on the first region and the second region, and the gate electrodes are stacked in a staircase shape on the second region;

a channel extending in the first direction on the first region, the channel extending through the gate electrodes;

a first conductive structure on an end portion of a first gate electrode among the gate electrodes, the end portion on the second region, the first gate electrode being disposed at a lowermost level of the plurality of levels; and

a second conductive structure spaced apart from the first conductive structure in the second direction on the second region, the second conductive structure not overlapping the first gate electrode in the first direction and being disposed at a height different from that of the first conductive structure,

wherein the substrate further includes a third region at least partially surrounding the second region, and

wherein the second conductive structure is disposed on the second region and a portion of the third region adjacent thereto.

2. The vertical memory device of claim 1, wherein the second conductive

structure is disposed at the height lower than the first conductive structure.

3. The vertical memory device of claim 1, wherein the second conductive structure is disposed at the height higher than the first conductive structure.

4. The vertical memory device of any one of claims 1 to 3, further comprising a third conductive structure spaced apart from the first and second conductive structures in the second direction, the third conductive structure not overlapping the first gate electrode in the first direction and being disposed at a height different from that of the second conductive structure.

5. The vertical memory device of any one of claims 1 to 4, wherein the first conductive structure is disposed at a position which is higher than the first gate electrode and disposed at the position which is lower than one of the gate electrodes closest to the first gate electrode in the first direction.

6. The vertical memory device of any one of claims 1 to 5, wherein the first and second conductive structures include a material substantially the same as that of the gate electrodes.

7. The vertical memory device of any one of claims 1 to 6, further comprising a blocking pattern including a metal oxide, the blocking pattern covering upper and lower surfaces and a sidewall of each of the first and second conductive structures.

8. The vertical memory device of any one of claims 1 to 7, further comprising a

first insulation pad spaced apart from the first conductive structure in the second direction on the second region, the first insulation pad not overlapping the first gate electrode in the first direction and being disposed at a height substantially the same as that of the second conductive structure.

9. The vertical memory device of claim 8, wherein the first insulation pad is spaced apart from the end portion of the first gate electrode in the second direction.

10. The vertical memory device of claim 8 or claim 9, wherein the first insulation pad includes silicon nitride.

11. The vertical memory device of any one of claims 8 to 10,

wherein the vertical memory device further comprises a second insulation pad at a height different from that of the second conductive structure on the third region.

12. The vertical memory device of any one of claims 1 to 11, wherein a plurality of first gate electrodes are spaced apart from each other in a third direction substantially parallel to the upper surface of the substrate and substantially perpendicular to the second direction, and

wherein a plurality of first conductive structures are spaced apart from each other in the third direction on the plurality of first gate electrodes.

13. The vertical memory device of any one of claims 1 to 12, wherein conductive pads are formed at end portions in the second direction of the gate electrodes, each of the conductive pads having a thickness greater than other portions of the gate

electrodes on which they are formed.

14. A vertical memory device, comprising:

a substrate including a cell array region, an extension region at least partially surrounding the cell array region, and a circuit region at least partially surrounding the extension region;

gate electrodes at a plurality of levels, the gate electrodes spaced apart from each other in a first direction substantially perpendicular to an upper surface of the substrate, each of the gate electrodes extending in a second direction substantially parallel to the upper surface of the substrate on the cell array region and the extension region of the substrate, and the gate electrodes being stacked in a staircase shape on the extension region of the substrate;

a channel extending in the first direction on the cell array region of the substrate, the channel extending through the gate electrodes;

a first insulation pad on a portion of the circuit region of the substrate spaced apart from an end portion, in the second direction, of a first gate electrode among the gate electrodes, the first gate electrode being disposed at a lowermost level of the plurality of levels, and the first insulation pad being higher than the first gate electrode with respect to the upper surface of the substrate; and

a second insulation pad spaced apart from the first insulation pad in the second direction on the circuit region of the substrate, the second insulation pad being at a height different from that of the first insulation pad,

wherein the first and second insulation pads include substantially the same material, and

wherein the vertical memory device further comprises, a conductive structure

disposed in the second direction on the extension region and a portion of the circuit region adjacent thereto.

15. The vertical memory device of claim 14, wherein the first and second insulation pads include a nitride.

16. A vertical memory device, comprising:

a substrate including a cell array region, an extension region at least partially surrounding the cell array region, and a circuit region at least partially surrounding the extension region;

gate electrodes at a plurality of levels, the gate electrodes spaced apart from each other in a first direction substantially perpendicular to an upper surface of the substrate, each of the gate electrodes extending in a second direction substantially parallel to the upper surface of the substrate on the cell array region and the extension region of the substrate, and the gate electrodes stacked in a staircase shape on the extension region of the substrate;

a channel extending in the first direction on the cell array region of the substrate, the channel extending through the gate electrodes;

a conductive structure higher than a first gate electrode among the gate electrodes and lower than a second gate electrode of the gate electrodes, the conductive structure overlapping an end portion of the first gate electrode in the first direction, the first gate electrode being adjacent to the upper surface of the substrate; and

a cut-off pattern extending in the first direction on the circuit region of the substrate, the cut-off pattern contacting the conductive structure,

wherein the conductive structure is disposed on the extension region and a portion of the circuit region adjacent thereto.

17. The vertical memory device of claim 16, wherein a plurality of first gate electrodes are spaced apart from each other in a third direction substantially parallel to the upper surface of the substrate and substantially perpendicular to the second direction, and

wherein the conductive structure overlaps an end portion of each of the first gate electrodes in the first direction.

18. The vertical memory device of claim 17, wherein a plurality of conductive structures are spaced apart from each other in the third direction, and wherein the cut-off pattern contacts each of opposite end portions, in the third direction, of each of the plurality of conductive structures.

19. The vertical memory device of any one of claims 16 to 18, further comprising an insulation pad on the circuit region of the substrate, at least a portion of the insulation pad having substantially the same height as that of the conductive structure and contacting the conductive structure.