

Power supply circuit with standby arrangement

The invention relates to a power supply circuit comprising: an input terminal, an output terminal and a reference terminal, for connection of a direct voltage source to the input terminal and the reference terminal and for connection of a load to the output terminal and the reference terminal, a series arrangement of an inductive element and a diode which are connected to one another in a first node, the inductive element being connected between the input terminal and the first node and the diode being connected between the first node and the output terminal, a first electronic switch having a main current path connected between the first node and the reference terminal, and a drive circuit for periodically making the main current path of the first electronic switch conductive and non-conductive.

The invention also relates to an electrical apparatus comprising such a power supply circuit.

Such a power supply circuit is known from United States Patent US 4,970,451. The known power supply circuit is of a configuration referred to in the literature as a "boost converter". Across the load an output voltage can be generated which is higher than the voltage from the direct voltage source. Converters of this type are used *inter alia* in battery-powered apparatuses in order to boost the comparatively low battery voltage to the operating voltage of the electronic circuitry of the apparatus. The aim is then to enable operation with a minimal number of batteries in series and hence with a battery voltage which is as low as possible. Many battery-powered apparatuses have a so-called standby mode, which is necessary in order to prevent certain measurement data from being lost. For example microprocessors, random access memories and the like are thus kept at a minimum operating voltage which is high enough to preclude loss of information.

It is an object of the invention to provide a boost converter which enables the load to be connected to the direct voltage source in the standby mode without mechanical switches and with a minimal voltage loss.

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To achieve this, in accordance with the invention, a power supply circuit of the type defined in the opening paragraph is characterized in that the drive circuit comprises a first switching device for making the main current path of the first electronic switch permanently non-conductive in response to a standby signal, and the
5 power supply circuit further comprises a second electronic switch having a control electrode, and a first and a second main electrode which constitute a main current path connected in parallel with at least the diode of the series arrangement of the inductive element and the diode, and a second switching device for making the main current path of the second electronic switch permanently conductive in response to the standby
10 signal.

The first switching device turns off the converter and the second electronic switch short-circuits the output terminal to the input terminal. This reduces the voltage loss across the inductive element and the diode. In particular the voltage loss across the diode is comparatively high if the direct voltage source comprises one or two
15 batteries arranged in series.

The second electronic switch itself also produces a voltage loss. In order to minimize this loss a first embodiment of a power supply circuit in accordance with the invention is characterized in that the second electronic switch is a MOSFET transistor having a source, a drain and a gate formed in a semiconductor body and
20 respectively corresponding to the first main electrode, the second main electrode and the control electrode of the second electronic switch.

The low drain-source resistance of a conductive MOSFET transistor connects the load to the direct voltage source virtually without any voltage loss, as opposed to a bipolar transistor which always carries a saturation voltage. An additional
25 advantage of a MOSFET transistor in comparison with a bipolar transistor is that hardly any current is needed to drive the control electrode of the MOSFET transistor, so that the direct voltage source is not loaded unnecessarily in the standby mode.

A second embodiment of the invention, which attractively simplifies the power supply circuit, is characterized in that the main current path of the second
30 electronic switch is connected between the first node and the output terminal, and the diode is formed by a parasitic body-to-drain diode of the MOSFET transistor.

The parasitic body-to-drain diode of the MOSFET transistor now also functions as the converter diode. This enables one diode to be dispensed with.



A third embodiment of a power supply circuit in accordance with the invention is characterized in that the power supply circuit further comprises: an auxiliary voltage terminal and a voltage doubler comprising a bootstrap capacitor, a smoothing capacitor, and a first and a second rectifier diode, the bootstrap capacitor
5 being connected between a tap of the inductive element and a node, the first rectifier diode being connected between the output terminal and the node, the second rectifier diode being connected between the node and the auxiliary voltage terminal, and the smoothing capacitor being connected between the auxiliary voltage terminal and the reference terminal.

10 When the first electronic switch is operative this enables an auxiliary voltage to be generated which is twice as high as the voltage on the output terminal. The bootstrap capacitor is connected to the first node or to a tap of the inductive element.

These and other aspects of the invention will now be described and
15 clarified with reference to the accompanying drawings, in which

Figure 1 shows a first embodiment of a power supply circuit in accordance with the invention,

Figure 2 shows a second embodiment of a power supply circuit in accordance with the invention,

20 Figures 3, 4, 5 and 6 show variants of the embodiments shown in Figures 1 and 2.

In these Figures parts having the same function or purpose bear the same references.

Figure 1 shows an embodiment of a power supply circuit in accordance
25 with the invention. A direct voltage source 2 has its positive pole connected to an input terminal 4 and its negative pole to a reference terminal 6 which is assumed to be earthed. By way of example the direct voltage source 2 is shown as a direct voltage battery but any other direct voltage source, such as an alternating voltage source with a rectifier, may be used. A load 8 is connected across an output terminal 10 and earth. A
30 smoothing capacitor 12, which is connected to the output terminal 10, suppresses ripple voltages which may be present on the output terminal 10. A series arrangement of an inductive element in the form of a coil 14 and a diode 16, which are connected to each other in a node 18, is arranged between the input terminal 4 and the output terminal 10.



Moreover, the coil 14 is connected to the input terminal 4 and the diode 16 has its cathode connected to the output terminal 10.

The main current path of an electronic switch formed by an NPN transistor 20 is connected between the first node 18 and earth. The first main electrode or emitter of the NPN transistor 20 is connected to earth. The second main electrode or collector of the NPN transistor 20 is connected to the node 18. The control electrode or base of the NPN transistor 20 is driven by a drive circuit 22 which periodically supplies current to the base of the NPN transistor 20 to turn on and turn off the NPN transistor 20.

The drive circuit 22 comprises a PNP transistor 24 having its emitter coupled to the input terminal 4 *via* a resistor 26, having its collector connected to the base of the NPN transistor 20, and having its base connected to earth *via* a resistor 28 and to the collector of the NPN transistor 20 *via* a capacitor 30. The drive circuit 22 further comprises an NPN transistor 32 whose emitter, collector and base are respectively connected to earth, the base of the NPN transistor 20 and the node between a zener diode 34 and a resistor 36. The zener diode 34 and the resistor 36 are arranged in series between a node 38 and earth and together they constitute a reference voltage source generating a constant voltage difference between the node 38 and the base of the NPN transistor 32.

The drive circuit further comprises a switching device 40 which activates and deactivates the drive circuit 22 by means of a standby signal SBS applied to a signal terminal 42. The switching device 40 comprises a PNP transistor 44 and the resistors 46 and 48. The base of the PNP transistor 44 is connected to the input terminal 4 *via* the resistor 46 and to the signal terminal 42 *via* the resistor 48. The PNP transistor 44 has its emitter connected to the input terminal 4 and its collector to the resistor 26.

A PMOS transistor 50, which functions as an electronic switch, is arranged in parallel with the diode 16. The source, drain and gate forming respectively the first main electrode, the second main electrode and the control electrode of the PMOS transistor 50 are connected to the output terminal 10, the node 18 and the node 38 respectively. The gate of the PMOS transistor 50 is driven by a switching device 52 comprising a PNP transistor 54 and the resistors 56, 58 and 60. The resistor 56 is connected between the node 38 and earth, the resistor 58 between the output terminal 10 and the base of the PNP transistor 54, and the resistor 60 between the signal terminal



42 and the base of the PNP transistor 54. The PNP transistor 54 has its emitter connected to the output terminal 10 and its collector to the node 38.

The standby signal SBS can be generated in various manners. One manner is, for example, by means of a switch connecting the signal terminal 42 to and
5 disconnecting it from earth. The disconnected state then denotes the standby mode. The PNP transistors 44 and 54 then do not conduct. As a result, the drive circuit 22 is not energized and the NPN transistor 20 is off. The power supply circuit is now in a passive state. The voltage on the output terminal 10 is then approximately one diode voltage below the voltage on the input terminal 4 as a result of the voltage drop across
10 the diode 16. The gate of the PMOS transistor 50 is connected to earth *via* the resistor 56, so that the main current path of the PMOS transistor 50 becomes conductive and forms a short-circuit across the diode 16. In this way it is achieved that in the standby mode the voltage across the load 8 is substantially equal to the voltage of the direct voltage source 2. This plays a role particularly if the direct voltage source 2 comprises
15 one or two battery cells. The voltage loss across the diode 16 is then comparatively large and could give rise to a premature incorrect operation of the load in the standby mode. Examples of loads are microprocessors, random access memories and other digital and/or analog circuits which should remain operative in the standby mode in order to preclude loss of information. It is to be noted that the switching devices 40 and
20 52 do not draw any current from the direct voltage source 2 in the standby mode. This is favourable when batteries are used. Instead of the PMOS transistor 50 it is possible to use a bipolar PNP transistor, as is shown in Figure 3. However, even in the case of a small load current the saturation voltage of such a transistor causes a voltage loss between the input terminal 4 and the output terminal 10. This may be undesirable.
25 Besides, a certain amount of base current is needed for driving a bipolar transistor, which current must be supplied by the direct voltage source 2 in the standby mode.

The power supply circuit is activated when the standby signal SBS connects the signal terminal 42 to earth. In that case the PNP transistors 44 and 54 are conductive. The PNP transistor 54 then connects the node 38 to the output terminal 10.
30 The gate-source voltage of the PMOS transistor 50 is then substantially zero and the PMOS transistor 50 is turned off. By means of the PNP transistor 44 the emitter of the PNP transistor 24 is connected to the input terminal 4 *via* the resistor 26. Now a base current can flow into the PNP transistor 24 *via* the resistor 28 and the resulting



collector current flows to the base of the NPN transistor 20, which is driven into saturation. The collector voltage of the NPN transistor 20 then exhibits a negative transient, which is transferred to the base of the PNP transistor 24 by the capacitor 30, as a result of which the PNP transistor 24 is also saturated. The resistor 26 limits the current through the PNP transistor 24. The collector current through the NPN transistor 20 also flows through the coil 14 and increases as a linear function of time. The diode 16 is then cut off. For a certain value of the collector current through the NPN transistor 20 this transistor is desaturated and the collector voltage rapidly increases in a positive sense. The capacitor 30 transfers this voltage increase to the base of the PNP transistor 24, so that this transistor and hence the NPN transistor 20 are turned off. The current through the coil now finds its way to the load 8 and the smoothing capacitor 12 through the diode 16 which is now conductive. The current through the coil 14 then decreases to zero and the collector voltage of the NPN transistor 20 decreases to the voltage on the input terminal 4. After this the capacitor 30 can discharge to earth via the resistor 28 and drive the base of the PNP transistor 24 to turn on this transistor. This cycle repeats itself. The power supply is self-oscillating (SOPS). If the voltage on the output terminal 10 and hence that on the node 38 exceeds a given value the zener diode 34 is turned on. The NPN transistor 32 is then driven into conduction and turns off the NPN transistor 20 prematurely. The peak value of the current in the coil 14 is limited to such an extent that the voltage on the output terminal 10 does not increase any further. This voltage is equal to the sum of the base-emitter voltage of the NPN transistor 32, the zener voltage of the zener diode 34 and the collector-emitter saturation voltage of the PNP transistor 54. This SOPS operates at a substantially constant frequency, which may be advantageous for the dimensioning of the coil 14.

25 The internal body-to-drain diode of the PMOS transistor can also preform the function of the diode 16, so that no separate diode 16 is needed in that case. If required, the PMOS transistor 50 may be arranged between the input terminal 4 and the output terminal 10, as is shown in Figure 4, so that the coil is also bypassed in the standby mode. In that case a separate diode 16 is necessary.

30 At option the power supply circuit may further comprise a diode 62 having its cathode connected to the node 38 and its anode to an output terminal 64 to which a load 66 can be connected, and a smoothing capacitor 68 to suppress ripple voltages on the output terminal 64. The diode 62 isolates the load 66 from the power



supply circuit in the standby mode, so that it cannot be energized. In this way a distinction can be made between a load 8 which is energized in the standby mode and a load 66 which is not energized in the standby mode.

Further optional parts are an auxiliary voltage terminal 69 for the
5 connection of a load 70, a bootstrap capacitor 72, a smoothing capacitor 74, and the diodes 76 and 78, which parts are arranged to form a voltage doubler. The bootstrap capacitor 72, the cathode of the diode 76 and the anode of the diode 78 are interconnected. The other terminals of these elements are respectively connected to the
10 node 18, the output terminal 10 and the auxiliary voltage terminal 69, to which the smoothing capacitor is also connected. In the standby mode the load 70 is isolated from the power supply circuit in the same way as the load 66 by a diode, *i.e.* the diode 78.

As is shown in Figure 5 the bootstrap capacitor 72 may be connected to a tap of the coil 14. Figure 6 shows the possibility of using a transformer 80 of which one winding forms the coil 14.

15 Figure 2 shows another embodiment of a power supply circuit in accordance with the invention. This embodiment is largely identical to that shown in Figure 1. The resistor 26 is now connected directly to the input terminal 4. The resistor 28 is dispensed with and the NPN transistor 32 is replaced by an NPN transistor 82 whose emitter is connected to earth and its collector to the base of the PNP transistor
20 24. The base-emitter junction of the NPN transistor is connected in parallel with the corresponding junction of an NPN transistor 84 having its collector and its base interconnected. The two NPN transistors 82 and 84 are arranged as a current mirror whose input, which is formed by the collector of the NPN transistor 84, is connected to an output 86 of a differential amplifier 88. A first inverting input 90 of this amplifier is
25 connected to a tap 92 of a voltage divider comprising two resistors 94 and 96 arranged in series between the node 38 and earth. The two resistors 94 and 96 also perform the function of the resistor 56 in the embodiment shown in Figure 1. A second non-inverting input 98 is connected to a reference voltage source 100, which generates a reference voltage relative to earth and which is energized from the node 38 *via* a
30 resistor 101.

The differential amplifier 88 comprises a differential pair of PNP transistors 102 and 104 whose emitters are connected to the node 38 *via* a resistor 106. The inputs 90 and 98 are formed by the base terminals of the PNP transistors 102 and

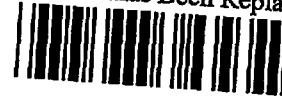


104 respectively. The collector of the PNP transistor 104 is connected to the collector of a diode-connected NPN transistor 108 having its base-emitter junction arranged in parallel with the corresponding junction of an NPN transistor 110. The emitters of the NPN transistors 108 and 110 are connected to earth. The collectors of the PNP
5 transistor 102 and of the NPN transistor 110 are interconnected, their node forming the output 86 of the differential amplifier 88.

In the present configuration the NPN transistor 82 functions as a variable resistor whose resistance is controlled by the differential amplifier in dependence upon the voltage difference between the tap 92 and the reference voltage from the reference
10 voltage source 100. This causes a change of the time constant with which the capacitor 30 is charged. The switching frequency of the SOPS will decrease to counteract an increasing voltage on the node 38 and hence on the output terminal 10. In the standby mode the differential amplifier 88 is no longer powered. The NPN transistor 82 then receives no base current and is turned off, so that the PNP transistor 24 neither receives
15 a base current. The oscillation ceases. This configuration does not require a switching device comparable with the switching device 40 in the embodiment shown in Figure 1.

The invention is not limited to the embodiments shown herein. The bipolar transistors may be replaced by their unipolar counterparts. In that case the source, drain and gate of a unipolar transistor take the place of the emitter, collector
20 and base of a bipolar transistor.

The power supply circuit is eminently suitable for use in consumer appliances with rechargeable batteries, such as for example shavers having sophisticated electronic devices for measuring, monitoring and displaying the battery status and for measuring the current consumption of the motor. The measurement data should not be
25 lost when the shaver is switched off. With the power supply circuit in accordance with the invention it is possible even at comparatively low battery voltages to use conventional digital circuits, such as microprocessors, which otherwise could not have remained connected directly to the output terminal 10 in the standby mode on account of too low a supply voltage. In addition, the power supply circuit is also suitable for use in
30 portable communication equipment such as radio and television receivers, telephone sets and the like and in portable computers and other digital equipment.

Claims:

1. A power supply circuit comprising: an input terminal (4), an output terminal (10) and a reference terminal (6), for connection of a direct voltage source (2) to the input terminal (4) and the reference terminal (6) and for connection of a load (8) to the output terminal (10) and the reference terminal (6), a series arrangement of an
5 inductive element (14) and a diode (16) which are connected to one another in a first node (18), the inductive element (14) being connected between the input terminal (4) and the first node (18) and the diode (16) being connected between the first node (18) and the output terminal (10), a first electronic switch (20) having a main current path connected between the first node (18) and the reference terminal (6), and a drive circuit
10 (22) for periodically making the main current path of the first electronic switch (20) conductive and non-conductive, characterized in that the drive circuit (22) comprises a first switching device (40) for making the main current path of the first electronic switch (20) permanently non-conductive in response to a standby signal (SBS), and the power supply circuit further comprises a second electronic switch (50) having a control
15 electrode, and a first and a second main electrode which constitute a main current path connected in parallel with at least the diode (16) of the series arrangement of the inductive element (14) and the diode (16), and a second switching device (52) for making the main current path of the second electronic switch (50) permanently conductive in response to the standby signal (SBS).
- 20 2. A power supply circuit as claimed in Claim 1, characterized in that the second electronic switch (50) is a MOSFET transistor having a source, a drain and a gate formed in a semiconductor body and respectively corresponding to the first main electrode, the second main electrode and the control electrode of the second electronic switch (50).
- 25 3. A power supply circuit as claimed in Claim 1 or 2, characterized in that the main current path of the second electronic switch (50) is connected between the first node (18) and the output terminal (10).



4. A power supply circuit as claimed in Claim 3, characterized in that the diode (16) is formed by a parasitic body-to-drain diode of the MOSFET transistor (50).

5. A power supply circuit as claimed in Claim 3 or 4, characterized in that the second switching device (52) comprises: a first resistor (56) connected to a second
5 node (38) between the control electrode of the second electronic switch (50) and the reference terminal (6), and a switching transistor (54) having a main current path connected between the output terminal (10) and the second node (38) and having a control electrode arranged to receive the standby signal (SBS).

6. A power supply circuit as claimed in Claim 1, 2, 3, 4 or 5, characterized
10 in that the first electronic switch (20) is a transistor of a first conductivity type and having a first main electrode connected to the reference terminal (6), a second main electrode connected to the first node (18), and a control electrode, the drive circuit (22) comprises: a second resistor (26), a second transistor (24) of a second conductivity type opposite to the first conductivity type, a third transistor (32) of the first conductivity
15 type, the second (24) and the third (32) transistor each having a first main electrode, a second main electrode and a control electrode, the second main electrode of the second transistor (24) and the second main electrode of the third transistor (32) being connected to the control electrode of the first transistor (20), and the first main electrode of the third transistor (32) being connected to the reference terminal (6), a capacitor (30)
20 connected between the second main electrode of the first transistor (20) and the control electrode of the second transistor (24), a third resistor (28) connected between the control electrode of the second transistor (24) and the reference terminal (6), and a reference voltage source (34, 36) connected between the control electrode of the third transistor (32) and the second node (38), and the first switching device (40) comprises a
25 fourth transistor (44) of the second conductivity type having a main current path connected in series with the second resistor (26) between the input terminal (4) and the first main electrode of the second transistor (24) and having a control electrode arranged to receive the standby signal (SBS).

7. A power supply circuit as claimed in Claim 1, 2, 3, 4 or 5, characterized
30 in that the first electronic switch (20) is a transistor of a first conductivity type and having a first main electrode connected to the reference terminal (6), a second main electrode connected to the first node (18), and a control electrode, the drive circuit (22) comprises: a second resistor (26), a second transistor (24) of a second conductivity type



opposite to the first conductivity type, a third transistor (82) of the first conductivity type, the second (24) and the third (82) transistor each having a first main electrode, a second main electrode and a control electrode, the first main electrode of the second transistor (24) being connected to the input terminal (4) *via* the second resistor (26), the
5 second main electrode of the second transistor (24) being connected to the control electrode of the first transistor (20), and the first main electrode of the third transistor (82) being connected to the reference terminal (6), a capacitor (30) connected between the second main electrode of the first transistor (20) and the control electrode of the second transistor (24), a reference voltage source (110), a voltage divider (94, 96)
10 connected between the second node (38) and the reference terminal (6) and having a tap for supplying a fraction of a voltage difference prevailing between the second node (38) and the reference terminal (6), a differential amplifier (88) having a first (90) and a second (98) input connected to the tap (92) and the reference voltage source (100) respectively, and having an output (86) coupled to the control electrode of the third
15 transistor (82).

8. A power supply circuit as claimed in Claim 5, 6 or 7, characterized in that the power supply circuit further comprises: a further output terminal (64) and a further diode (62) arranged between the second node (38) and the further output terminal (64).

20 9. A power supply circuit as claimed in Claim 1, 2, 3, 4, 5, 6, 7 or 8, characterized in that the power supply circuit further comprises: an auxiliary voltage terminal (69) and a voltage doubler comprising a bootstrap capacitor (72), a smoothing capacitor (74), and a first (76) and a second (78) rectifier diode, the bootstrap capacitor (72) being connected between a tap (18) of the inductive element (14) and a node, the
25 first rectifier diode (76) being connected between the output terminal (10) and the node, the second rectifier diode (78) being connected between the node and the auxiliary voltage terminal (69), and the smoothing capacitor (74) being connected between the auxiliary voltage terminal (69) and the reference terminal (6).

10. An electrical apparatus comprising a power supply circuit as claimed in
30 Claim 1, 2, 3, 4, 5, 6, 7, 8 or 9.

